Characterisation of Polarization Super-Junction Power devices in Gallium Nitride

By

Yangming Du

Department of Electronic and Electrical Engineering

A thesis submitted to the University of Sheffield

for the degree of Doctor of Philosophy

October 2022

Acknowledgements

I want to sincerely thank and respect my supervisor, Prof. Shankar Ekkanath Madathil, for his patient and kind supervision, insightful advice, and inspirational words. I am able to carry out my doctoral studies thanks to his confidence and encouragement.

Additionally, I want to express my gratitude to Dr Akira Nakajima from AIST, Japan, for the insightful remarks on the PSJ diode current saturation behaviour through our Skype calls. I was motivated to investigate this research topic by his recommendations and thoughts on this work. Thanks to Dr Hiroji Kawai, Shuichi Yagi, and Hironobu Narui at POWDEC.K.K in Japan, I was able to do my tests using fantastic PSJ power devices. as well as their insightful remarks on my research and paper.

I want to express my gratitude to the entire EEE department personnel at the University of Sheffield. I thank Mr Adam Stroughair, Dr Kean Boon Lee, and the other technical staff members for their assistance and support with the cleanroom training. I also want to thank Dr Gavin L. Williams for the assistance with the measurements.

My deepest appreciation and compliments go out to my Power Microelectronics Team colleagues. I appreciate the warm assistance and patient introduction to my research work from Dr Hong Yao Long when I joined the team group. I would especially want to thank Mr Hongyang Yan and Dr Peng Luo for their assistance with the fabrication and discussion of my work. A special thanks go out to Mr Alireza Sheikhan, who gave me advice and assisted me with the circuit tests.

Last but not least, I'd like to use this chance to thank my parents in the sincerest way possible. Their motivation and assistance allow me to concentrate on my scholarly studies. I want to sincerely thank Yue Wang, my girlfriend, and tell her how much I adore her. My life is brightened by her unfailing love and support during our phone chats, which is how she helps me get over the difficulties and obstacles of my academic research job.

Abstract

GaN Polarisation Superjunction (PSJ) technology utilises charge balance concepts using the polarisation effects in GaN, significantly enhancing the blocking voltage of GaN power devices. Due to these advantages, it has become one of the promising candidates for the next generation of GaN Power technology. Further exploring findings of the characterisation of the PSJ power devices are introduced in this thesis. POWDEC.K.K, Japan, is one of the first companies which started to investigate PSJ technology. They have made several new PSJ power devices and presented their electrical performances based on their mature and complete technologies, including GaN wafer epitaxial growth, wafer process fabrication, dicing and packaging[1], [2].

The findings obtained from the POWDEC.K.K PSJ samples include (1) the impacts from the top u-GaN and AlN nucleation layer on the sheet density of 2DEG and 2DHG, (2) the mechanisms of the current saturation of PSJ diodes and (3) gate reliability and leakage performance of PSJ HFETs. Moreover, the performances of the PSJ-on-Si power devices obtained from the fabricated samples in Sheffield are also introduced in this thesis.

The impacts from the top u-GaN layer thickness on the sheet density of 2DEG and 2DHG in u-GaN/AlGaN/u-GaN double heterostructures are analysed through the theoretical model. It found that the top surface potential determines the relationship. Under the free surface condition, the sheet density of 2DHG is inconsistent with u-GaN thickness. However, the sheet density of 2DHG rises when the Schottky surface conditions are introduced. Similar conclusions can be drawn from the PSJ heterostructures with a P-GaN cap layer. Furthermore, the AlN nucleation layer effects on the 2DEG sheet density are relevant to the relationship between the AlN nucleation layer and u-GaN buffer layer thickness.

The current saturation behaviour and the saturation mechanisms of the unipolar power GaN diodes: Conventional AlGaN/GaN diode and PSJ hybrid diode are firstly reported and discussed. It is found that velocity saturation, together with the minimal

conductivity modulation induced by the minority carrier in the drift region, is the main reason for the saturation behaviour in these two diodes. Moreover, a unique current saturation behaviour of the forward I-V characteristics of the bipolar PSJ PiN diode is also discussed. The negligible and localised conductivity modulation is one of the critical causes of this phenomenon. Moreover, according to the simulation results, trap-induced velocity saturation is also responsible for the current saturation behaviour in the PSJ PiN diodes.

The shift in threshold voltages (V_{th}) of 1.2 kV P-GaN ohmic-gate Normally-on Polarization Superjunction (PSJ) HFETs is reported for the first time. A comprehensive analysis of threshold voltage shifts and recovery processes under different gate stress voltages and temperatures is presented. Temperature effects on the V_{th} shift are also evaluated. Compared with the P-GaN gate HEMTs, the Pulsed I_d-V_d results confirm that the current collapse induced by the Vth instability is relatively low in PSJ HFETs. Moreover, the V_{th} shift in 1.2kV PSJ Schottky gate HFETs is also investigated.

The characteristics of the P-type ohmic gate leakage current is also examined. And its unique saturation behaviour is presented and explored. Finally, it details how the leakage current operates in the saturation and non-saturation regions.

The fabrication process flow and electrical performances of the PSJ-on-Si power semiconductor devices at the University of Sheffield are firstly presented. It includes the on-state and breakdown characteristics of PSJ HFETs and PSJ hybrid diodes. Furthermore, the current density and specific on-state resistance are also studied as a function of the finger length, quantity and temperature.

Contents

Acknowledgements ii

Abstract iii

Chapter 1. Introduction 1

1.1. Overview 1

1.2. Introduction of Power semiconductor devices 4

1.3. Thesis organisation 5

Chapter 2. Background of Gallium Nitride (GaN) HFETs 9

2.1. GaN Material Property 9

2.2. Substrates for GaN Power devices 13

2.3. Polarisation Effects 17

2.3.1. Spontaneous Polarisation 18

2.3.2. Piezoelectric Polarisation 20

2.4. AlGaN/GaN heterostructures and the formation of 2DEG 23

2.4.1. Polarisation charge 23

2.4.2. Origin of 2DEG 28

2.5. Conventional AlGaN/GaN High Electron Mobility Transistor (HEMT) 35

2.5.1. The operation principle of conventional AlGaN/GaN HEMTs 36

2.5.2. Introduction of field-plate technology 39

2.5.3. Introduction of the RESURF concept 43

2.5.4. Introduction of Si Superjunction 46

2.6. GaN Polarisation Superjunction technology (PSJ) 49

2.7. Current collapse 54

2.8. Summary 58

Chapter 3. Theoretical Analysis of the Sheet Density of 2DEG and 2DHG in Polarization Super-Junction Heterostructures 60

3.1. Top u-GaN layer thickness 60

3.1.1. U-GaN/AlGaN/u-GaN heterostructures 62

3.1.2. P-GaN/GaN/AlGaN/GaN Heterostructures 68

3.2. The AlN nucleation layer thickness 76

3.3. Summary 79

Chapter 4. Fabrication and Evaluation of PSJ-on-Si Power devices 81

4.1. Design objective 81

4.2. Device design information 82

4.3. Device fabrication 83

4.4. Electric characterisation of fabricated PSJ-on-Si devices 83

4.4.1. PSJ hybrid diodes (test structure) 84

4.4.2. PSJ hybrid diodes(large-area) 88

4.4.3. Temperature effects on PSJ hybrid diodes 91

4.4.4. PSJ hybrid diode reverse blocking characteristics 93

4.4.5. PSJ HFETs (I-V static characteristics) 98

4.4.6. The Off-state Breakdown Voltage(BV) for PSJ HFETs 103

4.5. Summary 106

Chapter 5. Investigation of Shift in Threshold Voltages of 1.2kV GaN Polarization Superjunction (PSJ) HFETs 108

5.1. Threshold Voltage (V_{th}) shift in P-GaN gate PSJ HFETs 108

5.1.1. Introduction 108

5.1.2. Device structure and dimensions 110

5.1.3. Pulse-mode measurement setup and conditions 111

5.1.4. V_{th} shift under positive gate stress voltages 113

5.1.5. Vth shift under negative gate stress voltages 119

5.1.6. The Vth shifts under positive stress voltages as a function of temperature 123

5.2. Threshold Voltage (V_{th}) shift in Schottky gate PSJ HFETs 125

5.2.1. Devices structures, parameters and fabrication details 125

5.2.2. Vth shift under positive and negative gate stress voltage 126

5.3. Summary 128

Chapter 6. GaN Polarization Superjunction diode current saturation behaviour 130

6.1. Current saturation behaviour in conventional AlGaN/GaN diode 130

6.1.1. Device structures and Measurement results 130

6.1.2. Simulation results and analysis 133

6.2. PSJ Hybrid diode current saturation behaviour 136

6.2.1. Introduction 136

6.2.2. Measurement results 137

6.2.3. Simulation results and analysis 139

6.3. Current saturation behaviour in PSJ PiN diode 144

6.3.1. Introduction 144

6.3.2. Device structures and measurement results 145

6.3.3. Conductivity modulation evaluation in PSJ PiN diode 147

6.3.4. Trap effects on the current saturation 150
6.4. Summary 157
Chapter 7. Gate leakage current mechanisms of PSJ HFETs 159
7.1. Introduction 159
7.2. Device structures and parameters 161
7.3. Electric static characteristics of devices 162
7.4. Gate leakage current measurement results 162
7.5. Mechanisms of gate leakage Current at the saturation region ($V_g \leq V_{th}$=-5V) .. 164
7.6. Mechanisms of gate leakage current at the non-saturation region (Vg ≥Vth=-5V) 168
7.7. Summary 171
Chapter 8. Conclusions and Future work 172
8.1. Conclusions 172
8.2. Future work 175
Appendix-1 178
Mask design 178
Sample dicing size and cleaning preparation steps 181
Fabrication process flow 182
Fabricated devices/sample 187
Appendix-2: References 188
Appendix-3: List of Figures 207
Appendix-4: List of Tables 221

Chapter 1. Introduction

1.1. Overview

The International Energy Outlook 2021 states that total world energy consumption has grown from around 550 quadrillions (10^{15}) British thermal units(Btu) in 2010 to about 600 quadrillions Btu in 2020 shown in Figure 1.1[3]. Although it dropped slightly during 2020 because of the pandemic of COVID-19 and climate change, the world's energy consumption is predicted to be back to the pre-pandemic level. It will keep increasing until 2050 due to economic and population growth[3]. However, as Figure 1.2 illustrates, the primary energy consumption composition is expected to be changed in 2050 [3]. The

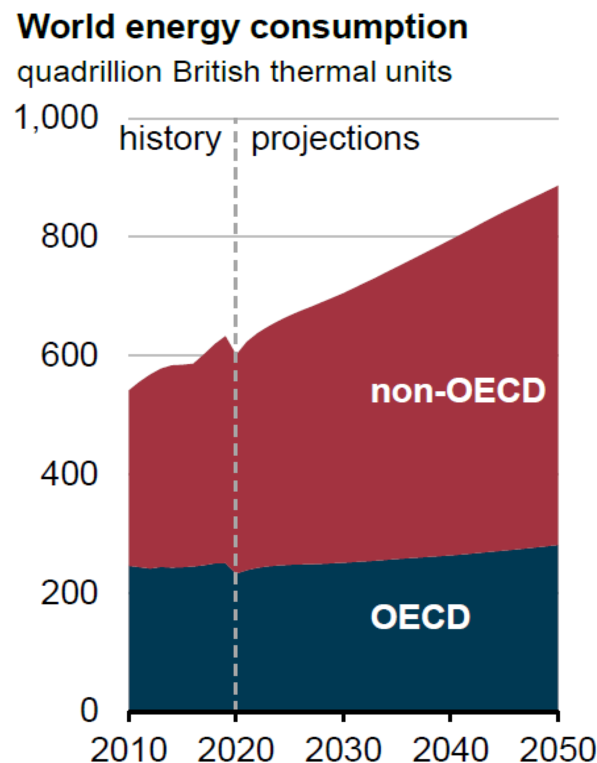


Figure 1.1 World energy consumption: history and projection from 2010-2050 [3].

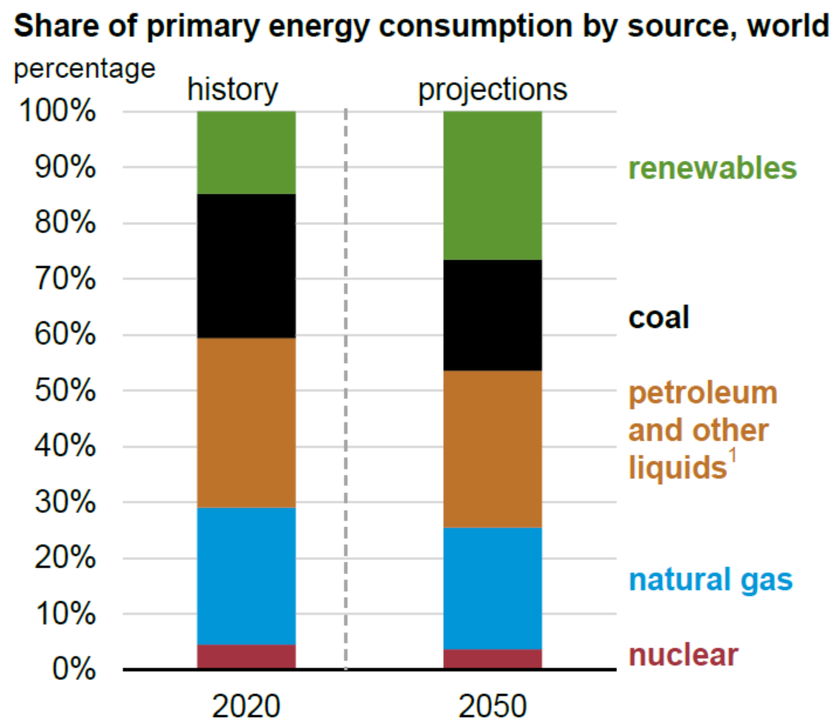


Figure 1.2 Share primary energy consumption by source in 2020 and the prediction in 2050[3].

renewable energy source is projected to increase from around 15% in 2020 to 25% in 2050. Still, the traditional fossil fuel, including coal, natural gas, petroleum and other liquids, will decrease due to the lowering of greenhouse gases emission and minimising the global warming effects.

However, renewable energy sources cannot be regarded as a reliable supply of energy to support economic growth and technological advancement. Moreover, due to the high expenses of equipment and transportation, the price of renewable energy is much higher than that of fossil fuel, causing more severe problems in economic growth and other social issues.

Energy efficiency improvement and waste reduction are hot topics because of the rising demand for energy and the anticipated shortage in the following decades. Electricity power, a renewable source, is widely used in power

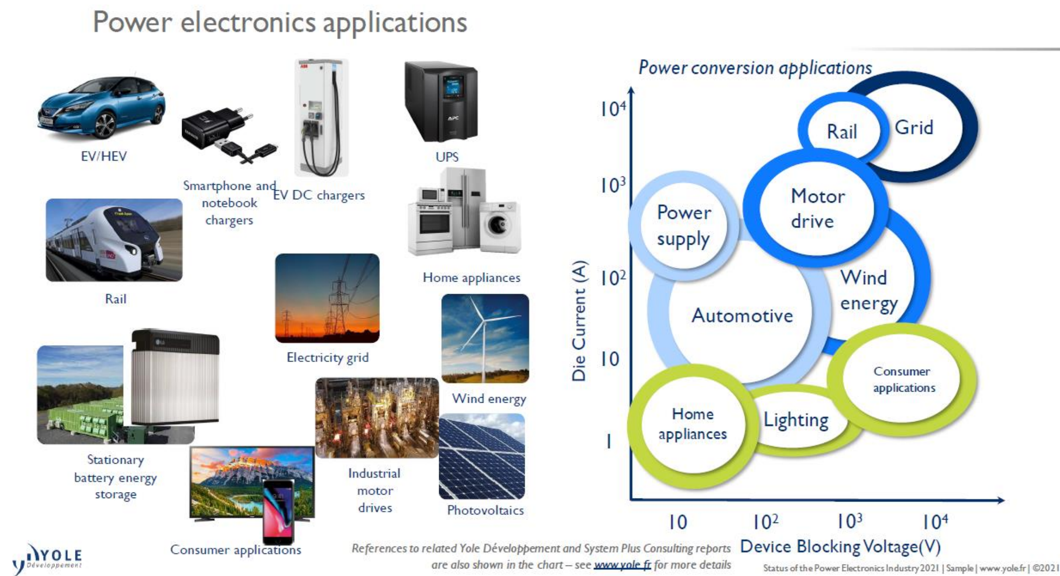


Figure 1.3 Power electronics applications[4].

electronic systems. Enhancing energy efficiency and reducing energy waste in power electronic systems are therefore essential

Power electronic systems have various applications due to the widespread and rapid advancement of electronic technology over the past few decades. Yole development reported the status of the power electronic industry applications in 2021[4]. According to the die current and the device blocking voltage of power electronics, the applications range from consumer applications, home appliances, and lighting to industrial motor drives, power supply, wind energy, automotive, rail, electricity grid, etc. [4].

1.2. Introduction of Power semiconductor devices

Power semiconductor devices play a critical role in power electronic systems. Due to the wide range of applications mentioned above, the devices are required to operate under different conditions to meet the various requirements. Figure 1.4 presents the positioning of the power semiconductor devices technology concerning the operating frequency in 2021[5].Silicon(Si) power devices, including Si thyristor and IGBT (Insulated Gate Bipolar Transistor), are mainly operated under relatively low operating frequency (below 10^4 Hz) but relatively high switching power[5]. However, metal-oxide semiconductor field-effect transistors (Si MOSFETs) are employed at a relatively higher frequency.

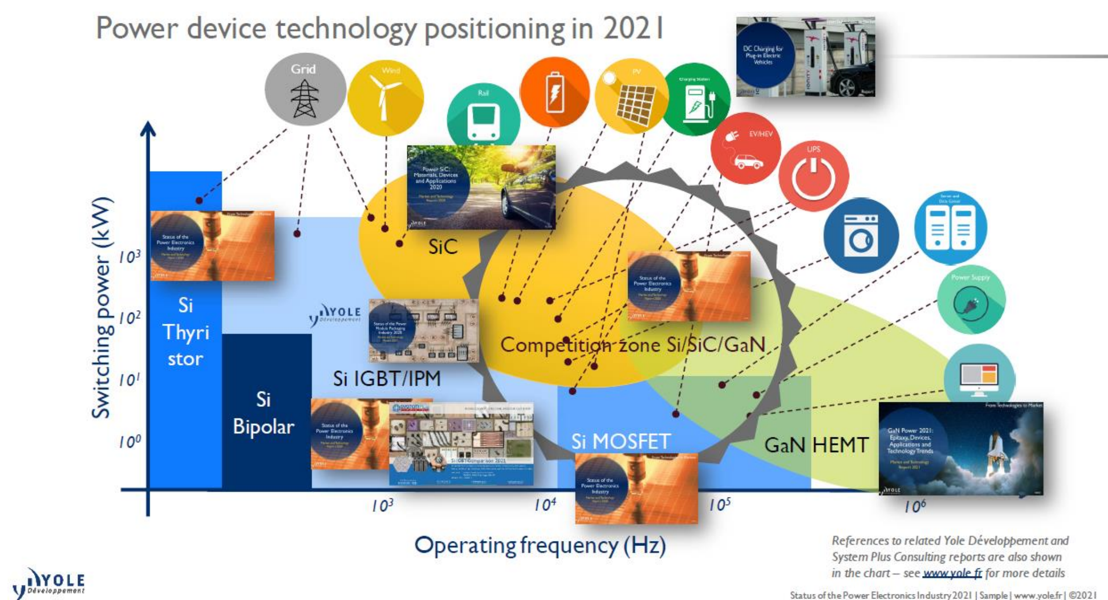


Figure 1.4 Power device technology positioning in 2021[5].

Recently, Wide Band Gap (WBG) material-based, such as silicon carbide (SiC) and gallium nitride (GaN), power devices are emerging as competitive alternatives which are due to their inherent material properties. As Figure 1.4

illustrates, GaN-based power devices are gaining popularity because of their extremely fast switching speed and relatively low switching loss[5]. However, compared with Si and SiC-based power devices, GaN-based power devices are mainly utilised for low-power applications (the maximum rated voltage for commercial GaN power devices is below 650V). Therefore, the technology for enhancing the breakdown voltage for GaN power devices is becoming essential. GaN Polarisation Superjunction (PSJ) technology combines the polarisation effects and superjunction technology, significantly increasing the breakdown voltage of GaN power devices (over 2kV). All these advantages make GaN PSJ power devices the most competitive candidates for next-generation technology for GaN power devices.

However, as an emerging technology, more topics on the characterisation of GaN PSJ power devices are still under investigation to further understand their mechanisms and improve their performances. This thesis is devoted to exploring the impacts from the top u-GaN and AlN nucleation layer thickness on the sheet density of 2DEG and 2DHG, respectively, the performances of the PSJ power devices on Si substrates, PSJ diode current saturation behaviour and PSJ gate performance and reliability.

1.3. Thesis organisation

The structure of the thesis is as follows:

The background information about the current condition, energy consumption projections, and the use of power electronic devices are briefly introduced in Chapter 1.

GaN material physical characteristics and the basic idea of polarisation effects in AlGaN/GaN heterostructures are initially covered in chapter 2. Additionally, the origin of 2DEG and the fundamental electric properties of the GaN High Electron Mobility Transistor (HEMT) in the context of the application to power devices are presented. Moreover, examples of the device structures and operational principles in both the on-state and off-state are given. However, because of the uneven electric field distribution, conventional AlGaN/GaN HEMTs are unable to block the high voltage. Additionally, examples of the RESURF and Field-plate approaches for managing the electric field, frequently employed in conventional GaN power devices, are provided. Additionally, the operational principles of the PSJ Heterostructures Field effect transistors (HFETs) and diodes, as well as the polarisation Superjunction (PSJ) as a compensation idea for optimising the electric field distribution and boosting the breakdown voltage are discussed in detail.

Theoretical analysis of the 2DEG and 2DHG sheet densities in various PSJ heterostructures is covered in Chapter 3 as a function of the top u-GaN layer. Following the theoretical analysis approach and measurements, the effects of the SiO2 passivation layer, such as thickness and other impacts, on the density

of 2DEG and 2DHG are examined. Furthermore, the impacts of introducing the AlN nucleation layer in the PSJ heterostructures on the sheet density of 2DEG are also reported.

Chapter 4 describes the details of the PSJ-on-Si power devices fabricated at the University of Sheffield, including the fabrication process flow, alignment rules, mask design and electric performance. Also, the measured on-state performance and breakdown performances of PSJ HFETs and diodes are presented.

In chapter 5, the threshold voltage (V_{th}) shift mechanisms of 1.2kV P-GaN gate PSJ HFETs are investigated based on the pulsed-mode measurement results under different gate stress voltages. Furthermore, the temperature effects on the shifts are also discussed. As a comparison, the V_{th} shift performances are also investigated in PSJ Schottky gate HFETs.

In chapter 6, the PSJ diode current saturation behaviour is first reported, and their mechanism is investigated. The current saturation behaviour of the unipolar GaN power diodes, including the PSJ hybrid diode and conventional AlGaN/GaN diode, is discussed. Velocity saturation in the pinch-off region is the main cause of this phenomenon. However, the current saturation behaviour mechanisms in the bipolar PSJ PiN diode are different. The localised and negligible conductivity modulation, together with the trap effects, causes saturation behaviour.

In chapter 7, the gate leakage current mechanisms of P-GaN gate PSJ HFETs are reported and discussed in detail.

The study described in this thesis is concluded in Chapter 8, and future research and future research work are also discussed.

Chapter 2. Background of Gallium Nitride (GaN) HFETs

The physical material properties of Gallium Nitride (GaN) are first mentioned in this chapter. The polarisation effects and the origin of 2DEG in the AlGaN/GaN heterostructures are then thoroughly explored. The operation principles and electrical characteristics of conventional AlGaN/GaN High Electron Mobility Transistors (HEMTs) are also introduced. The technologies for managing the electric field in power devices are also presented, including the field plate (FP), RESURF, and Superjunction (SJ) technologies. Finally, the concept and structure of GaN Polarisation of Superjunction (PSJ) are introduced and their advantages are explained.

2.1. GaN Material Property

One of the III-V wide bandgap semiconductor materials is gallium nitride (GaN) [6]. Table 21 lists some of the inherent Si properties as well as the key wide bandgap semiconductor features for Si, diamond, 4H-SiC, and GaN[7]. Wide bandgap semiconductor materials, such as 4H-SiC and GaN, can attain greater breakdown voltages than Si because they have a higher critical electric field [8]. Si, GaN, and diamond, which have high electron mobility, may have comparatively low on-state resistance and fast switching speed, indicating that

Table 2-2 Main figures of merit for WBG semiconductors compared with Si[9], [10]

FOM	Si	4H-SiC	GaN	Diamond
BFOM ($\varepsilon_r \cdot \mu \cdot E_c^3$)	1	488	2414	8964
BHFOM ($\mu \cdot E_c^2$)	1	62	221	762
JFOM ($(E_c \cdot v_{sat}/2\pi)_2$)	1	366	1287	4322
KFOM ($\lambda \cdot \sqrt{(vsat/\varepsilon r)}$)	1	4.0	1.6	31.5
HMFOM ($E_c \sqrt{\mu}$)	1	7.5	8	23.8
HCAFOM ($\varepsilon_r \sqrt{\mu} E_c^2$)	1	65.9	61.7	220.5
HTFOM ($\lambda / \varepsilon r \cdot E_c$)	1	0.6	0.1	1.7

they have low conduction and switching losses. The saturation velocities of GaN and SiC are almost double for Si, representing that they can operate at higher switching frequencies.

The critical parameters for assessing the performances for various purposes are the Figure of Merits (FOMs) for power devices, which mainly depend on the inherent material properties. The major FOMs of the semiconductor materials are presented in Table 2-1[9], [10]. Some of the critical indexes are introduced below. Baliga's Figure of Merit(BFOM), which is used to assess the conduction loss of power devices, is the product of on-state resistance and breakdown

voltage[11], [12]. The relative dielectric constant, electron mobility and critical electric field of the materials all affect this index. The product of the electric critical field and charge carrier saturation velocity is known as Johnson's figure of merit (JFOM).

Moreover, it is employed to calculate the maximum breakdown voltage and cut-off frequency. Baliga's high-frequency Figure of Merit, or BHFOM, assesses the switching loss of power field-effect transistors (FETs). KFOM is Keyes' FOM, which takes into consideration the thermal constraints on transistors' switching capabilities. Furthermore, several new FOMs are proposed to evaluate the power semiconductor devices by Alex Huang[13]. Huang's material figure of merit (HMFOM) is defined as the product of the critical electric field and carrier mobility, which is inversely proportional to the minimum total power loss. It takes into account both the switching losses and conduction losses[13]. Huang's device chip area figure-of-merit (HCAFOM) is inversely proportional to the optimal chip area. Higher HCAFOM represents the lower chip area[13]. Huang's thermal figure of merit (HTFOM) is used to evaluate the power devices' junction temperature rise under the given chip area and power losses[13].

GaN performs significantly better on BFOM, BHFOM, and JFOM than Si and SiC due to its excellent electrical material properties, which were previously described. However, the slight improvement in the KFOM of GaN indicates

that the thermal performances of GaN-based power devices have no apparent advantages over Si devices. According to HMFOM and HCAFOM, GaN is eight times lower on power loss than Si and 61.7 times smaller chip area than Si. The minimum HTFOM of GaN indicates that it has a higher junction temperature rise for operating similar conditions in these four materials[13]. Moreover, due to these material properties, compared to Si MOSFETs(maximum 125 to 150°C), GaN high-electron-mobility transistors(HEMTs) can be operated at relatively higher temperatures(above 400-500°C) [14]–[16], which is a noteworthy benefit of GaN-based power devices [17].

2.2. Substrates for GaN Power devices

The market for commercial GaN power devices is currently dominated by lateral GaN power semiconductor devices. High-power GaN HEMTs operate at high voltages and simultaneously offer low on-state resistances.

The epitaxial crystal quality and the process significantly depend on the difference in the thermal expansion coefficients between the epitaxial layer and substrates. The increased dislocation density caused by the lattice mismatch between substrates and the GaN epitaxy layer possibly leads to a more significant leakage current under a high electric field [17]. It is detrimental to the static and dynamic electrical performances and the reliability of GaN power devices. GaN power devices can also function at high frequencies and temperatures because of the wide bandgap. As a result, GaN power device applications involving high voltage and high temperature also depend critically on the thermal constraints of the substrate [17].

GaN substrates have low thermal conductivity and no lattice mismatch, indicating low defect densities. The commercial market does not, however, favour expensive GaN materials. GaN heterostructures are subsequently produced epitaxially on foreign substrates [18]. The main substrates for GaN power semiconductor devices include sapphire, SiC, and silicon. According to the report[19], the first GaN transistors were grown on (0001) SiC and c-plane sapphire. Furthermore, due to the low costs of Si substrates, GaN-on-Si power

Table 2-3 properties of different Substrates for GaN power devices[7]

Property	Sapphire	SiC	Si	GaN
Lattice mismatch (%)	16	3.1	-17	0
Linear thermal expansion coefficient ($\times \mathbf{10^{-6} K^{-1}}$)	7.5	4.4	2.6	5.6
Thermal conductivity (W $\mathbf{cm^{-1} K^{-1}}$	0.25	4.9	1.6	2.3
Cost	cheap	expensive	Cheap	Very Expensive
Dislocation density of GaN films grown on substrate(optimized) ($\mathbf{cm^{-2}}$)	Low 10^8	Low 10^8	Low 10^8	$10^4 - 10^6$

devices are becoming the leading choice for commercial GaN power devices. In Table 2-3 [7], the crucial characteristics of the various substrates, such as the dislocation density of GaN films produced on the substrate, thermal conductivity, lattice mismatch, and lattice thermal expansion coefficient are shown.

Threading dislocation density and significant lattice mismatch produce crystal defects, increasing the leakage current and trap states [17]. The dislocation densities of GaN films produced on Si, SiC, and sapphire substrates are about

10^8, which is two orders of magnitude higher than GaN. Additionally, lattice mismatch for the epitaxially formed GaN layer (0001) on the c-plane sapphire and silicon substrate (111) is extremely high, at 16 and -17 percent, respectively. SiC substrates have the lowest lattice mismatch, with a value of just 3.1%.

The linear thermal expansion coefficient is another critical parameter for evaluating the epitaxial process's substrate effects. GaN layers differ significantly from Si or Sapphire substrates in terms of thermal expansion coefficient [20]–[22]. After the temperature dropped to room temperature, cracks began to occur in the GaN epitaxial layer on the substrate, notably for the thick GaN epitaxial films. It may also cause the generation of dislocations and defects along the GaN epitaxial layer.

GaN power devices work at rapid speeds and high-power densities, which results in significant heat generation. Heating effects degrade the current density and cause more power losses. As a result, another crucial factor is the thermal conductivity of the substrates. High substrate thermal conductivity helps the devices operate more effectively at high temperatures. SiC shows the highest thermal conductivity among three foreign substrates and becomes the best candidate for GaN power devices concerning thermal management. However, sapphire substrates have recently become more appealing for commercial use, including power integration applications and high-voltage

GaN power devices. The first GaN-on-sapphire power Integrated (IC) die was commercially available from Power Integrations in 2019 [23].

Moreover, Transphorm Inc. presented the first commercial 1200V GaN-on-sapphire power transistor with 99% efficiency power switching at ISPSD in 2022[24]. Even though the SiC substrate has a low lattice mismatch and good thermal conductivity, enabling it to be an ideal substrate for GaN high-power devices, the commercial market does not favour SiC due to its high cost. However, the sapphire substrate has lower manufacturing cost and is less influenced by temperature in manufacturing. These advantages make it one of the most competitive candidates for GaN power devices[24].

Although Transphorm Inc. has proved that GaN-on-sapphire shows good electrical performances and will be commercially available[25], the sapphire substrate is facing challenges. Low thermal conductivity and high lattice mismatch of sapphire substrates still need to be solved[24].

2.3. Polarisation Effects

III-V compound semiconductor materials have wide applications in power, optoelectronic and RF-related semiconductor devices. The crystal formations of wurtzite, zinc blende and rock salt make up the three most prevalent III-V semiconductor materials. Furthermore, the wurtzite structure is the major crystal structure of the III-N(Nitride) semiconductors, including GaN, AlN, and InN [26]. The hexagonal close-packed (HCP) structure of wurtzite is depicted in the axial direction along the c-axis [0001] with the Ga- or N-face at the crystal's surface, respectively, as Figure 2.1 shows[7].

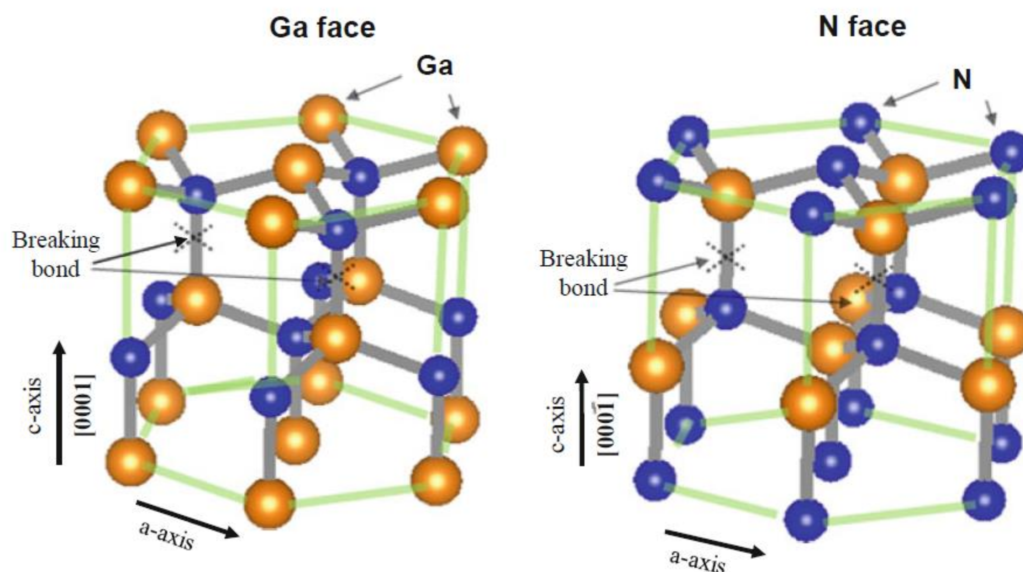


Figure 2.1 Wurtzite-type Hexagonal GaN crystal structure with Ga- or N-face at the surface of the crystal[7].

The chemical bond between Gallium and Nitride is ionic because the electronegativity of Ga and N atoms differs from one another. It demonstrates the reversed direction along the c-axis in the wurtzite structure with Ga- and N-face at the crystal surface, resulting in the various electrical properties in

GaN-based devices with Ga- and N-face. In III-nitrides semiconductors, there are two polarisation effects: spontaneous polarisation and piezoelectric polarisation [27].

2.3.1. Spontaneous Polarisation

Due to the difference in electronegativity between Ga and N atoms, polarisation results in a dipole leading to the spontaneous polarisation that occurred in the crystal structure of wurtzite GaN[27]–[29]. When an atom creates chemical bonds with other atoms, its ability to attract the shared electrons is known as electronegativity. In the GaN semiconductors, the electronegativity of nitrogen is higher than that of gallium. N atoms attract the shared electrons and show cationic (-) characteristics. Conversely, Ga atoms

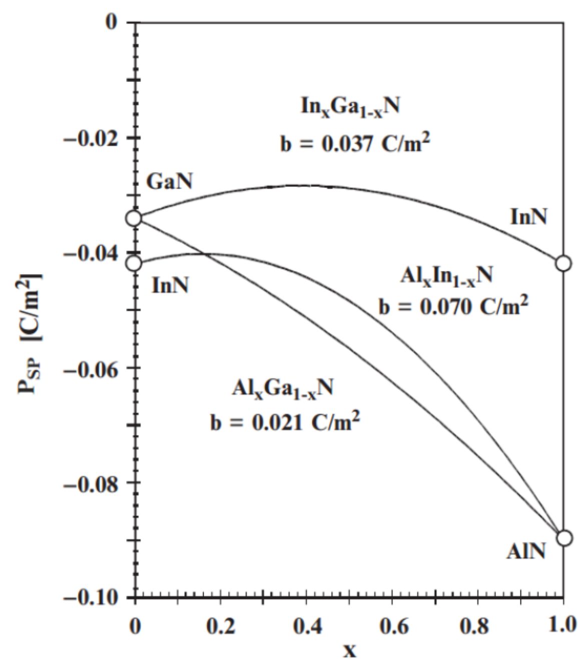


Figure 2.2 Spontaneous polarisation (Psp) coefficient in $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ as a function of Al mole fraction(x) [32].

show anionic characteristics. Therefore, electrical polarisation exists at a dipole across the chemical bonds [30]. GaN wurtzite crystal structure is not centro-symmetrical along the c-axis[31]. Thus, the polarisation at the dipoles from different orientations is neutralised inside the GaN material. However, the asymmetry of polarisation happens at the surface of GaN material, causing the net macroscopic polarisation, referred to as spontaneous polarisation (P_{sp}).

Therefore, based on the prior explanation, the orientation of P_{sp} in the crystal structure of wurtzite GaN is parallel to the c-axis. GaN, AlN, and InN each have spontaneous polarisation coefficients of 0.029, 0.081, and 0.032 C/m^2, respectively.

The expression of the spontaneous polarisation for $Al_xGa_{1-x}N$, which mostly depends on the mole fraction of Al(x), is [32][33]:

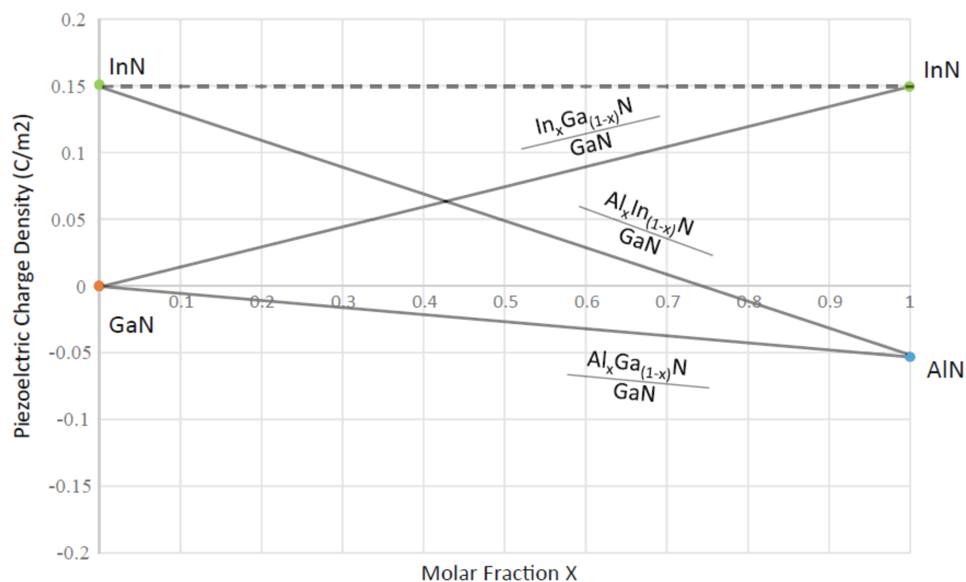


Figure 2.3 Theoretical calculation results of the piezoelectric polarisation charge density as a function mole fraction of Al or In in $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $Al_xIn_{1-x}N$[7].

$$P_{sp}(Al_xGa_{1-x}N) = -0.09x - 0.034(1-x) + 0.021x(1-x)\ C/m^2 \qquad (2.1)$$

Similar to this, Al mole fraction(x) and P_{sp} in AlxGa1-xN, InxGa1-xN, and AlxIn1-xN are also provided in Figure 2.2[32][33].

2.3.2. Piezoelectric Polarisation

The mechanical stress or strain results in the polarisation effects and lattice mismatch because of the various lattice constants between different semiconductors. Thus the electric polarisation is named piezoelectric polarisation (P_{PZ}). The mechanisms of piezoelectric polarisation are explained in Figure 2.4 [32].

As a result of a symmetrical tetrahedral crystal structure, the internal polarisation vectors (P_1+P_2+P_3+P_4) between Ga and N atoms are equal to zero. However, due to the lattice mismatch, the tensile stress is generated in the

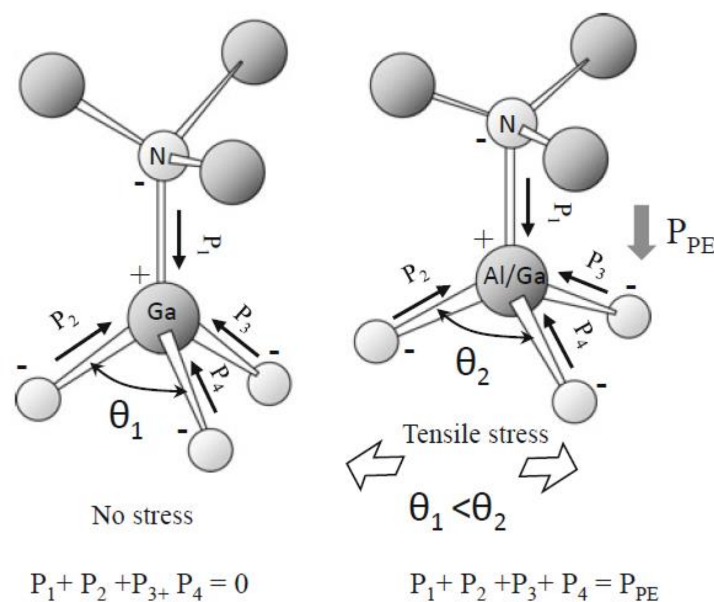


Figure 2.4 The polarisation field exists in the ionic bonds of the GaN tetrahedron structure with (right) and without (left) the mechanical stress[7].

tetrahedral crystal structure of GaN. Therefore, as Figure 2.4 shows, when tensile stress is applied, angle 2 widens more than angle 1, resulting in a net polarisation field and an unbalanced polarisation electric field equivalent to P_{PZ} ($P_1+P_2+P_3+P_4= P_{PE}$) along [000-1]. On the contrary, in the case of N polarity, a similar net polarisation exists in the GaN tetrahedron, but the direction is reversed [0001] [7]. Figure 2.3 demonstrates the charge density caused by the piezoelectric polarisation of $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$, and $Al_xIn_{1-x}N$ as a function of the mole fraction x [7].

In contrast, when a compressive strain is applied, angle 2 shrinks to a smaller value than angle 1, creating net polarisation in the [0001] direction for Ga polarisation and the [000-1] direction for N polarisation. [34].

F.Bernardini [10] reported that the expression of piezoelectric polarisation P_{PZ} is:

$$P_{PZ} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad (2.2)$$

The material's lattice constants are represented by a and a_0 , while the piezoelectric constants along the (x,y) and (z) directions are represented by e_{31} and e_{33}. The elastic constants are denoted by C_{13} and C_{33}. The piezoelectric polarisation constants of the GaN, InN and AlN binary semiconductor devices are displayed in Figure 2.5 [10][35].

However, for AlxGa1-xN, InxGa1-xN, and AlxIn1-xN, the lattice constant varies with the mole fraction (x) of metal (Al or In). From Figure 2.5, the relationship between the lattice constant and the mole fraction of Al or In is linear [9]. As a result, the piezoelectric polarisation follows equation (2) and is inversely proportional to the mole fraction of Al or In. The piezoelectric polarisation charge density in AlxGa1-xN, InxGa1-xN, and AlxIn1-xN is calculated as a function of the mole fraction of Al or In, assuming that they are all grown on a relaxed GaN layer[19][31]. The piezoelectric polarisation charge density for $Al_xGa_{1-x}N$/GaN exhibits a declining linear trend as the mole fraction of Al and In rises [7].

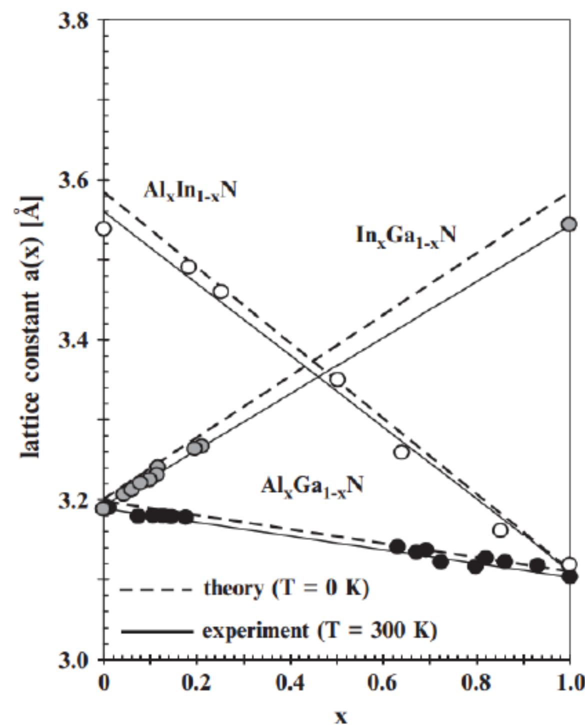


Figure 2.5 the theoretical and experimental lattice constant of $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ at T=0K and 300K, respectively[9].

2.4. AlGaN/GaN heterostructures and the formation of 2DEG

2.4.1. Polarisation charge

Following the previous discussions, it is clear that spontaneous and piezoelectric polarisation exists in III-V nitride heterostructures semiconductors. Ga- and N-face spontaneous and piezoelectric polarisation under various stress conditions are described in AlGaN/GaN heterostructures [31].

According to Figure 2.6, in AlGaN/GaN heterostructures with Ga face, the spontaneous polarisation in AlGaN and GaN layers is negative, indicating that

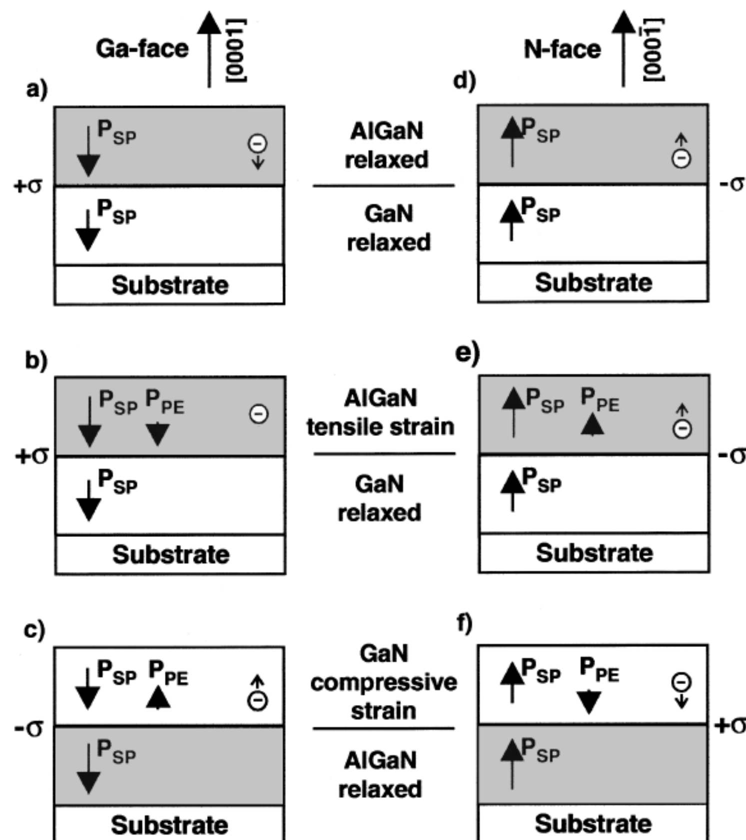


Figure 2.6 Spontaneous and piezoelectric polarisation with Ga-face and N-face induced sheet charge density under different conditions [35].

the polarisation vectors point toward the substrate [35]. In contrast, the spontaneous polarisation vectors in AlGaN and GaN layers have the opposite direction in N-face AlGaN/GaN heterostructures. It relies on the stress conditions, following the preceding concept of piezoelectric polarisation. When there is no stress between the AlGaN and GaN layer, there is no piezoelectric polarisation in the AlGaN/GaN heterostructures. When the tensile strain is delivered from the AlGaN layer to the relaxed GaN layer in the case of a Ga-face, piezoelectric polarisation is created in the AlGaN layer.

Moreover, piezoelectric polarisation is parallel to spontaneous polarisation. On the other hand, when compressive-strained GaN is formed on the relaxed AlGaN layer, the antiparallel piezoelectric polarisation is detected in the AlGaN layer. However, piezoelectric and spontaneous polarisation have opposite directions if it switches from the Ga face to the N face.

The gradient of polarisation induces the sheet charge density (σ) because it generates net polarisation between the AlGaN and GaN layers (ΔP). The following equation reported by O.Ambacher et al. [35]can express this relationship :

$$\sigma = \Delta P \tag{2.3}$$

$$\sigma = P(top) - P(bottom) \tag{2.4}$$

$$= \left[P_{sp}(top) + P_{PE}(top)\right] - \left[P_{sp}(bottom) + P_{PE}(bottom)\right]$$

P_{sp} and P_{PE} denote spontaneous polarisation and piezoelectric polarisation, respectively.

In the AlGaN/GaN heterostructures, Equation (2.4) can be expressed by:

$$\sigma = P(AlGaN) - P(GaN) \quad (2.5)$$
$$= [P_{sp}(AlGaN) + P_{PE}(AlGaN)] - [P_{sp}(GaN)]$$

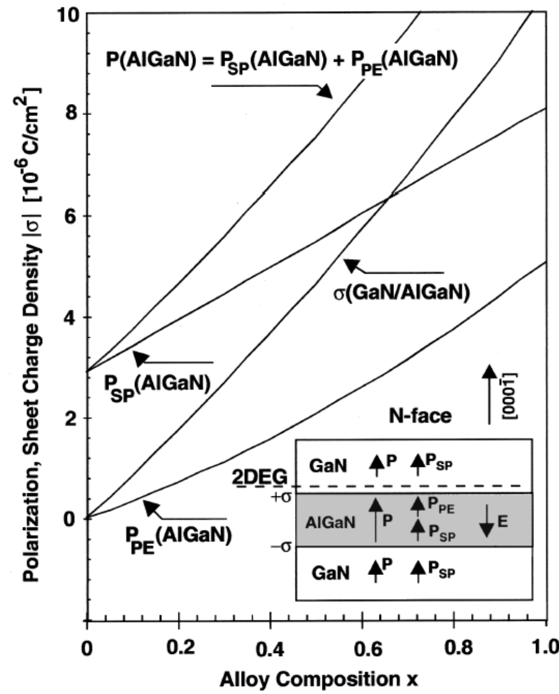
According to equation (2.5), the sheet polarisation charge density (σ) is positive at the heterointerface. The free electrons are accumulated to balance the polarisation charge density. On the other hand, positive holes can be induced to achieve charge neutrality by the negative polarisation charge.

The calculation method can also be applied to double heterostructures GaN/AlGaN/GaN. The calculated sheet charge density as a function of the Al mole fraction in the N-face and Ga-face GaN/AlGaN/GaN heterostructures are depicted in Figure 2.7(a) and (b), respectively. The expression of the total polarisation sheet charge density for N-face GaN/ $Al_xGa_{1-x}N$/GaN heterostructures as a function of Al-content is [31]:

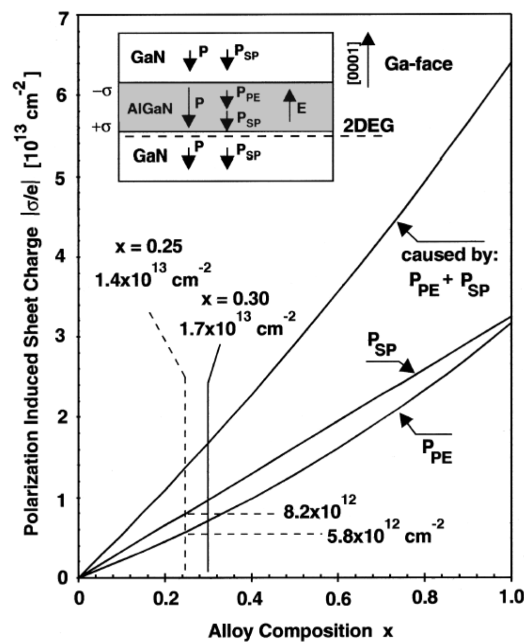
$$|\sigma(x)| = \left|[P_{sp}(AlGaN) + P_{PE}(AlGaN)] - [P_{sp}(GaN)]\right|$$

$$|\sigma(x)| = \left|2\frac{a(0) - a(x)}{a(x)}\left\{e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right\} + P_{SP}(x) - P_{SP}(0)\right| \quad (2.12)$$

For the Ga-face GaN/$Al_xGa_{1-x}N$/GaN, the spontaneous polarisation, piezoelectric polarisation, and total polarisation-induced sheet charge density are displayed as a function of Al-content(x) in Figure 2.7 (b) [31]. The calculated polarisation sheet charge density as a function of Al mole fraction in $Al_xGa_{1-x}N$/GaN, $In_xGa_{1-x}N$/GaN and $Al_xIn_{1-x}N$/GaN heterostructures are shown in Figure 2.8.



(a)



(b)

Figure 2.7 (a)The spontaneous, piezoelectric and total polarisation sheet charge density as a function of Al-content in the N-face GaN/ AlxGa1-xN/GaN heterostructures(b)the polarisation induced sheet charge density[31].

Moreover, the maximum sheet carrier concentration is expressed as a function

of Al content [36]:

$$n_s(x) = \frac{+\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon_x}{de^2}\right)[e\phi_b(x) + E_F(x) - \Delta E_C(x)] \qquad (2.13)$$

Where e is the electronic charge and d is the barrier thickness of $Al_xGa_{1-x}N$.

Furthermore, $e\phi_b$ stands for the Schottky barrier of the Schottky gate contact.

The Fermi level and the conduction band offset are denoted by E_F and ΔE_C, respectively.

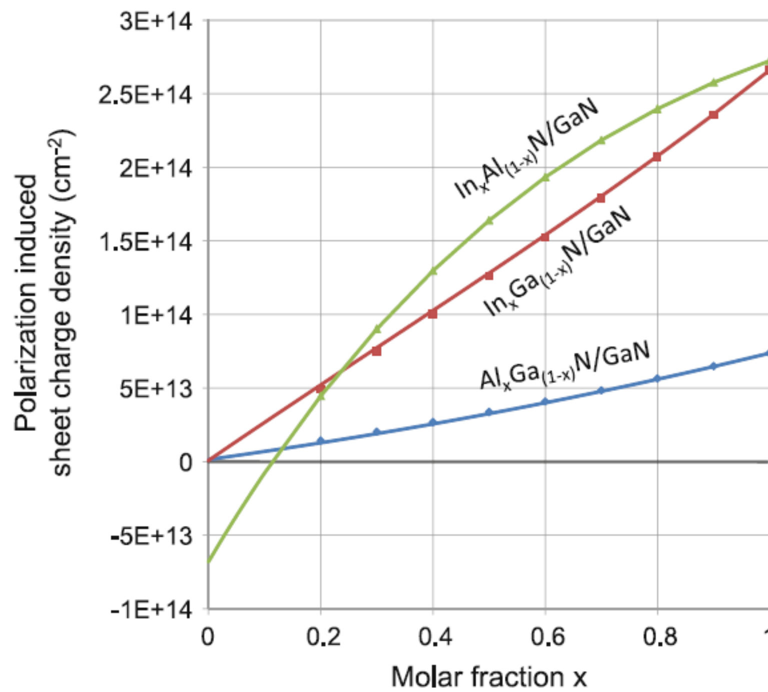


Figure 2.8 Theoretical calculation results of the polarisation induced sheet charge density as a function of Al or In molar fraction(x) in $Al_xGa_{1-x}N/GaN$, $In_xGa_{1-x}N/GaN$ and $Al_xIn_{1-x}N/GaN$ heterostructures[36].

2.4.2. Origin of 2DEG

M.Asif Khan et al. initially discovered that undoped $Al_{0.13}Ga_{0.87}N$/GaN heterostructures contain two-dimensional electron gas (2DEG) with a sheet density of 2.6×10^{-12} cm^{-2} at 7 k [37]. Moreover,2DEG mobility was 834 cm^2/Vs at room temperature [37]. With decrease in temperature, 2DEG mobility monotonically increased and gradually saturated at 2626 cm^2/Vs at 77K [37].

At present, the surface-donor model is widely accepted as the main theory of the origin of 2DEG. J.P.Ibbetson et al. [38] formulated and then experimentally supported the theory of the origin of 2DEG in AlGaN/GaN HFETs. According to electrostatics theory, the surface states are relevant to the source of 2DEG. Figure 2.9 shows the AlGaN/GaN conduction band diagram with different space charge components:(1) negative charge due to 2DEG(n_s);(2) polarisation-induced charges located at the AlGaN/GaN hetero-interface(σ_{PZ});(3)the

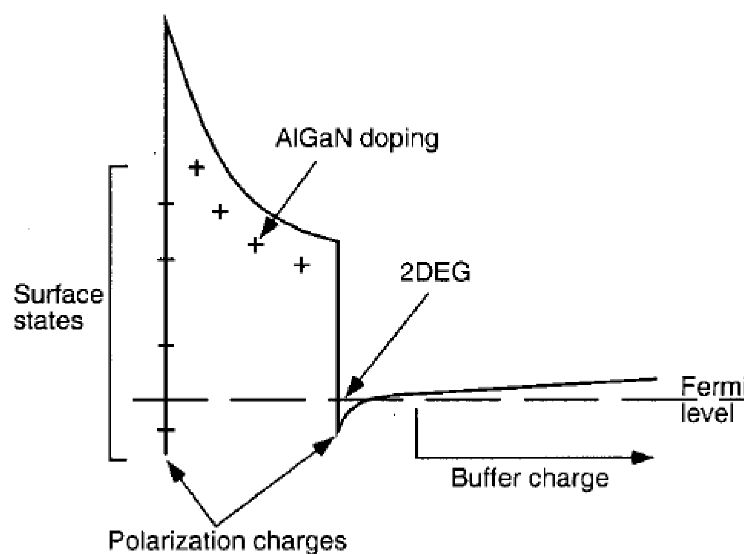


Figure 2.9 conduction band diagram of AlGaN/GaN HFET with different space charge components [38].

ionised-donors induced sheet charge in the AlGaN(σ_{AlGaN});(4)the ionised-surface-states induced charge($\sigma_{surface}$); and,(5)buffer charge(σ_{buffer}).According to the theory of the polarization, the total polarization-induce charges composed by the a dipole contributes zero to the total space charge in the AlGaN/GaN heterostructures. Moreover, the magnitude of the buffer charge is assumed as low as possible in the well-designed FETs and can be neglected. Therefore, the space charges should follow the charge neutral principles, indicating that the 2DEG sheet density is equal to the sum of the $\sigma_{surface}$ and $\sigma_{AlGaN.}$ In the undoped AlGaN/GaN heterostructures, σ_{AlGaN} is zero, representing that sheet density of the 2DEG is dominated by the surface states. The idea argues that the ionised

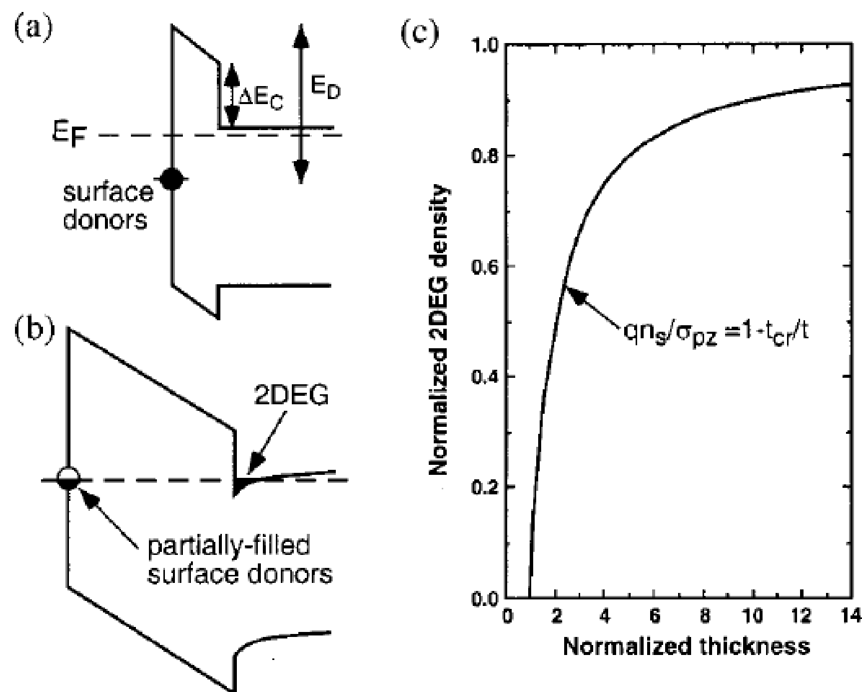


Figure 2.10 schematic band diagram of the surface-donor model under different AlGaN thicknesses:(a)less than(b)more than the critical thickness. (C)The theoretical relationship between 2DEG density and AlGaN barrier thickness is based on the surface donor model[38].

donor or acceptor-like surface states have a significant influence on the 2DEG sheet density. This is called the surface-donor model.

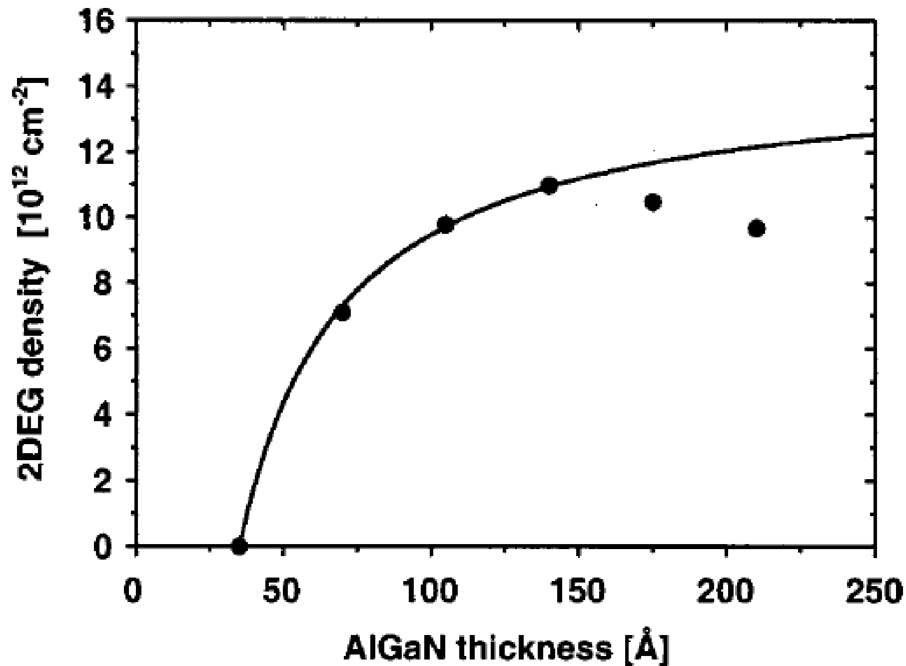
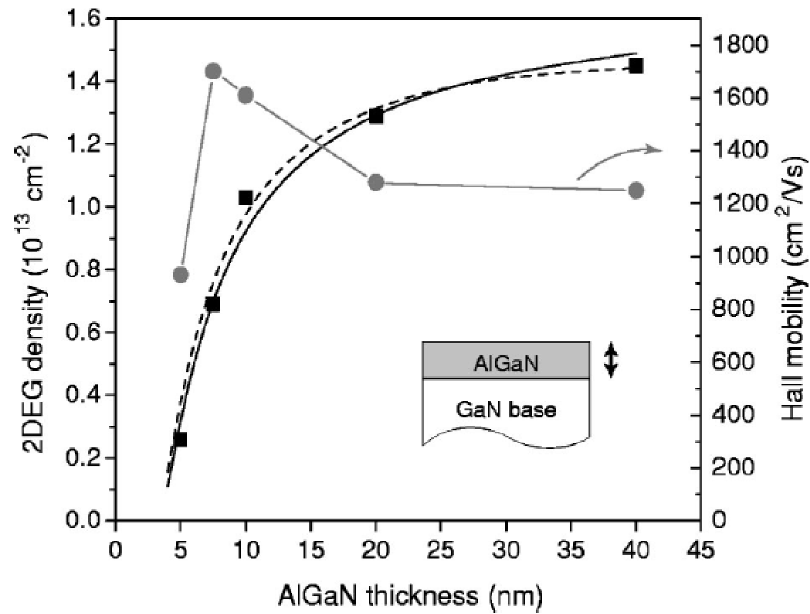


Figure 2.11 shows the measured and calculated 2DEG sheet density as a function of $Al_{0.34}Ga_{0.64}N$ barrier thickness at room temperature [39].

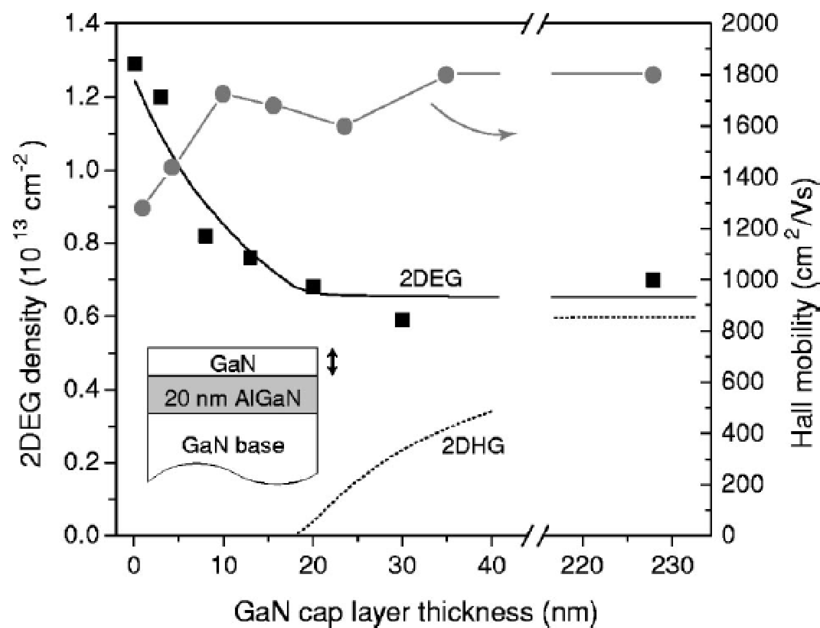
Figure 2.10 demonstrates the relationship between the AlGaN barrier thickness and 2DEG sheet density [38]. Based on the surface donor model, electrons cannot transfer to the AlGaN/GaN interface when the surface donor energy is below the Fermi level, and the AlGaN barrier thickness is below the critical thickness. However, once it reaches the critical thickness, the surface donor energy hits the Fermi level, allowing electrons to move from the filled surface states to the AlGaN/GaN interface as illustrated in Figure 2.10 (b) [38].

Figure 2.11 demonstrates the relationship between 2DEG density and AlGaN thickness, including measured and calculated results [39]. When the AlGaN

thickness goes above the critical thickness, it is possible to see that 2DEG density increases (around 3nm) and then gradually saturates. This trend is



(a)



(b)

Figure 2.12 The relationship between 2DEG and 2DHG sheet density and carrier mobility as a function of GaN cap layer thickness in GaN/AlGaN/GaN double heterostructures [33].

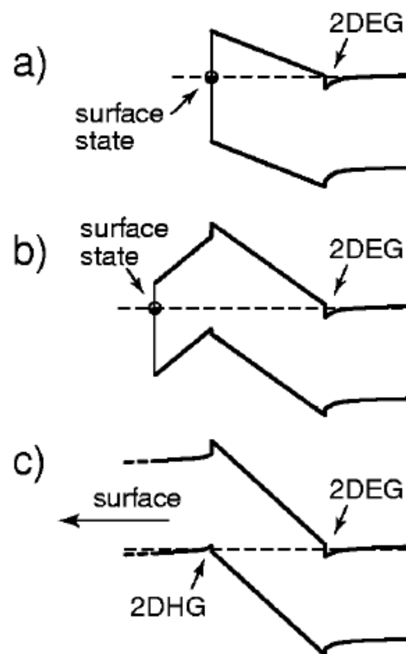


Figure 2.13 schematic band diagram of (a) AlGaN/GaN heterostructures; GaN/AlGaN/GaN double heterostructures with a(b) thin GaN cap layer(C) thick GaN cap layer [39].

consistent with the outcome obtained based on the theory of the surface-donor model. However, other models, such as surface-pinning model, can also explain the data shown in Figure 2.11.And other questions in the surface donor model, for example, whether the surface donors are intrinsic or impurity-related, are still unknown. Therefore, although the surface-donor model is controversial and debatable, it is the widely accepted theory of the origin of 2DEG.

Heikman et al. also reported similar research findings, which also supported the theory of the surface donor model [39]. The 2DEG density and hall mobility is also provided as a function of AlGaN thickness in Figure 2.12(a) [39].

Moreover, GaN cap layer thickness impacts sheet density and hall mobility are also documented in Figure 2.12 (b) in GaN/AlGaN/GaN double heterostructures. As the thickness of the GaN cap layer increases, the density of the 2DEG density decreases, going from about 1.3×10^{13} cm^{-2} with no cap layer to 0.7×10^{13} cm^{-2} with a 20nm GaN cap layer. The 2DEG sheet density reaches saturation at a thickness greater than 20nm. However, no 2DHG is seen when the GaN cap layer thickness is less than 17nm, and 2DHG density increases when the thickness is more than 17nm. The carrier hall mobility slightly decreases with the rise of the 2DEG sheet density. The reduction in mobility is caused by the increased coulomb scattering.

Figure 2.13 explains the reasons based on the surface donor model. In AlGaN/GaN heterostructures, donor states at the surface hold the Fermi level

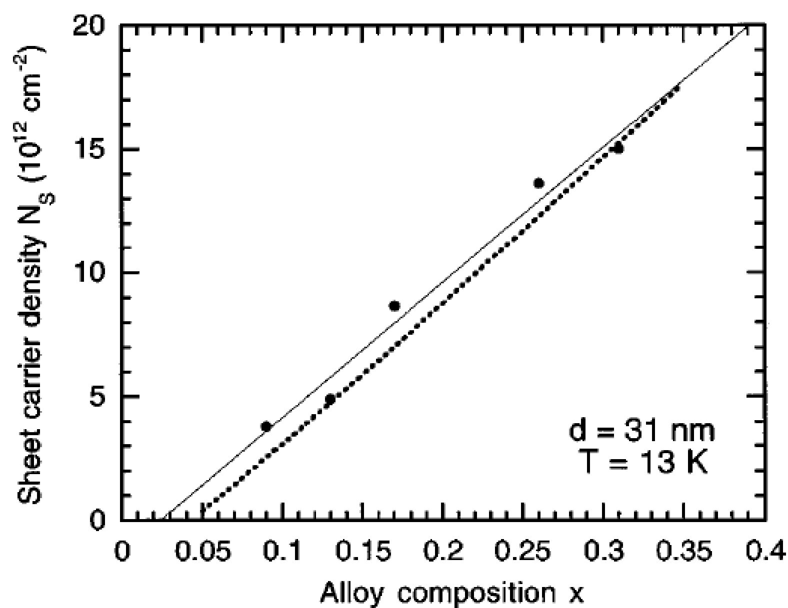


Figure 2.14 2DEG sheet density as a function of Al composition of AlGaN in AlGaN/GaN heterostructures [40].

in place. When a GaN cap layer is grown on top of AlGaN/GaN heterostructures, negative polarisation charges are generated at the hetero-interface, raising the electric fields in the AlGaN layer and lowering the 2DEG density. As the GaN cap layer gets thicker, the valence band level rises. Until the thickness exceeds the critical thickness and the valence band energy reaches the Fermi level, 2DHG is formed at the GaN cap layer/AlGaN interface.

In addition, the 2DEG sheet density is also varied with the Al content of AlGaN and the relationship is reported in [40]. Figure 2.14 illustrates the linear relationship between 2DEG sheet densities and Al composition.

2.5. Conventional AlGaN/GaN High Electron Mobility Transistor (HEMT)

Heterostructures based field-effect transistors were first invented through the MBE-grown doped GaAs/n-AlGaAs in 1980 [41]. Conventional AlGaAs/GaAs HEMTs are grown on the GaAs substrate. Additionally, it contains the n-type doped AlGaAs layer as well as the undoped AlGaAs space layer and GaAs layer. 2DEG is constrained at the AlGaAs/GaAs heterointerface. The n-doping concentration and the electronic states at the AlGaAs/GaAs interface potential have the most remarkable effects on the 2DEG concentration(roughly 1.0×10^{12} cm^{-3})[42].

Conventional AlGaN/GaN HEMTs were firstly invented in 1993[43], [44]. Compared with the AlGaAs/GaAs HFETs, conventional AlGaN/GaN HEMTs have a simplified structure but have similar electrical characteristics. The diagram below depicts the schematic cross-section of the conventional AlGaN/GaN HEMTs in Figure 2.15 [45].

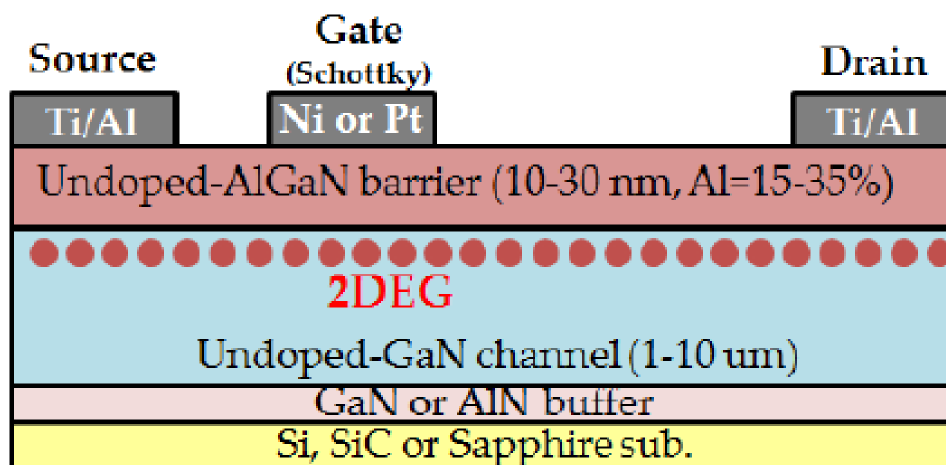


Figure 2.15 The schematic cross-section of conventional AlGaN/GaN HEMTs [45].

AlGaN/GaN HEMTs frequently use Si, SiC, or sapphire substrates. Above the substrate, a buffer layer made of GaN or AlN, an undoped GaN layer, and a barrier layer made of undoped AlGaN are all consecutively grown. On the AlGaN layer, there are three electrodes: the gate (G) contact forms the Schottky contact, while the source (S) and drain (D) contacts are Ohmic to the 2DEG.

Due to the high mobility and high density of 2DEG, AlGaN/GaN HEMTs have low conduction and switching losses, making them one of the most appealing alternatives for power electronic applications.

2.5.1. The operation principle of conventional AlGaN/GaN HEMTs

Conventional AlGaN/GaN HEMTs are lateral devices. 2DEG channel forms the conduction path when no gate biases are applied, representing that they are the normally-on devices. Therefore, the expression of V_{th} in the conventional AlGaN/GaN HEMTs is [34]:

$$V_{th} = \phi_b - \frac{\Delta E_c}{e} - V_p - \frac{ed}{\varepsilon}(\sigma + N_B W_d) \qquad (2.15)$$

Where ϕ_b is the Schottky barrier height of the gate,ΔE_c denotes the conduction band offset, d is the total thickness of the AlGaN barrier layer, and σ denotes the interfacial polarisation charge. N_B and W_d denote the doping density in the bulk and depletion width in the channel, respectively. $V_p = qN_d {d_d}^2/2\varepsilon$, where N_d is the AlGaN barrier layer's donor concentration, and d_d is the doped thickness of the barrier layer. ε is the dielectric constant of the AlGaN barrier layer. Based on equation (2.15), the AlGaN barrier layer thickness, Al content

and the barrier height of the Schottky gate are varied to alter the 2DEG sheet density, which primarily determines the threshold voltage.

Figure 2.16 depicts the conduction band diagram of AlGaN/GaN HEMTs under different gate voltages [46]. Under the positive gate bias, the 2DEG channel is not depleted. When it becomes negative but higher than the threshold voltage, the conduction band are lifted, causing the reduction of 2DEG sheet density. However, when the gate voltage is lower than the threshold voltage, no quantum well can store 2DEG at the AlGaN/GaN interface when the conduction band is above the Fermi level.

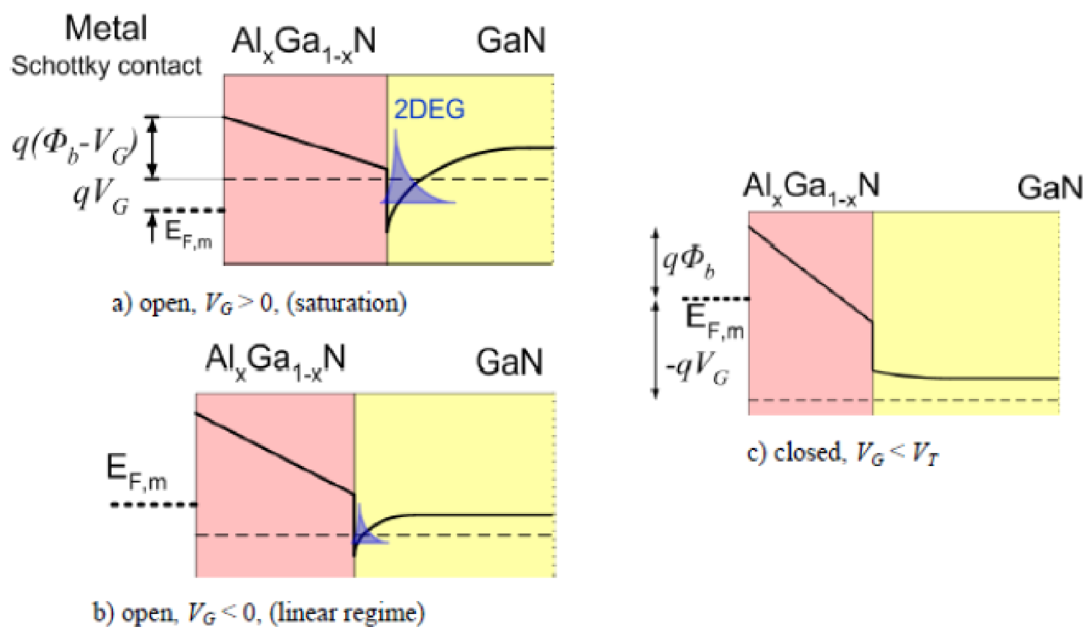


Figure 2.16 conduction band diagram under different gate voltage(a)V_g is positive (b)0<Vg<V_{Th} (C) Vg>V_{Th} [46].

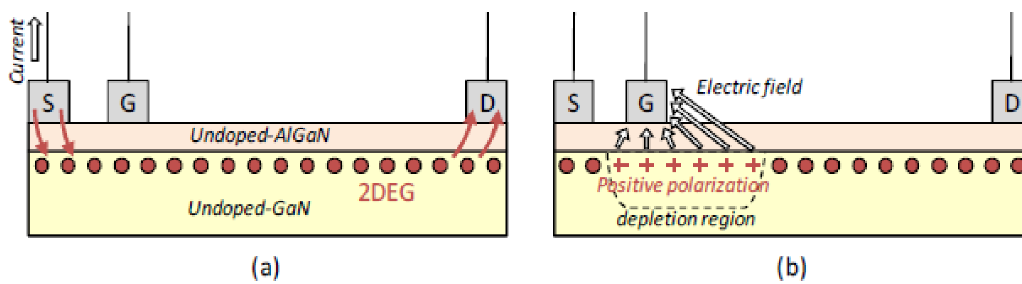


Figure 2.17 Schematic of a conventional HFET in (a) the ON-state and (b) the off-state[47].

Figure 2.17 explains the on-state and off-state operating principles of an AlGaN/GaN HEMT. Electrons flow through the 2DEG channel when the gate voltage rises beyond the threshold voltage. However, the 2DEG channel is depleted under the Gate region, disrupting the conduction path. Figure 2.17 (b) depicts the high electric field between positive polarisation charges in the depletion area and the gate electrode with negative biases causing the electric field to be crowded near the drain-side edge of the gate [47]. The electric breakdown of conventional AlGaN/GaN HEMTs occurs due to the high electric field peak exceeding the critical electric field. Therefore, enhancing the breakdown voltage is their main challenge for high-power applications.

2.5.2. Introduction of field-plate technology

Several Field plate (FP) technologies are studied by W.saito et al. [48] for optimising the electric field management in AlGaN/GaN HEMTs to improve the inhomogeneous electric field distribution of the AlGaN/GaN HEMTs in the off-state. Single Field plate design (FP) was analysed in [48]. Several research also reports similar results of FP technology [49]–[53]. Figure 2.18 depicts the electric field distribution along the 2DEG channel with and without a single FP. The drain-side edge of the gate has a crowded electric field without using single FP technology, causing an extremely high electric field peak and low breakdown voltage (BV=100V). However, the highest electric field peak is

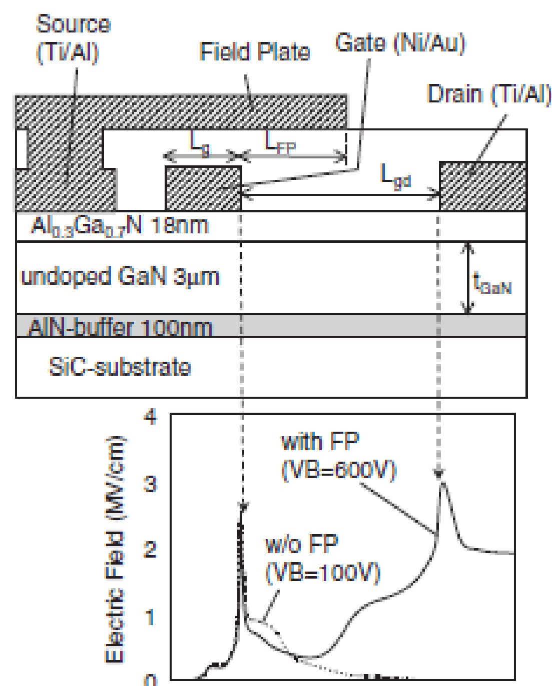


Figure 2.18 Cross-sectional structures of fabricated AlGaN/GaN HEMT with field plate structure (FP-HEMT) and electric field distribution along with the AlGaN/GaN interface layer with field plate (solid line) and without field plate (broken line)[54].

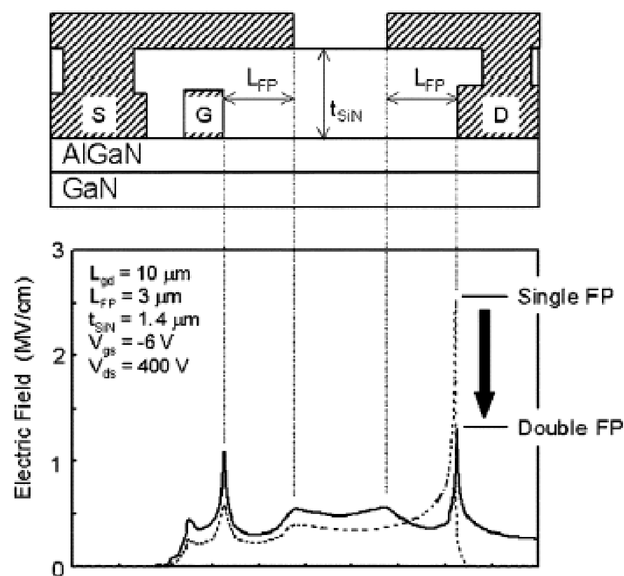


Figure 2.19 Comparison of electric field profile between single and double FP technology during off-state[54].

suppressed and shifted from gate to drain through FP design. Thus it optimises the electric field profile and enhances the BV from 100V to 600V. The single FP technique can increase not only breakdown voltage but also decrease gate leakage and hot electron generation[48]. Although the electric field peak of AlGaN/GaN HEMTs is somewhat flattened by the single FP design, the presence of these two peaks in the electric field profile suggests that the electric field distribution may be further optimised. Therefore, the double Field plate design was discussed in detail [54], which is thought to be a significant improvement in the breakdown voltage compared with the single FP design. Compared with the single FP technology, a drain field plate was added in the double FP design to suppress the high electric field peak at the drain, which is where the electric breakdown occurs in the single FP design GaN HEMTs.

Figure 2.19 presents the AlGaN/GaN HEMT cross-section with single and double FP technologies and also depicts the electric field distribution at V_{ds}=400V and V_{gs}=-6V. The electric field peak at the drain is successfully controlled once the drain field plate is introduced.

Figure 2.20 displays how the double FP method improves the breakdown voltage of the AlGaN/GaN HEMTs. Although the electric field profile of the Double FP design GaN HEMTs is far better, it is not the perfect box-shape distribution, indicating that the double FP technology is not ideal for enhancing the breakdown voltage. Meanwhile, the fabrication process becomes more complicated when increases the number of field plates in AlGaN/GaN HEMTs. Moreover, the single FP, multiple FP, and slant FP technologies are also suggested to lower the electric field peak and improve the electric field

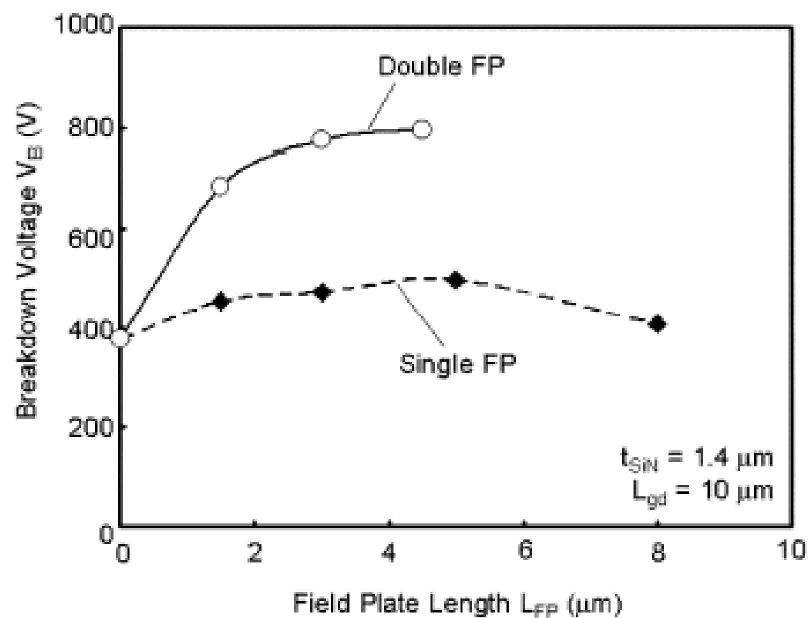


Figure 2.20 The breakdown voltage of AlGaN/GaN HEMTs with single and double FP technology as a function of field plate length[54].

distribution at the off state, respectively, in [51], [52], [55]. Although the recently published FP designs are very effective at enhancing the breakdown voltage of AlGaN/GaN HEMTs, precisely controlling the thickness of the dielectric layer, which is crucial for lowering the electric field peak, is highly challenging [56].

2.5.3. Introduction of the RESURF concept

The concept of a reduced surface electric field (RESURF) was initially put forth by Appels and Vaes [57][58] for Silicon power devices. It is one of the most essential methods to optimise the electric field profile for lateral power devices. Figure 2.21 illustrates the lateral PN diode with RESURF technology[57][58]. Compared with conventional PN diode, the p+ region, a thin n-type epitaxial layer and n+ region are grown on a low-doped p-doped substrate.

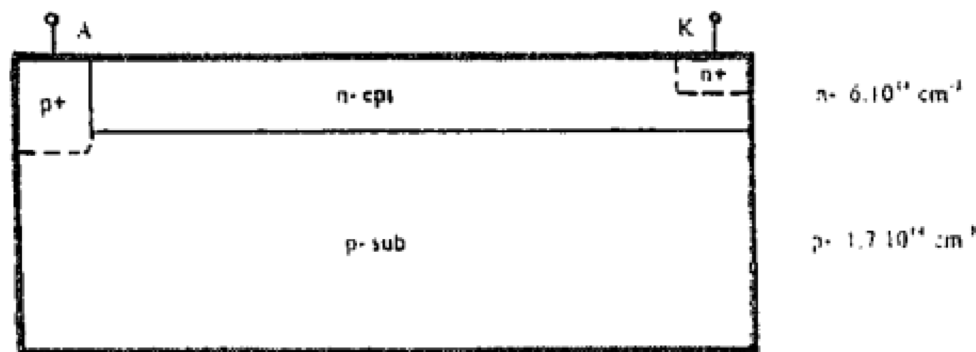


Figure 2.21 The schematic cross-section of the PN diode with RESURF technology [57]

For a conventional diode, the depletion region is generated between the junction of the P+/ N- region. The electric field peak is close to the anode, and a triangle-shaped electric field profile is observed. With the increase in the reversed bias, the depletion region is extended laterally until the lateral surface breakdown happens.

However, due to the vertical n-epitaxial/p-substrate junction, RESURF technology enables the vertical (P-sub/N-epi) and lateral junction (P+/N-epi) to deplete simultaneously. It aims to make the vertical junction reach the critical

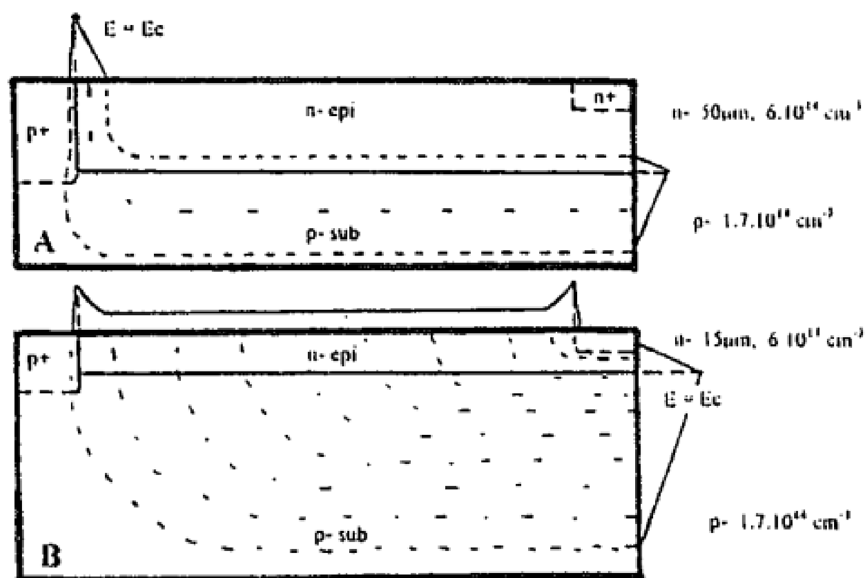


Figure 2.22 Th electric field distribution and potential lines in bulk and at the surface under various t_{epi}:(A) 50um at BV=370-470V;(B)for 15um at BV=1150V [57].

electric field before the lateral junction by precisely controlling the charge density of the n-epi, causing a larger lateral depletion region.

Moreover, it also discussed n-epi thickness influences on the blocking voltage performances of RESURF technology. Figure 2.22(A) shows the diode's electric field and potential distribution with a thicker n- region. Under these circumstances, the lateral junction reaches the critical electric field firstly, which represents the breakdown that firstly occurs at the surface P+/N- junction. However, when the thickness of the n-epi layer reduces from 50um to 15um, the P+/N- junction at the surface will be depleted until the depletion region approaches the N+ region, and the N-/P-substrate vertical junction will reach the critical electric field firstly. A larger lateral depletion region and symmetrical electric field profiles are obtained at the thickness equal to 15um.

It also found that the BV rises from 370-470V to 1150V when the n-epi thickness drops from 50um to 15um.

In conclusion, it was discovered that the N-epi layer's charge density would determine the blocking voltage performance of RESURF technology. To further optimise the high-voltage performances of RESURF power devices, double RESURF [57], [59], [60] and multiple/3D-RESURF technologies[61], [62] are investigated and discussed.

2.5.4. Introduction of Si Superjunction

Superjunction (SJ) technology has been used in Si power devices for many years and is a mature technology. It helps silicon power devices overcome the Si material limit and reach remarkable results based on the charge balance concept in the drift region[62][63]. Compared with the conventional Si power devices, Si super-junction devices are composed of thin, highly doped N-pillar and P-pillar, as shown in Figure 2.23[64]. The Si power MOSFETs [65] and diodes[66] utilising the SJ technology were proposed and discussed.

As Figure 2.23(a) illustrates[64], with a rise in reversed bias, the depletion region of a typical diode extends from the anode to the cathode. The triangular-

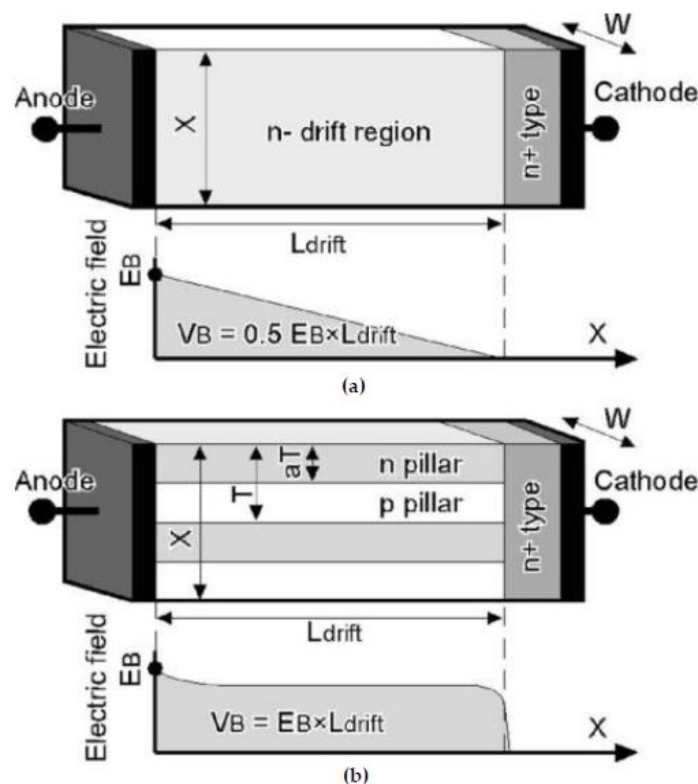


Figure 2.23 Schematic cross-section and electric field profile of (a) Conventional diode (b) SJ diode [64]

shaped electric field is observed, and the peak is at the anode. Therefore, the doping concentration and thickness of the n-drift region are the key determinants of breakdown voltage [64]. Although the BV can be enhanced by reducing the N-doping concentration, the on-state resistance increases.

The specific on-resistance is defined as the resistance per unit area for the drift region[64].As illustrated in Figure 2.23,in the vertical devices, such as power MOSFETs, the area of them is $L_{drift} \times W$.

Similarly, in the unipolar lateral devices, such as GaN HEMTs, the on-resistance R_{on} can be expressed by[64]:

$$R_{on} = \frac{1}{qn\mu_n} \times \frac{L_{drift}}{WX}$$

Where L_{drift} is the length of drift region, n is the carrier density, μ_n is the carrier mobility, W is the width of devices. And the device area A is equal to $L_{drift} \times W$[64].

Therefore, the specific on-resistance can be expressed by:

$$R_{on} \times A = \frac{1}{qn\mu_n} \times \frac{{L_{drift}}^2}{X}$$

And it can obtain the relationship between specific on-resistance and breakdown voltage:

$$R_{on} \times A \propto {V_B}^3$$

However, as Figure 2.23(b) illustrates, SJ diodes enable the depletion region to extend both laterally and vertically. Compared with the conventional diodes with the triangular field distribution, the drift region of the SJ diode exhibits a

flat electric field distribution, shown in Figure 2.23(b). The highly accurate doping control of the n-pillar and p-pillar is required to achieve charge balance conditions and deplete the drift region completely under the low reverse bias. Therefore, the flat and rectangular electric field profile can be observed in Si SJ power diodes under the relatively higher reverse bias.

Compared with conventional power devices, SJ technology can lower the on-state resistance and increase the breakdown voltage [65]. Thus it overcomes the Si material limit [62], [67].

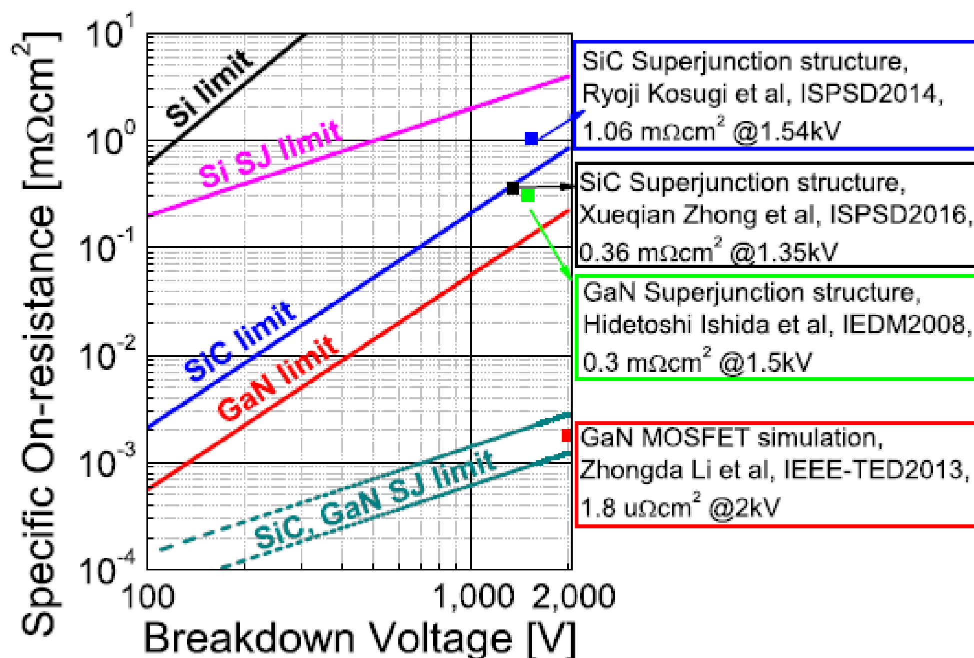


Figure 2.24 The trade-off relationship between specific on-state resistance and breakdown voltage for conventional Si, SiC, GaN and super junction for Si, SiC and GaN[65].

2.6. GaN Polarisation Superjunction technology (PSJ)

Because of doping difficulties, the GaN power devices cannot use the conventional Superjunction technology like the Si and SiC power devices. A. Nakajima et al. proposed Polarisation technology (PSJ), which combines the polarisation and charge balance concepts[64], and successfully realised it in GaN power devices in 2009 at the University of Sheffield.

As Figure 2.25 illustrates, the Polarisation Super-junction (PSJ) HFET includes double heterostructures. Due to the polarisation effects, the high density of polarisation charge (σ_P=~10^{13} cm^{-2}) is created in GaN/AlGaN/GaN heterostructures, causing the 2-dimension electron gases(2DEG) and 2-dimension hole gases(2DHG) to coexist between AlGaN/GaN and GaN/AlGaN interface, respectively[68]. Source, Gate, and Drain electrodes are all present in PSJ HFETs. Source and Drain make ohmic contact with 2DEG. P-type ohmic

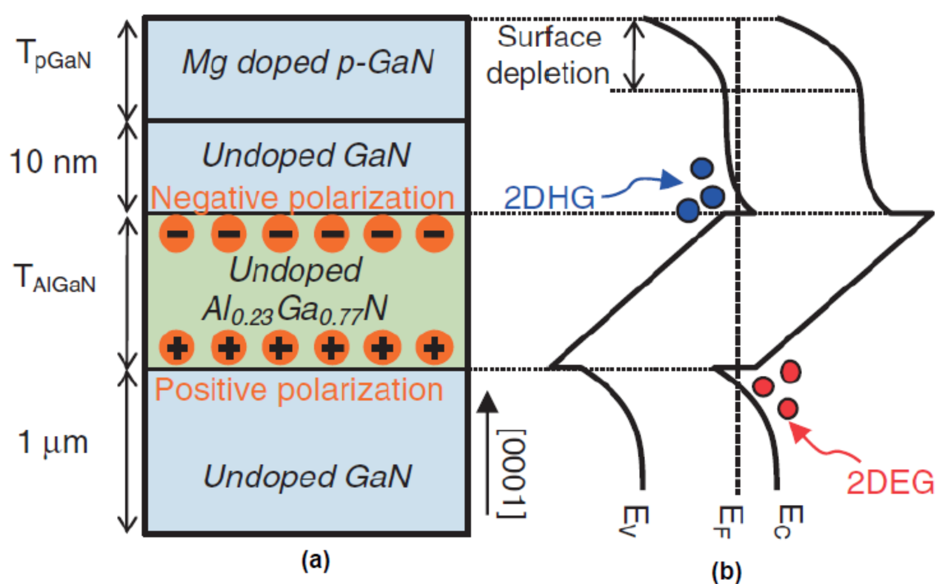


Figure 2.25 Schematics of (a) layer structure and (b) band diagram[68].

gate assists the transportation of 2DHG during the switching process.The passivation details are not shown in [68].Although the passivation details are not mentioned in the ref. [69], the composition of SiN,SiO_2 and polyimide are the main choices for the passivation in the PSJ HFETs.

In the conventional P-GaN HEMTs,P-type ohmic or schottky gate enables the devices to attain the normally-off function. However,due to the considerably thicker top u-GaN layer and AlGaN layer in PSJ HFETs, the P-type gate design cannot achieve the normally-off function in PSJ HFETs.

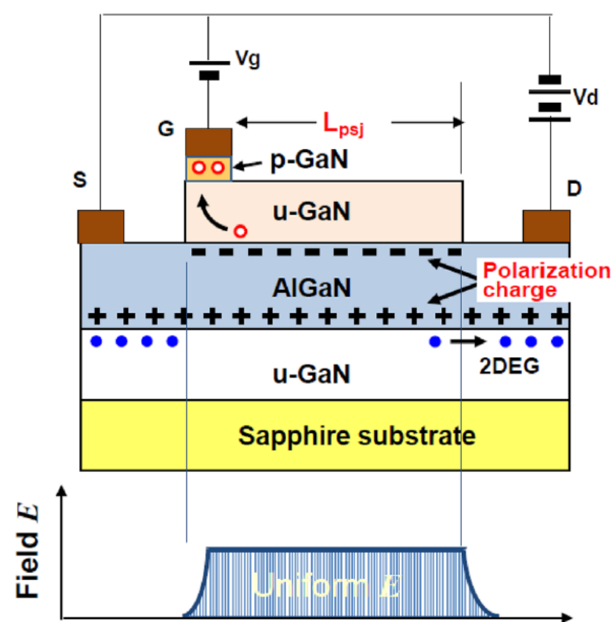
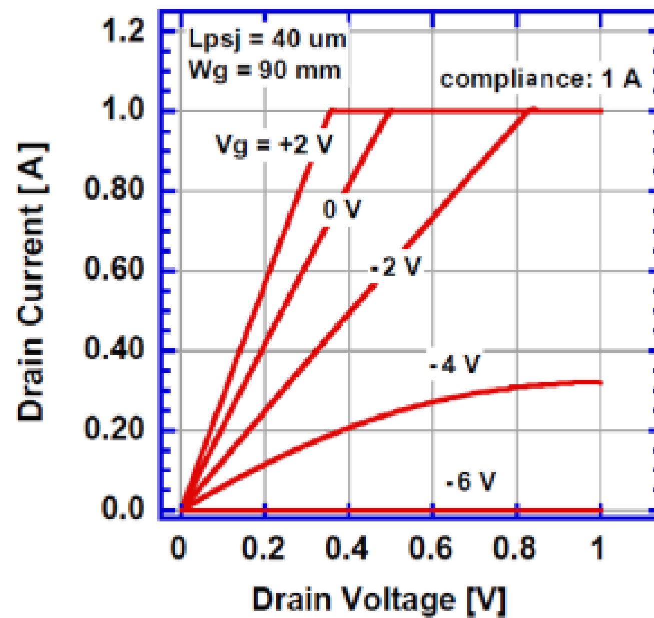
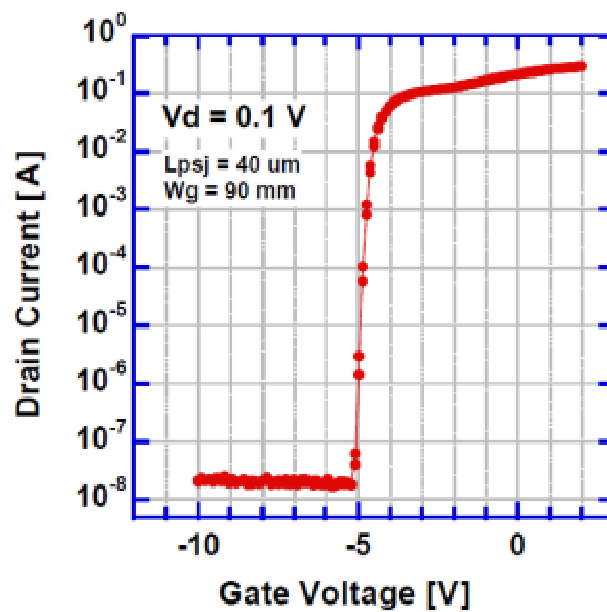


Figure 2.26 The cross-section and electric field distribution under the ideal condition of PSJ HFETs during off-state[69].

Similar to AlGaN/GaN HEMTs, when the drain bias is applied while the device is in the on-state, current flows through the 2DEG channel. Typical transfer and Id-Vd characteristics of PSJ HFETs are depicted in Figure 2.27 [69]. The Vth is around -5V, representing that they are normally-on devices. However, under



(a)



(b)

Figure 2.27 Typical (a)transfer characteristics and (b) Id-Vd characteristics of PSJ HFETs [69].

the off-state, as Figure 2.26 illustrates, 2DEG and 2DHG are discharged through the drain and gate, respectively, which achieves the ideal charge balance condition in the drift region (PSJ region). Therefore, the flat and box-shaped

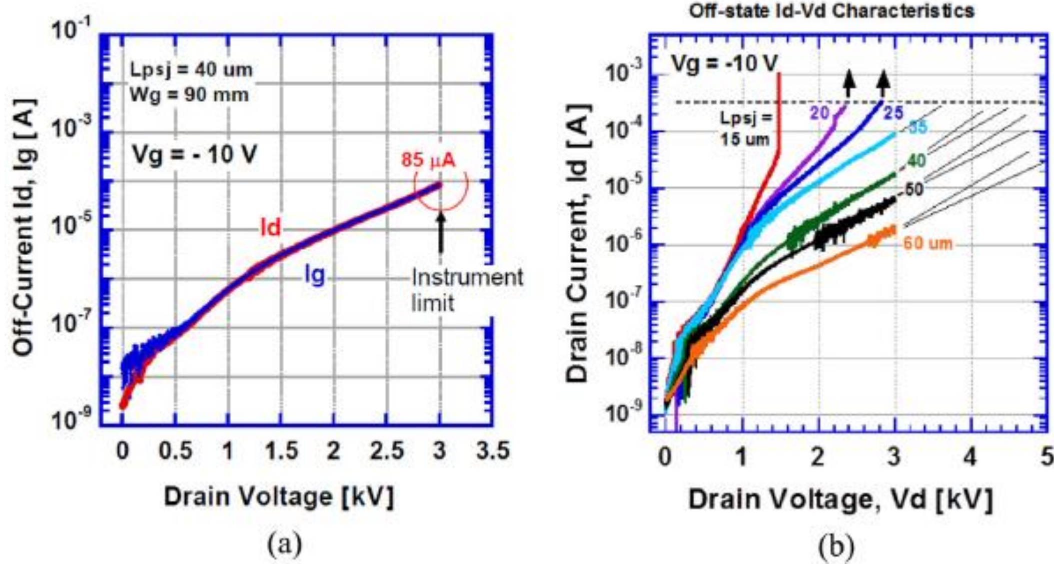


Figure 2.28 (a)Typical gate leakage(Ig) and drain leakage(Id) characteristics of Lpsj=40um (b) the breakdown characteristics as a function of PSJ Length during the off state of the PSJ HFETs with Wg=90mm. Furthermore, they are all measured at Vgs=-10V[69].

electric field profiles can be observed in the PSJ HFETs[69], significantly enhancing BV. Moreover, PSJ HFETs have a more simplified structure as compared to the field-plate design, representing that PSJ HFETs are less challenging for device fabrication, especially for high-voltage applications.

Figure 2.28(a) shows the off-state gate leakage current (Ig) and drain leakage current (Id) of PSJ HFETs at off-state. I_d and I_g are nearly identical, indicating that in PSJ HFETs, the leakage path is from the gate to the drain under off-state [69].

Figure 2.28(b) demonstrates how the PSJ Length affects the usual breakdown voltage of PSJ HFETs (L_{psj}). The linear relationship between breakdown voltage (BV) and L_{psj} is presented in Figure 2.28(b), representing that BV grows linearly as the length of the PSJ drift region increases.

Compared with traditional Superjunction technology, Polarisation super-junction (PSJ) power devices do not require the precise doping control of the n-pillar and p-pillar. This is due to 2DEG and 2DHG being naturally and equally generated in the GaN/AlGaN/GaN double heterojunctions. Therefore, In the PSJ HFETs, the optimum charge balance condition and flat electric field distribution are easy to attain compared with the ideal Si Superjunction power devices. Due to the high density and mobility of 2DEG, PSJ HFETs can also attain low on-state resistance[70], indicating that they will not sacrifice the fast-switching speed, low conduction and switching losses. All these advantages enable GaN PSJ power devices to become the most competitive next-generation GaN power devices.

Nowadays, Schottky gate HFETs[47], diodes[71] and bi-directional devices[72] have been reported using the PSJ technology. More research on the design of GaN diodes using the PSJ concepts and technologies is discussed in[73]–[75].

2.7. Current collapse

Current collapse, also referred to as the dynamic on-state resistance ($R_{dynamic,dson}$) degradation, is a severe challenge for the conventional AlGaN/GaN HEMTs. This phenomenon occurs when devices are switched from off-state to on-state. The measurement setup and the switching waveform are shown in Figure 2.29[45]. The dynamic on-state resistance degrades in comparison to the static on-state resistance when the high drain-side stress voltage is applied at the off-state[45]. This effect will severely degrade the efficiency of the devices, increase the power losses and reduce the current-carrying capability during high switching speed and high voltage applications.

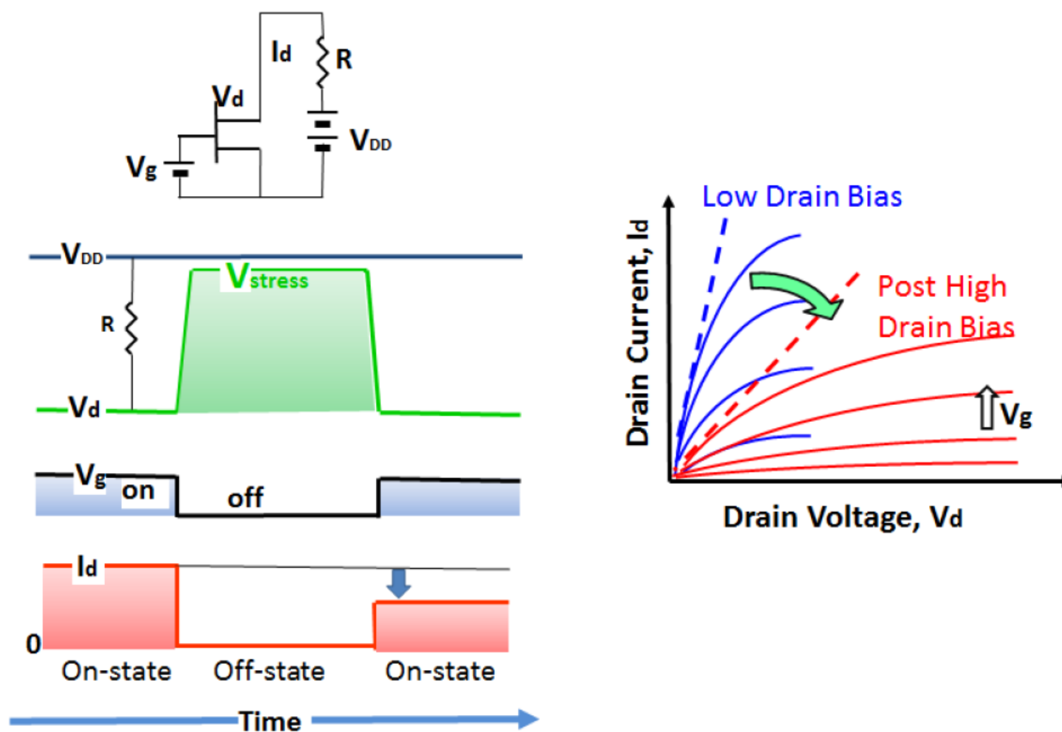


Figure 2.29 The switching waveform and circuit diagram for evaluating current collapse (left); Id-Vds characteristics of conventional HFETs(right) [45].

Current collapse originates from three main aspects: buffer trapping, surface trapping and gate instability[76].

Under the high V_{ds} stress during the off-state, the hot electrons which gained the high kinetic energy at the high-electric-field region are accelerated and trapped by the traps located at the surface or the buffer layer. When the devices switch from off-state to on-state, the trapped electrons cannot escape instantly from the traps because of the relatively long lifetime of traps, increasing the on-state resistance in comparison to the steady R_{on}. The increased dynamic R_{dson} can be recoverable if the time is sufficient after the stress is removed.

Surface trapping is caused by the surface traps along the interface of the passivation/AlGaN layer. The 2DEG is captured by the surface traps during the off-state, causing the increase of the dynamic R_{on}. The surface passivation, such

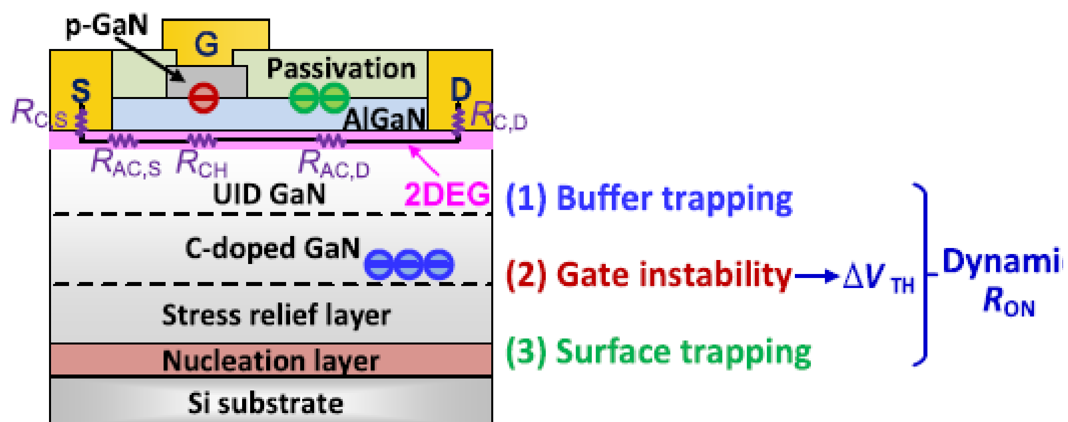


Figure 2.30 Schematic cross-section of conventional GaN-on-Si power HEMTsand the main factors for the current collapse[76].

as SiN, SiO_2 and Al_2O_3, can significantly lower the surface traps and effectively suppress the current collapse effects [77]. Alternatively, optimising the electric

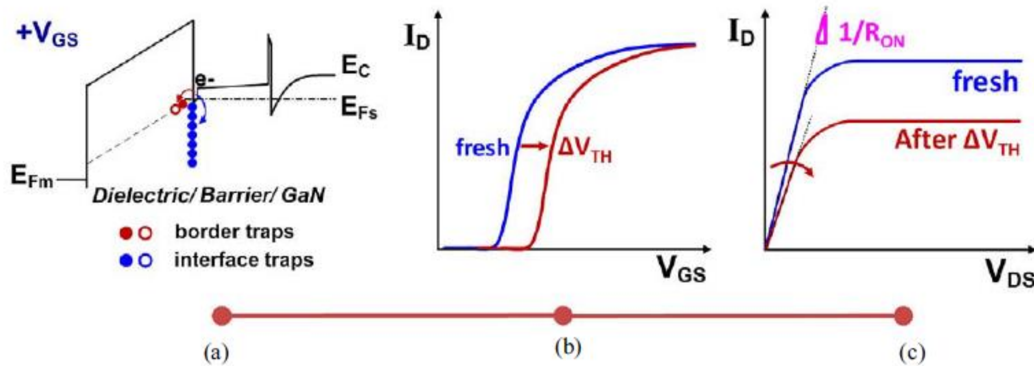


Figure 2.31 Gate-instability-induced dynamic R increase in the MIS-HEMTs (a) schematic of energy band diagram with the interface/border trapping mechanism under positive gate bias(b)positive V_{th} shift(ΔV_{th})(c)degradation of R_{on} after ΔV_{th}.

field profile is another method for mitigating the current collapse. FP technology can relax the electric field peak and minimise the impacts of current collapse effects[78], but it cannot completely solve this issue.

However, the buffer trapping has different mechanism. Due to the potential difference of the drain and substrate, the 2DEG will be escaped from the confined quantum well during the off-state and captured by the buffer traps, causing the increase of the dynamic R_{on}. The buffer trapping effects can be evaluated through back-gating measurements in GaN-on-Si power HEMTs[76]. Reducing the buffer defects during growth is an efficient way to mitigate this effect[79]. Figure 2.31 illustrates the gate instability induced by the current collapse in the MIS-HEMTs[80]. When the gate stress is applied, the border and interface traps capture the carriers, reducing the 2DEG density and producing a positive Vth shift. Therefore, dynamic R_{ds} rise because they cannot

immediately react to the variable threshold voltage from the off-state to the on-state.

2.8. Summary

In this chapter, GaN material properties are first introduced. Compared with Si, GaN is more advantageous in many aspects. Several Figures of Merits (FOMs) of Si, SiC and GaN, are discussed for different aspects. Substrate selection is also essential for GaN power devices. SiC and GaN substrate has better lattice properties than Si and Sapphire substrates. However, the low price of Si substrate is favoured by the commercial market.

Polarisation effects in AlGaN/GaN heterostructures are explored, including spontaneous and piezoelectric polarisation. Due to these polarisation effects, AlGaN/GaN heterointerface forms the high-density and high-mobility 2DEG, enabling AlGaN/GaN HEMTs to have low conduction loss and switching loss. The surface-state donor model, widely thought to be the origin of 2DEG, is also discussed in detail. The factors influencing the 2DEG sheet density, such as AlGaN layer thickness and Al mole fraction, are also presented. The device structure and the operation principle of Conventional AlGaN/GaN HEMTs are also introduced in detail.

Despite having a low on-state resistance, the breakdown voltage of AlGaN/GaN HEMTs is low due to ineffective electric field management. The typical methods for optimising the electric field distribution in the power devices include FP design, RESURF, and Superjunction technologies. For GaN power devices, polarisation superjunction technology is one of the most

effective ways to achieve flat and box-shaped electric field distribution. Due to the high density and mobility of 2DEG, GaN PSJ power devices have the potential to achieve the relatively lower conduction loss. Therefore, it can achieve low on-state resistance and high breakdown voltage simultaneously. These remarkable advantages of GaN PSJ power devices make them the most competitive next-generation power devices.

Current collapse, which significantly increases the power losses of the GaN power devices during the switching process, is also briefly reviewed. Surface trapping, buffer trapping and threshold voltage shift are the three main factors for this phenomenon.

Chapter 3. Theoretical Analysis of the Sheet Density of 2DEG and 2DHG in Polarization Super-Junction Heterostructures

The main topic of this chapter is the theoretical analysis of the impacts of the top u-GaN layer and the AlN nucleation layer thickness on the sheet density of 2DEG and 2DHG in PSJ heterostructures. The simulation and experiment results are also included to compare and validate the conclusions of the theoretical study.

3.1. Top u-GaN layer thickness

Chapter 2 already briefly introduced that the sheet density of 2DEG mainly depends on the parameter of the $Al_xGa_{1-x}N$ barrier layer, including the thickness and Al mole fraction(x) $Al_xGa_{1-x}N$[38], [39]. This chapter discusses how the top u-GaN layer affects the sheet density of 2DEG and 2DHG in the various PSJ heterostructures T. Prunty et al. [81] built the theoretical model of sheet density of 2DEG in AlGaN/GaN Heterostructures. Following a similar analysing method, Hahn et al. [82], [83]proposed the expression of the sheet density of 2DEG (n_S) and 2DHG (p_S) in the u-GaN/AlGaN/u-GaN heterostructures under different top u-GaN surface conditions. This model is built to analyse the relationship between the behaviours of threshold voltage Vth with the p_S in this article. Similarly, A. Kumar et al. [84] built the expression of the density of 2DEG and 2DHG in the GaN/AlGaN/GaN with SiO2 cap layer to investigate the threshold voltage behaviour in the P-channel GaN HEMTs

with MOS structures. Hongyang et al. [70]also analysed the 2DEG and 2DHG sheet density in PSJ heterostructures to investigate the on-state resistances in PSJ HFETs.

Although the surface donor model can be utilized to analyse the physical mechanisms of the origin of 2DEG, the expression of the sheet density of 2DEG and 2DHG cannot be obtained through it, because it neglected some components of the charges in the GaN/AlGaN/GaN heterostructures. Moreover, the possible generated charges in the PSJ heterostructures are different from the AlGaN/GaN heterostructures, causing the wrongly calculation of the sheet density of 2DEG and 2DHG. Therefore, in order to obtain the accurate expressions of them, the calculation method based on the band diagram is widely used at present.

3.1.1. U-GaN/AlGaN/u-GaN heterostructures

The expression for the density of 2DEG and 2DHG will be built first to consider the dependence on the u-GaN thickness via derivation in the u-GaN/AlGaN/u-GaN heterostructures shown in Figure 3.1.

Based on the band diagram illustrated in Figure 3.2, the expression of p_S and n_S obtained from Hahn's work is[83]:

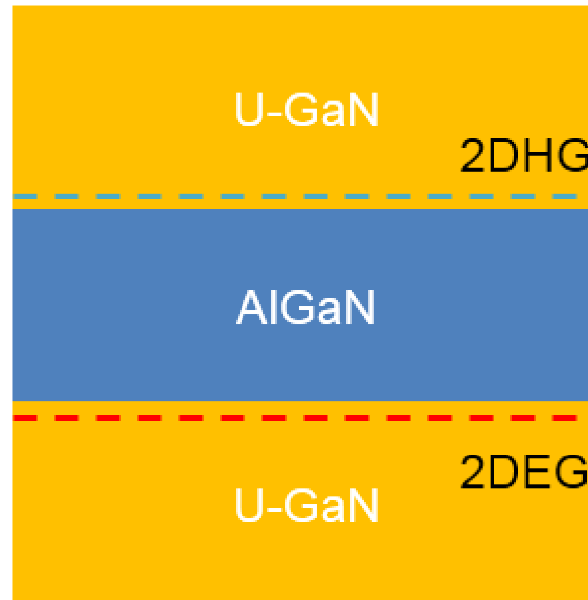


Figure 3.1 Schematic diagram of PSJ heterostructures (U-GaN/AlGaN/U-GaN).

$$p_S = \frac{1}{e} \cdot \frac{\sigma_b - \sigma_{ch} - C_{ch}\left(1 + \frac{C_b}{C_{buf}}\right)\phi_{1,p} + \frac{C_b}{C_{buf}}\sigma_n - C_b\phi_{2,p}}{1 + C_b\frac{\pi\hbar^2}{m^* e} + \frac{C_b}{C_{buf}}} \tag{3.1}$$

$$n_S \approx p_S + C_{ch}\frac{\phi_S}{e} \tag{3.2}$$

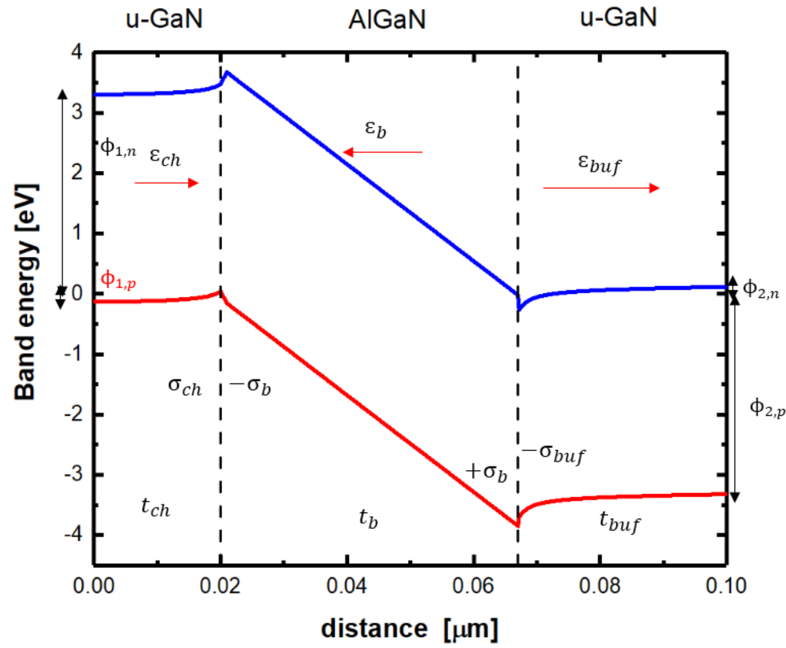


Figure 3.2 Schematic band diagram of PSJ heterostructures (U-GaN/AlGaN/U-GaN) with the free surface above the top U-GaN layer.

Where ϕ_S denotes the potential at the top U-GaN layer's top side (free surface potential),σ_b represents the polarisation charge, $\phi_{2,p}$ means the potential at the bottom-side U-GaN layer.

In Eq.(3.1) and (3.2), $C_b = \frac{\epsilon_b}{t_b}$, $C_{ch} = \frac{\epsilon_{ch}}{t_{ch}}$, $C_{buf} = \frac{\epsilon_{buf}}{t_{buf}}$ whereϵ_b, ϵ_{ch} and ϵ_{buf} are the dielectric constant of the AlGaN layer, top and bottom u-GaN layer, respectively. t_b, t_{ch} and t_{buf} are the thickness of the AlGaN layer, top and bottom u-GaN layer, respectively.

The GaN buffer layer is significantly thicker than the AlGaN layer and the top U-GaN layer in the actual PSJ devices. Thus, $C_b \gg C_{buf}$, $C_{ch} \gg C_{buf}$, and the $C_b \frac{\pi\hbar^2}{m^* e}$ are much smaller than 1.

Based on these conditions, Eq. (3.1) and (3.2) can be expressed as follow:

$$p_S = \frac{1}{e} \cdot \frac{\sigma_b - \sigma_{ch} - C_{ch}\left(1 + \frac{C_b}{C_{buf}}\right)\phi_S + \frac{C_b}{C_{buf}}\sigma_n - C_b\phi_{2,p}}{1 + \frac{C_b}{C_{buf}}} \quad (3.3)$$

$$n_S \approx \frac{1}{e} \cdot \frac{\sigma_b - \sigma_{ch} + \frac{C_b}{C_{buf}}\sigma_n - C_b\phi_p}{1 + \frac{C_b}{C_{buf}}} \quad (3.4)$$

S.Heikman et al. [39] presented that the 2DEG sheet density decreases when the top GaN thickness increases from 0 nm to 20nm. And then, it gradually saturates when the thickness exceeds 20nm.

the derivation of p_s and t_{ch} is shown in Eq. (3.5)

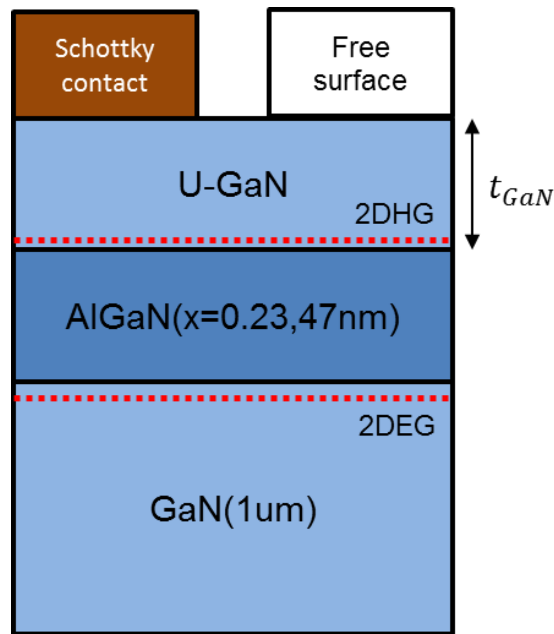
$$\frac{dp_s}{dt_{ch}} = \frac{dp_s}{dC_{ch}} \cdot \frac{dC_{ch}}{dt_{ch}} = \frac{\phi_S\left(1 + \frac{C_b}{C_{ch,n}}\right)}{e\left(1 + C_b\frac{\pi\hbar^2}{m^*e} + \frac{C_b}{C_{ch,n}}\right)} \frac{\epsilon_{ch}}{{t_{ch,p}}^2} \quad (3.5)$$

All the parameters in equation (3.5) are positive except for the ϕ_S, representing that the derivative results depend on the topside surface potential. Moreover, the ϕ_S can be extracted from the simulation tools SILVACO ATLAS TCAD. The ϕ_S is around 0.16eV, hence the $\frac{dp_s}{dt_{ch}} > 0$. By substituting the data into Eq. (3.5), the $\frac{dp_s}{dt_{ch}}$ is almost zero. Therefore, p_s is almost constant with the increase of t_{ch}. However, suppose the Schottky barrier contact ($\phi_{B,P} = 1.25eV$) is defined on the surface of the top u-GaN layer. In that case, the derivative result $\frac{dp_s}{dt_{ch}}$ is positive, representing that p_s grows when t_{ch} increases.

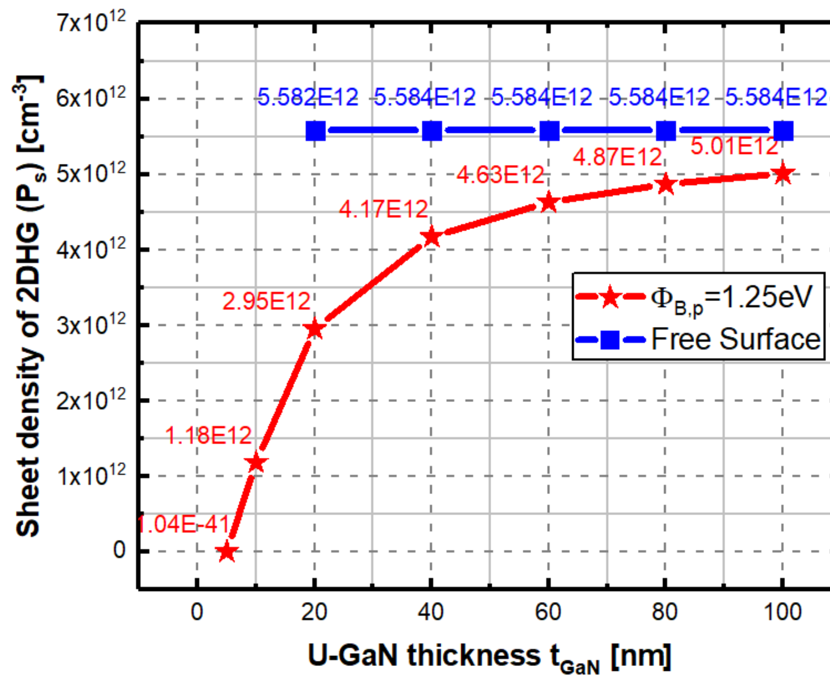
It is important to note that, surface donor model is not applicable for the calculation of the 2DEG and 2DHG sheet density. Compare with the AlGaN/GaN heterostructures, PSJ heterostructures have the more complicate

structures, indicating that the possible charges which inducing the 2DEG and 2DHG are difficult to list.

Figure 3.3(b) presents the trend analysis obtained from the simulation. Under free surface conditions, the top u-GaN layer thickness has no impact on the



(a)



(b)

Figure 3.3 (a) Schematic cross-section of U-GaN/AlGaN/U-GaN and (b) the relationship between top u-GaN thickness and 2DHG sheet density with the free surface and Schottky barrier ($\phi_{B,P}$) of the surface on top U-GaN layer.

sheet density of 2DHG. However, when the top u-GaN surface potential is the

Schottky barrier condition (1.25eV), the sheet density of 2DHG rises when the top u-GaN layer thickness increases from 5 to 100nm.

Compared with the research work which discussed the effects on the sheet density of 2DEG from 2DHG and the GaN cap layer thickness[39], our work obtained a deep understanding and comprehensive conclusion on this topic through theoretical analysis and simulation. The surface condition of the top u-GaN layer plays a critical role in the relationship between 2DHG sheet density and top u-GaN layer thickness.

3.1.2. P-GaN/GaN/AlGaN/GaN Heterostructures

PSJ heterostructures have a P-GaN layer permanently applied below the P-ohmic gate contact. Therefore, the sheet density of 2DEG and 2DHG with a varied top u-GaN layer thickness in PSJ heterostructures with the P-GaN layer are discussed in this section.

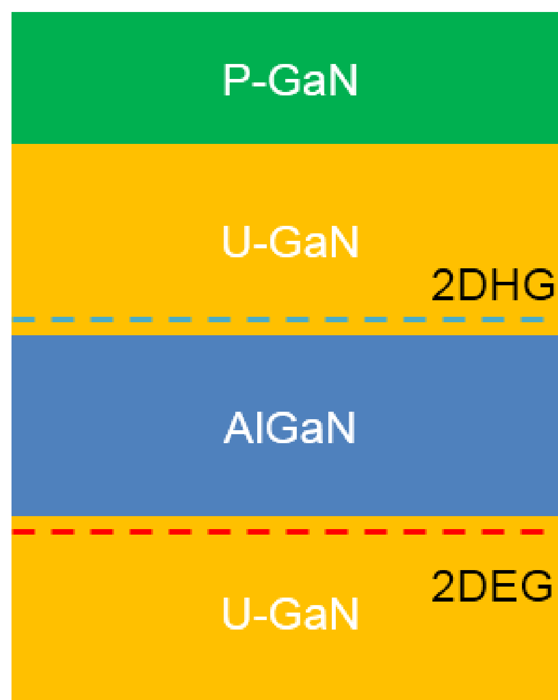


Figure 3.4 Schematic diagram of PSJ heterostructures with P-GaN layer(P-GaN/U-GaN/AlGaN/U-GaN)

The expression for the sheet density of 2DEG and 2DHG is first developed using a similar analytical technique outlined in the previous section. The cross-section of the PSJ heterostructures with the P-GaN cap layer is illustrated in Figure 3.4, and the band diagram of the heterostructures is depicted in Figure 3.5.

The Gauss law is applied at the interface of the P-GaN/u-GaN, top u-GaN/AlGaN, respectively:

$$\epsilon_{ch}\varepsilon_{ch} - \epsilon_p\varepsilon_p = \delta_{p-GaN} \tag{3.6}$$

$$\epsilon_{ch}\varepsilon_{ch} + \epsilon_b\varepsilon_b = \delta_p - ep_s \tag{3.7}$$

Where ε_{ch}, ε_p represents the electric field in the top u-GaN layer and P-GaN layer, respectively.δ_{p-GaN} is the sheet density of holes at the interface of Pthe -GaN/u-GaN layer.$\varepsilon_b$and t_b is the electric field, and the AlGaN layer thickness, respectively.σ_p, is the polarisation charge. p_s is the sheet density of 2DHG and E_G is the bandgap of the GaN.

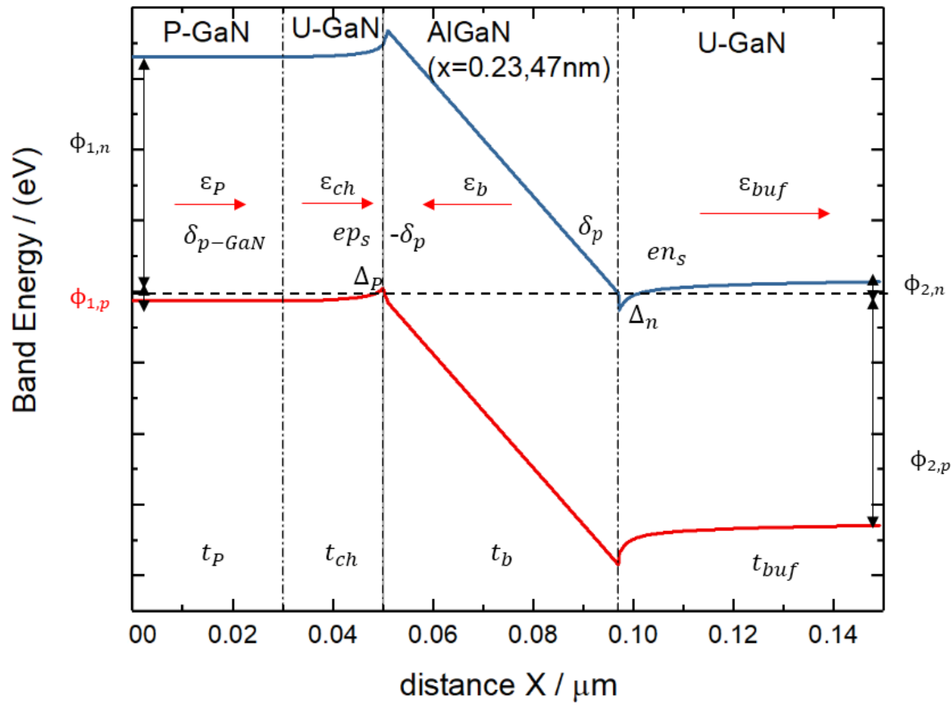


Figure 3.5 Schematic diagram of PSJ heterostructures (P-GaN/U-GaN/AlGaN/U-GaN) with the free surface above the top U-GaN layer.

The expression of ε_b is:

$$\varepsilon_b = \frac{1}{et_b}(E_G + \triangle p + \triangle n) \tag{3.8}$$

Δn and Δp are the barrier height of the conduction band and valence band edge of the quantum well below and above the Fermi level at the interface of AlGaN/U-GaN and u-GaN/AlGaN, respectively.

Based on the band diagram presented in Figure 3.5, the variation of the valence band potential towards the quantum well of the 2DHG can be represented as:

$$\frac{-\phi_{1,p}}{e} + t_{ch}\varepsilon_{ch} + t_P\varepsilon_p = \frac{\Delta p}{e} \tag{3.9}$$

Where $\phi_{1,p}$ denotes the potential at the topside of the P-GaN layer. t_{ch} is the top u-GaN layer thickness. ε_p and t_P denote the thickness and the electric field in the P-GaN cap layer, respectively.

The equation between the sheet density and the material parameters is constructed without any involvement of the electric field. Thus, the electric field will be replaced by combining Eq. (3.6)—(3.8). The equation is then expressed as:

$$\frac{-\phi_{1,p}}{e} + \frac{\delta_p - \mathrm{e}P_s}{C} + \frac{\delta_{p-GaN}}{C_{p-GaN}} - \frac{C_b}{eC}(E_G + \triangle \mathrm{p} + \triangle n) = \frac{\Delta p}{e} \tag{3.10}$$

Similarly, it can be applied to derive the expression for Δn:

$$\frac{-\phi_{2,n}}{e} + \frac{\delta_p - \mathrm{e}n_s}{C} + \frac{C_b}{eC_{buf}}(E_G + \triangle \mathrm{p} + \triangle n) = \frac{\Delta n}{e} \tag{3.11}$$

Where C is denoting:

$$\frac{1}{C} = \frac{1}{C_{p-GaN}} + \frac{1}{C_{ch}} \tag{3.12}$$

Therefore the sheet density of 2DHG(p_s)is:

$$p_s = \frac{\left(1+\frac{m_e e^2}{\pi\hbar^2 C_{buf}}\right)\delta_p - \frac{m_e e^2 C_b}{\pi\hbar^2 C_{buf}}\frac{E_G}{e} - C\left(1+\frac{C_b}{C_{buf}}+\frac{m_e e^2}{\pi\hbar^2 C_{buf}}\right)\left(\frac{\phi_{1,p}}{e}+\frac{\delta_{p-GaN}}{C_p}\right) - C_b\frac{\phi_{2,p}}{e}}{e\left[1+\frac{m_e e^2}{\pi\hbar^2 C_{buf}}+\frac{\pi\hbar^2}{e^2 m_h}\left(1+\frac{C}{C_b}+\frac{C}{C_{buf}}\right)C_b + \frac{C_b}{C_{buf}}+\frac{m_e}{m_h}\frac{(C_b+C)}{C_{buf}}\right]} \tag{3.13}$$

The sheet density of 2DEG (n_s) is:

$$n_s = \frac{\left(-\frac{\phi_{1,p}}{e}+\frac{\sigma_b}{C}+\frac{\sigma_{p-GaN}}{C_{p-GaN}}-\frac{C_b E_G}{eC}\right)\left(\frac{C_b}{eC_{ch}}\cdot\frac{\pi\hbar^2}{m_h}\right) + \left(\frac{C_b}{eC}\cdot\frac{\pi\hbar^2}{m_h}+\frac{\pi\hbar^2}{em_h}+\frac{e}{C}\right)\left(\frac{\phi_{ch}}{e}-\frac{\sigma_b}{C_{ch}}+\frac{C_b E_G}{eC_{ch}}\right)}{\left(\frac{C_b}{eC}\cdot\frac{\pi\hbar^2}{m_e}\right)\left(\frac{C_b}{eC_{ch}}\cdot\frac{\pi\hbar^2}{m_h}\right) - \left(\frac{C_b}{eC}\cdot\frac{\pi\hbar^2}{m_h}+\frac{\pi\hbar^2}{em_h}+\frac{e}{C}\right)\left(\frac{C_b}{eC_{ch}}\cdot\frac{\pi\hbar^2}{m_e}+\frac{\pi\hbar^2}{em_e}+\frac{e}{C_{ch}}\right)} \tag{3.14}$$

The bottom GaN layer is significantly thicker than the top U-GaN layer and AlGaN layer in the actual PSJ devices. Thus, $C_b \gg C_{buf}$, $C_{ch} \gg C_{buf}$. Based on this assumption, the expression of n_s and p_s can be simplified as:

$$p_s = \frac{\delta_p + \delta_{p-GaN} - \frac{C_b \cdot E_G}{e} - \frac{C \cdot \phi_{1,p}}{e}}{e} \tag{3.15}$$

$$n_s = \frac{\delta_p - \frac{C_b \cdot E_G}{e} - \frac{C_{buf} \cdot \phi_{1,n}}{e}}{e} \tag{3.16}$$

The simplified formulation of n_s in P-GaN/GaN/AlGaN/GaN heterostructures similarly exhibits no link between n_s and t_{ch}. Consequently, t_{ch} has minimal impact on the sheet density of 2DEG.

As for the impacts on the 2DHG sheet density, all other parameters in equation (3.15) are assumed to be constants, with the top u-GaN layer's thickness being the only variable. As a result, the expression of p_s derivation of t_{ch} is:

$$\frac{dp_s}{dt_{ch}} = \frac{dp_s}{dC} \cdot \frac{dC}{dt_{ch}} = \frac{\phi_{1,p}}{e^2} \cdot C^2 \frac{1}{\epsilon_{ch}} \tag{3.17}$$

According to the equation, only $\phi_{1,p}$ determine whether the derivation results are positive or negative. Therefore, the relationship mainly depends on the $\phi_{1,p}$. Considering that the surface condition of the P-GaN layer is ohmic conditions, $\phi_{1,p}$ is around 0.1eV, hence the $\frac{dp_s}{dt_{ch}} > 0$, indicating that the p_s barely increases with the increase of t_{ch}. AlGaN thickness is set to 47 nm, and the Al mole content is set at 0.23. The expression of P_s can be built in MATLAB, and the relationship between p_s and t_{ch} is plotted in Figure 3.6.

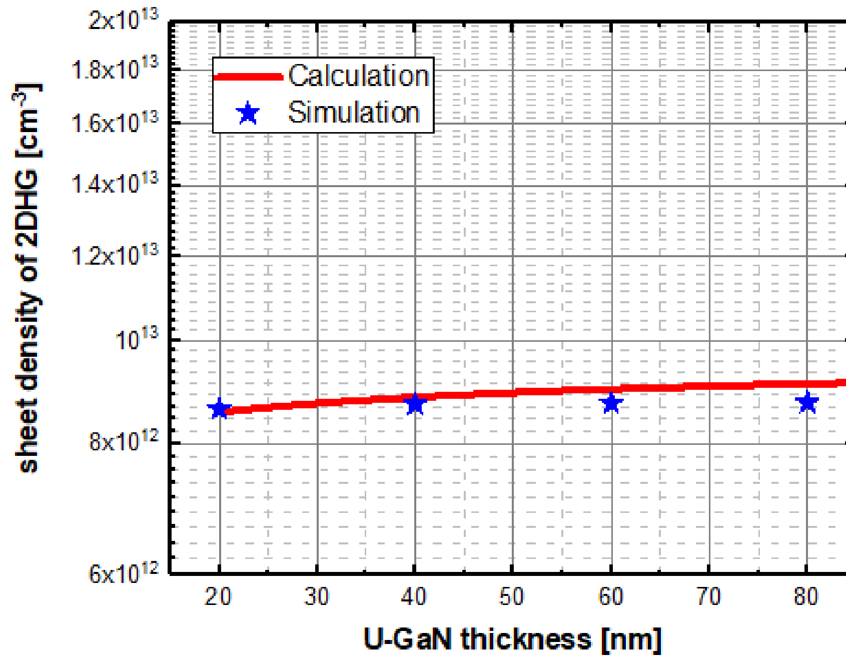


Figure 3.6 The calculated and simulated results of the relationship between top U-GaN thickness and sheet density of 2DHG are extracted from the numerical model of P-GaN/u-GaN/AlGaN/U-GaN heterostructures.

The simulation results are obtained from the SILVACO ATLAS TCAD. Additionally, the simulated structure shares the same dimensions as the

structures used in the theoretical study. As Figure 3.6 presents, the calculation and simulation results are well fitted, and both indicate that the p_s slightly increases with the increase of t_{ch} when the thickness is above 20nm.

Moreover, A.Nakajima et al. reported the sheet density of 2DHG as a function of temperature with two different u-GaN thicknesses (t_{ch} = 20 and 60 nm), and the results are displayed in Figure 3.6 [85]. These findings indicate that, at low temperatures, the top u-GaN thickness has no effect on the sheet density of 2DHG for both $t_{ch} = 20nm$ and $t_{ch} = 60nm$. However, they are not consistent with one another at temperatures higher than 300K.

The effects of temperature on the sheet density of 2DHG are first explored to identify the reasons for the discrepancy at high temperatures. Based on the Maxwell-Boltzman distribution, the expression of the 2DHG (p_s) as a function of the temperature is presented:

$$p_s = \frac{m_h}{\pi \hbar^2} k_b \mathrm{T} \ln\left[1 + \exp\left(\frac{\Delta p}{k_b T}\right)\right] \quad (3.18)$$

Where m_h is the effective mass, T is the temperature, and Δp denotes the height of the valence band edge above the Fermi level at the interface of U-GaN/AlGaN. Δp is around 0.1eV, $k_b T \approx 0.026eV$, hence exp $(\frac{\Delta p}{k_b T}) \gg 1$. The expression of p_s can be simplified as:

$$p_s = \frac{m_h}{\pi \hbar^2} \Delta p \quad (3.19)$$

In Eq.(3.19), all the parameters are independent of the temperature. As a result, the temperature barely affects the sheet density of 2DHG in the P-

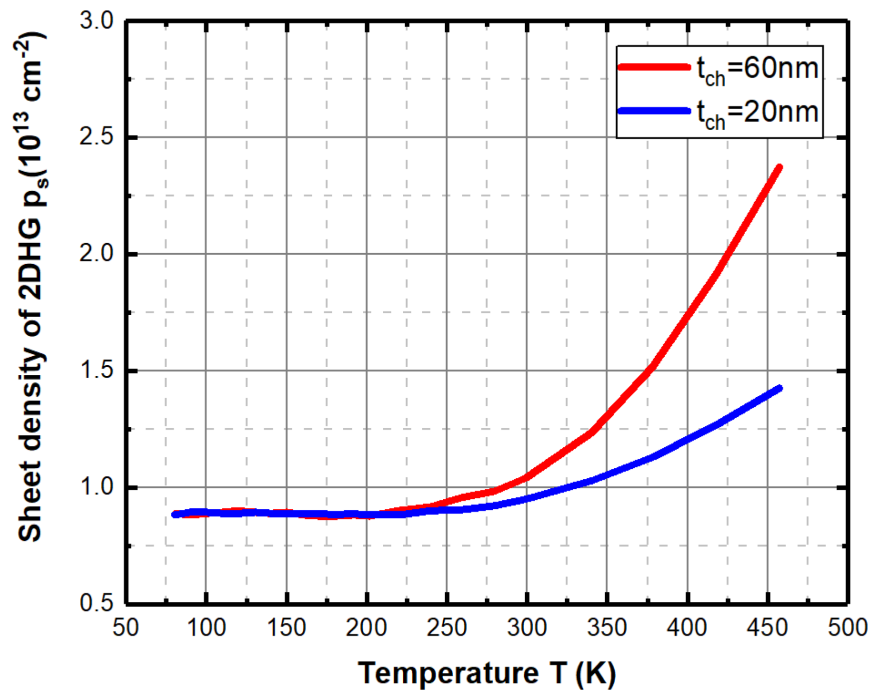


Figure 3.7 Measured sheet density of 2DHG with different top u-GaN thicknesses under different temperatures by Nakajima. [85]

GaN/GaN/AlGaN/GaN heterostructures, representing temperature is not responsible for the inconsistency of hole density between two different top u-GaN thickness at elevated temperatures. A.Nakajima et al. [85] explained that the Mg impurities in the p-GaN layers are thermally activated, causing the increase of the hole density at high temperature.

Combined with the measured data reported by A.Nakajima et al. [85], it can be concluded that the sheet density of 2DHG will marginally increase with top u-GaN thicknesses ranging from 20 to 100 nm. Moreover, A.Nakajima et al. [85] also presented that P-GaN thickness has almost no impact on the sheet density of 2DHG when it varies from 20nm to 60nm at room temperature, indicating

that it will not significantly influence the charge balance situation in PSJ heterostructures.

3.2. The AlN nucleation layer thickness

At present, GaN lateral power devices are grown on the foreign substrates, such as Si, SiC and Sapphire. However, the lattice mismatch between the GaN buffer layer and the foreign substrate is generated, causing the increase of the dislocation density and leakage current. Therefore, it requires the AlN layer between the GaN buffer layer and foreign substrate to act as a nucleation layer which can reduce the lattice mismatch and dislocation density between them during growth process [20] [87].

PSJ power devices are now grown on the foreign substrate. Therefore, the AlN nucleation layer is also widely applied in PSJ power devices. However, the impacts of the AlN nucleation layer on the sheet density of 2DEG and 2DHG in PSJ heterostructures are unknown, causing the uncertainty of the charge balance conditions. For example, holes and electrons are possible formed at the quantum wells at the hetero-interface of u-GaN/AlN and AlN/Si substrate[86], respectively, and the effects on the sheet density of 2DEG from these electrons and holes formed at the AlN nucleation layer are unknown. Therefore, the variation of the 2DEG density in PSJ heterostructures when inducing the AlN nucleation layer is investigated in this section. Although the buffer traps may influence the sheet density of 2DEG and 2DHG, this section aims to discusses the impacts of the AlN nucleation layer thickness. Thus, the buffer traps are not involved in the calculation and will be investigated in the future work.

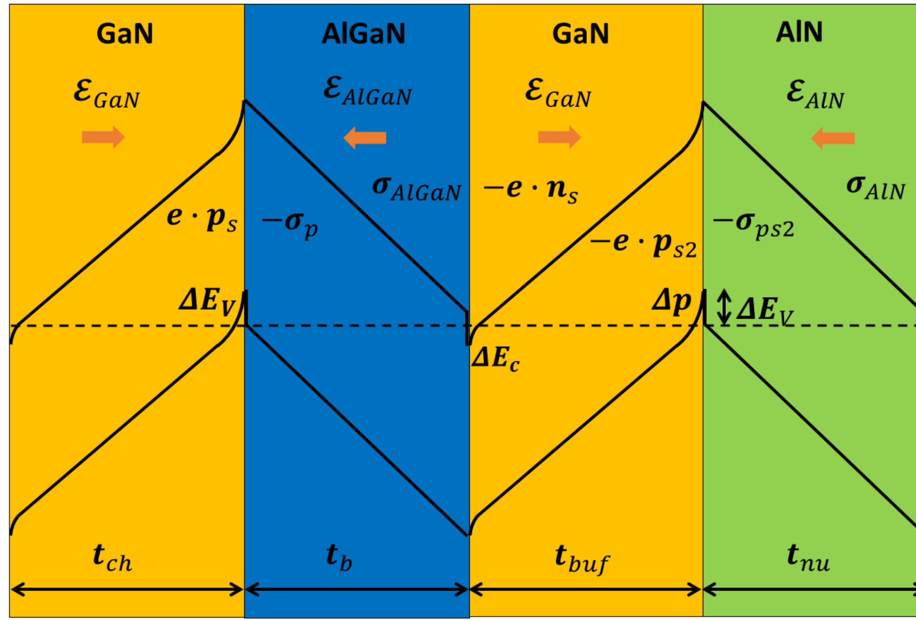


Figure 3.8 The band diagram of PSJ heterostructures with AlN nucleation layer

The band diagram of the PSJ heterostructures with the AlN nucleation layer is shown in Figure 3.8. Following a similar method, the expression of the 2DEG sheet density is built. We first apply Gauss' law at the interface of AlGaN/GaN and GaN/AlN, respectively:

$$\varepsilon_{buf} E_{buf} + \varepsilon_{nu} E_{nu} = \delta_{p2} - eP_{s2} \tag{3.20}$$

$$\varepsilon_b E_b + \varepsilon_{buf} E_{buf} = \delta_{p2} + eN_s \tag{3.21}$$

Where ε_{buf},ε_b&$\varepsilon_{nu}$are the dielectric constants of buffer, barrier and nucleation layer, Ns represents the density of 2DEG and P_{s2} represents the 2DHG density between the interface of GaN/AlN. The electric field within the barrier layer:

$$E_b = \frac{1}{et_b}(E_G + \triangle\, \mathrm{p} + \triangle\, n) \tag{3.22}$$

The relationship between quantum wells and sheet density is as follows:

$$\triangle\, \mathrm{p} = \frac{\Pi \hbar^2}{m_h} P_s \tag{3.23}$$

$$\triangle\, \mathrm{n} = \frac{\Pi \hbar^2}{m_e} N_s \tag{3.24}$$

Where △ p, △ n represents electron and hole quantum wells. Variation of the valence band potential

$$t_{nu}E_{nu} - t_{buf}E_{buf} + \frac{\Phi_{3,n} - \triangle E_{c2}}{e} = \frac{\Delta n}{e} \quad (3.25)$$

Combine the equation (3.20)-(3.25), the equation of 2DEG sheet density without the electric field is:

$$N_S = \frac{\Phi_{3,n}C_0 + \left(E_G + {}^{\pi\hbar^2 P_S}/_{m_h}\right)C_b - C_0\Delta E_c}{e^2 + \frac{\pi\hbar^2 C_0}{m_e} - \frac{\pi\hbar^2 C_b}{m_e}} \quad (3.26)$$

Where $C_0 = \frac{C_{nu}C_{buf}}{C_{nu}+C_{buf}}$, $C_{nu} = \frac{\varepsilon_{nu}}{t_{nu}}$(For AlN), $C_{buf} = \frac{\varepsilon_{buf}}{t_{buf}}$(For buffer GaN), $C_b = \frac{\varepsilon_b}{t_b}$(For AlGaN)

Assuming that the AlGaN thickness and Al mole fraction are constant in this model, the sheet density of 2DEG is mainly dependent on C_0, which is defined by GaN buffer and AlN nucleation layer thickness. When t_{buf} is much bigger than t_{nu}, C_0 is almost equal to C_{buf}, so the effect of the AlN layer can be ignored. Conversely, the thickness of the AlN layer will become the dominant factor and influence the density of 2DEG.

However, since the u-GaN buffer layer thickness (around 1 to 4 um) is much higher than the AlN nucleation layer (less than 100nm) in the actual PSJ wafers, thus the effects on the sheet density of 2DEG when inducing the AlN nucleation layer are negligible.

3.3. Summary

In this chapter, the impacts from top u-GaN and AlN nucleation layer thickness on the sheet density of 2DEG and 2DHG in the PSJ heterostructures are discussed through the theoretical analysis.

Firstly, the relationship between the top u-GaN layer thickness and the sheet density of 2DHG and 2DEG in PSJ heterostructures is discussed through theoretical analysis. Moreover, the simulation and measurement results are also presented to validate and support the theoretical analysis.

In u-GaN/AlGaN/u-GaN heterostructures, the relationship between the sheet density of 2DHG and the top u-GaN layer thickness mainly depends on the surface potential of the top u-GaN layer. It concludes that the sheet density of 2DHG is inconsistent with u-GaN thickness under the free surface condition. However, the sheet density of 2DHG rises when the Schottky surface conditions are introduced. Similar conclusions can be drawn from the PSJ heterostructures with a P-GaN cap layer. When the ohmic surface condition is applied, similar to the findings in A. Nakajima's article[85], 2DHG density slightly rises with the thickness of the top u-GaN layer.

Furthermore, an investigation has been done into how the AlN nucleation layer affects 2DEG sheet density. It concludes that the relationship between the thickness of the AlN nucleation layer and the buffer GaN layer plays a critical role in determining the sheet density of 2DEG. Considering that the GaN buffer

layer is substantially thicker than the AlN nucleation layer in the actual PSJ wafer, the impacts on 2DEG sheet density are marginal.

Chapter 4. Fabrication and Evaluation of PSJ-on-Si Power devices

In this chapter, the electrical results of PSJ on silicon power devices fabricated on Si substrate at the University of Sheffield are presented. Additionally discussed are specifics on the design information, fabrication process flow, and electrical performance of the manufactured PSJ-on-Si Power devices.

4.1. Design objective

The maximum rated voltage for commercial GaN power devices is 600V/650V. It has been shown that PSJ-on-sapphire power devices are one of the most promising technologies for 1.2kV-level GaN power devices [69]. However, compared with GaN-on-Sapphire power devices, Si substrate is preferable for manufacturers because of the relatively low costs and mature fabrication technologies[88]. Therefore, this work discusses the fabrication feasibility and fundamental performance of PSJ-on-Si power devices.

According to the present development situation, the design objectives for the fabricated PSJ-on-Si devices are to:

1. Evaluate the functionality of PSJ Power devices (including PSJ HFETs and PSJ hybrid diodes) on Si substrate.

2. Device Scalability: Evaluate the finger length and quantity that influence the performance of PSJ power devices, especially on Specific Ron.

3. Investigate the relationship between specific R_{on} and BV of the PSJ-on-Si power devices.

4.2. Device design information

Based on the design objectives, the information on the fabricated PSJ-on-Si devices is shown below:

Table 4-1 The design information of PSJ-on-Si power devices

Designed devices	PSJ Length (L_{PSJ})[μm]	Finger Length (total gate periphery) [μm]	Finger quantity
PSJ-diode	5	50	1
PSJ-HFET	10	200	5
	15	500	10
	20	800	20
	25	1000	

Each group of devices with same L_{psj} have the different Finger length ranging from 50 um to 1000 um. Moreover, each group of large devices with same L_{psj} have the different finger quantity ranging from 1 to 20. Following the PSJ devices fabrication process flow shown in Appendix 1, 11 masks are required to fabricate the PSJ power devices. The mask design information and design rules are attached in Appendix 1.

4.3. Device fabrication

All of the devices and relevant test results discussed in this chapter were processed in the University of Sheffield Nanoscience device fab Lab. The device fabrication details are attached in the Appendix 1.

4.4. Electric characterisation of fabricated PSJ-on-Si devices

The measurement findings of the PSJ-on-Si devices are shown in this part, together with information about the breakdown and static properties of the manufactured HFETs and PSJ hybrid diodes as a function of L_{PSJ}, finger length, and quantity. Furthermore, the temperature effects on the Specific R_{on} of PSJ-on-Si devices are also presented.

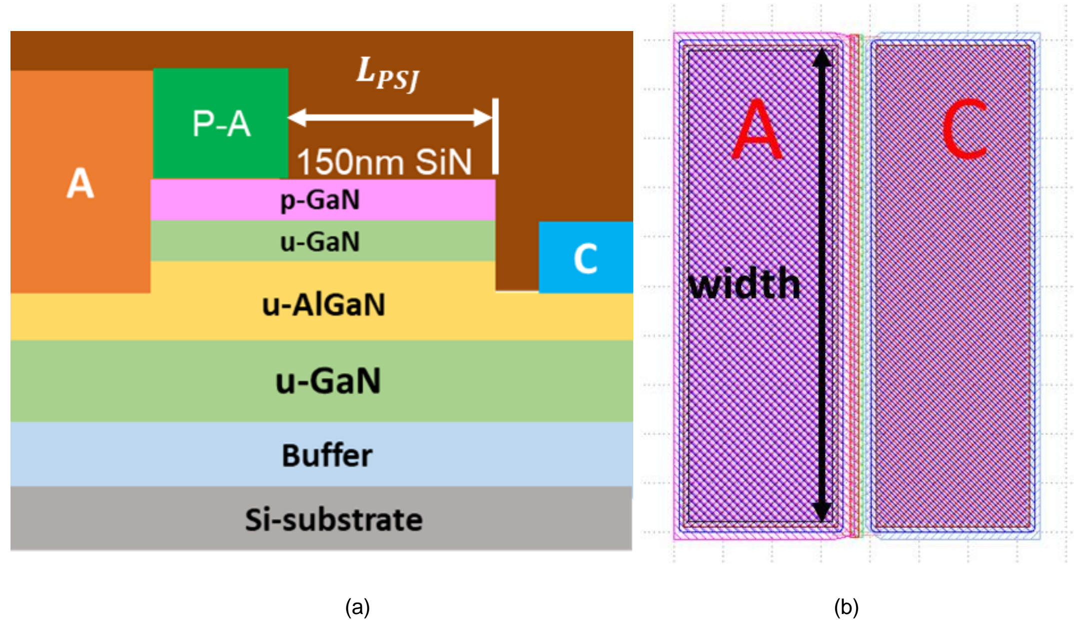
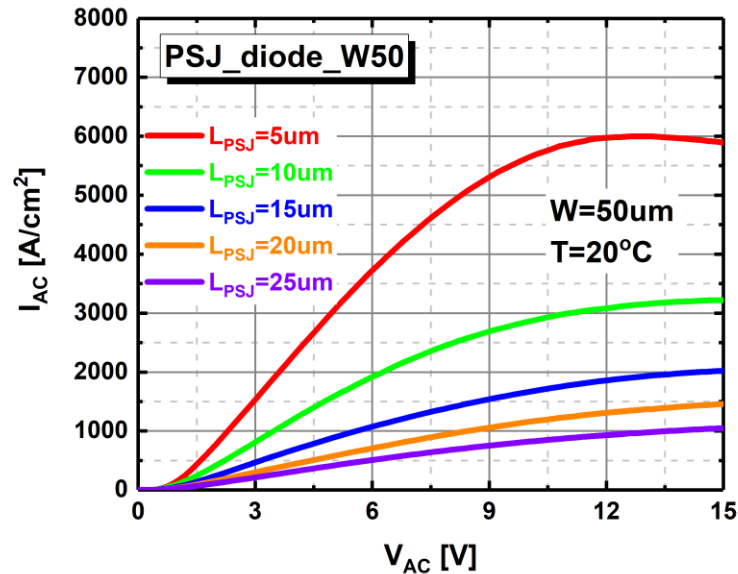


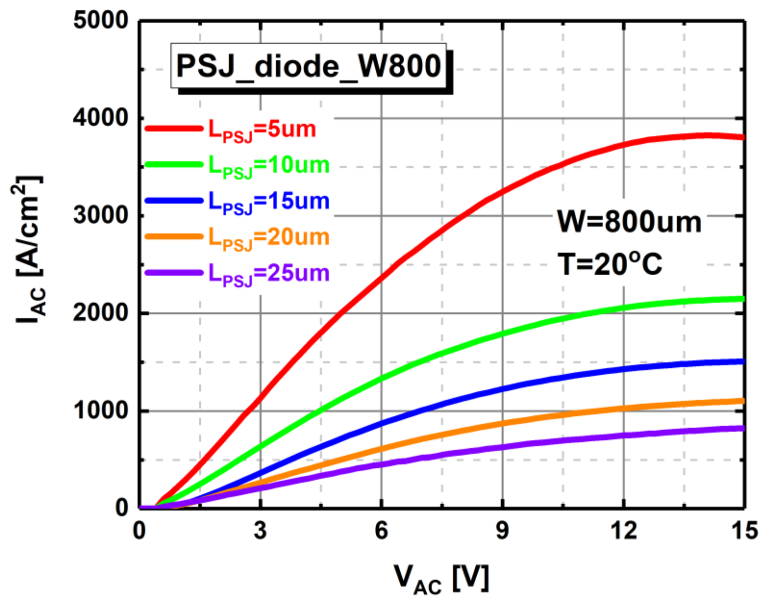
Figure 4.1 (a)The schematic cross-section of the PSJ hybrid diode(Anode is combosed by the scottky anode(orange) and P-ohmic anode(green) (b) the mask photograph of the test structure of the PSJ hybrid

4.4.1. PSJ hybrid diodes (test structure)

PSJ hybrid diode on the semi-insulating 6H-SiC substrate was first proposed in [71]. It shows low on-set Voltage (0.4V), high breakdown voltage (2400V) for L_{PSJ}=25μm and low specific R_{on}·A [71]. The cross-section of the PSJ hybrid diode



(a)



(b)

Figure 4.2 Typical PSJ hybrid diode I-V characteristics with different widths (finger length):(a)200 um and (b)800 um.

is depicted in Figure 4.1 (a). The anode is composed of the Schottky contact (above the AlGaN) and P-type ohmic contact (above the P-GaN layer). The length of PSJ is defined from the edge of the P-type ohmic contact to the edge of PSJ region shown in Figure 4.1 (a), because this is the actual drift region to support the voltage at reverse bias.

Under the forward bias, the current conducts from the Schottky Anode to Cathode through the 2DEG channel. However, the turn-on mechanism of the PiN junction is resistive, which means the voltage drop across the 2DEG region beneath the PN region must be large enough to cause a resistive voltage drop of 3.4V. With the high concentration of 2DEG, this does not happen under normal operating conditions; therefore, the PN junction does not turn on.

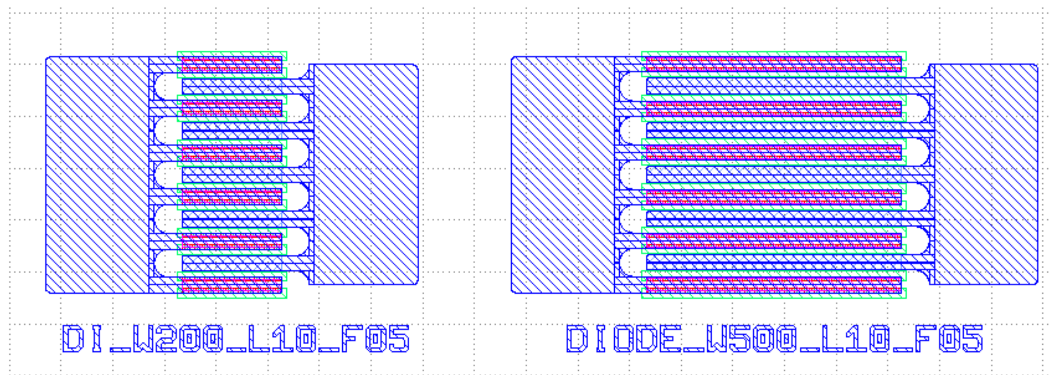


Figure 4.3 The multi-finger layout for PSJ large hybrid diode with five fingers and L_{psj} =10 um, but different finger widths (200um and 500um, respectively).

Therefore, the PSJ hybrid diode is a unipolar power device in theory. Under the reverse bias,2DEG and 2DHG are depleted. Thus it shows reverse blocking characteristics.

Firstly, the impact of L_{PSJ} and gate width (finger length) on specific R_{on}·A is investigated. The mask of the target devices is shown in Figure 4.1(b). Typical I-V properties of PSJ hybrid diodes with various widths (50 um and 800 um) as a function of L_{PSJ} ranging from 5 um to 25 um are presented in Figure 4.2. The measurement was processed at room temperature and dark conditions using the Agilent B1500A semiconductor device analyser. With a reduction in L_{PSJ}, an increase in diode current density can be seen. This is brought on by lengthening the device's active area, causing an increase in Ron. The specific R_{on}·A as a function L_{PSJ} of PSJ hybrid diode with different widths is shown in Figure 4.4. Moreover, the specific R_{on}·A of the devices with different finger lengths (50,200, 500, 800, 1000 um) is extracted.

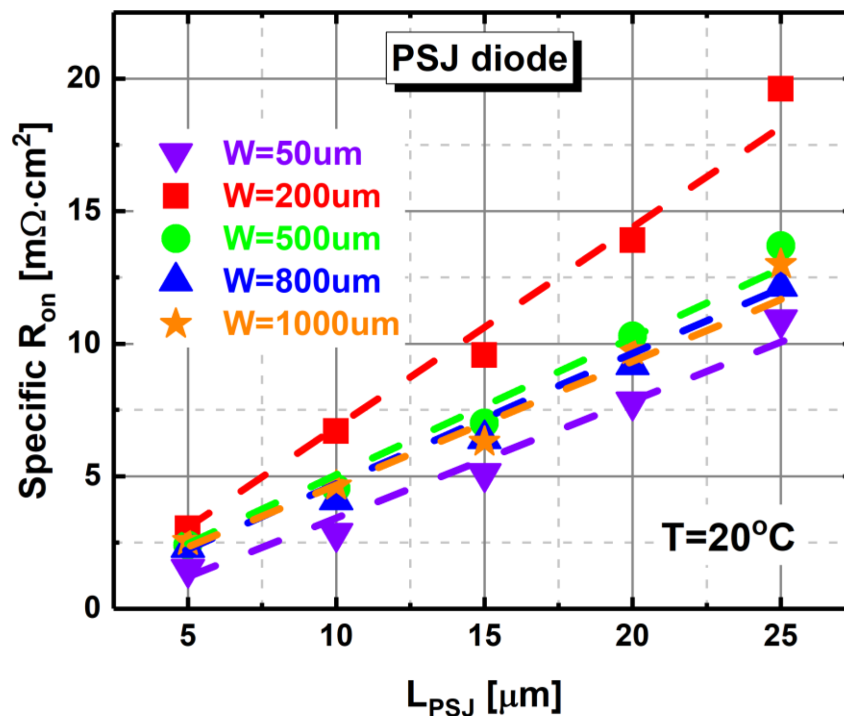
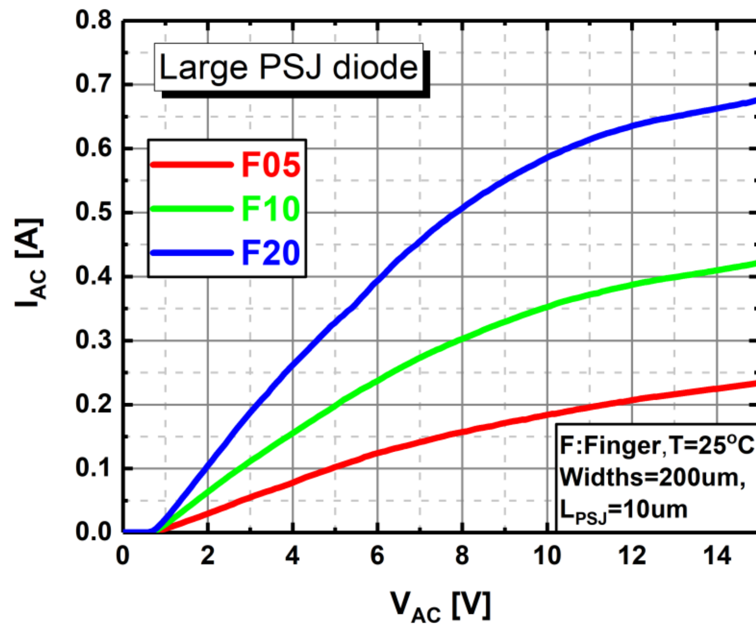


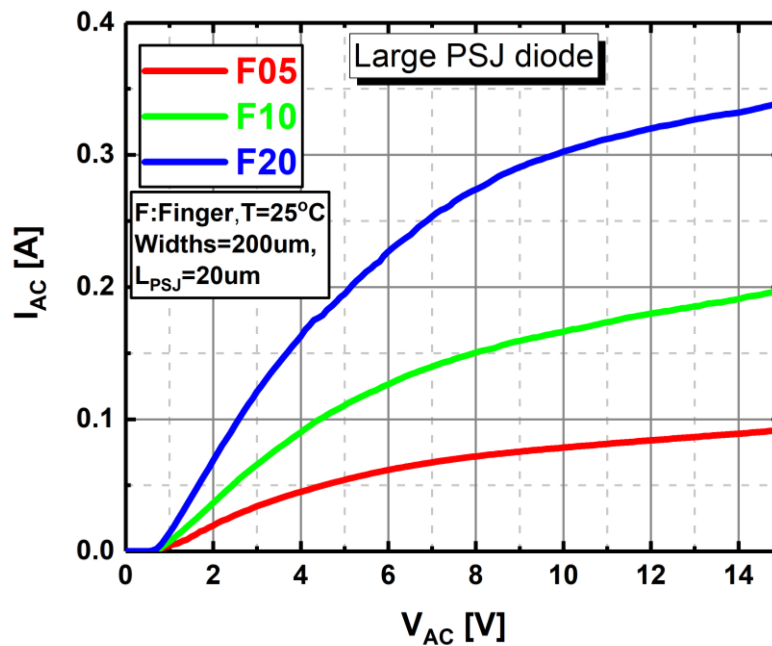
Figure 4.4 the specific R_{on}·A of PSJ hybrid diode as function L_{PSJ} (5um to 25 um) with different widths (finger length):50,200 ,500,800 and 1000 um.

The specific R_{on} obtained from Figure 4.2, is not perfectly linear as a function of L_{PSJ}, this is possibly due to the misalignment during the fabrication, causing the variation of the actual L_{PSJ}. Moreover, the thin metal thickness may also influence the value of the specific on-state resistance. However, it is still found that R_{on} shows an almost linear upward trend with increasing the length of PSJ.

4.4.2. PSJ hybrid diodes(large-area)

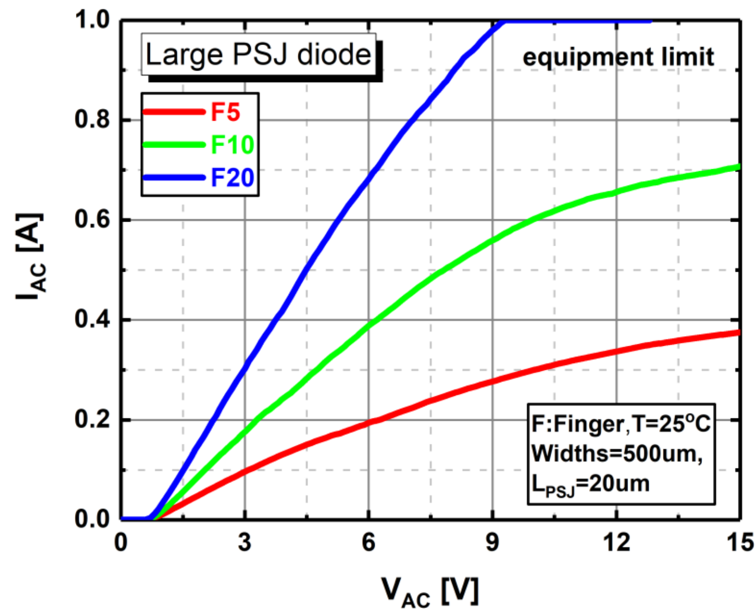


(a)

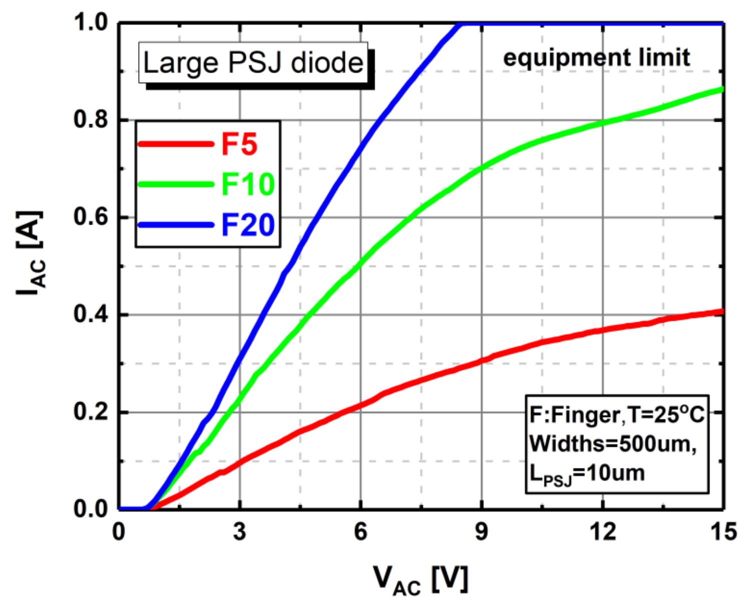


(b)

Figure 4.5 Typical I-V characteristics of PSJ hybrid diode with different finger quantities (5,10, and 20)(a)PSJ hybrid diode with L_{PSJ}=10um(b) with L_{PSJ}=20um and width=200um.



(a)



(b)

Figure 4.6 Typical I-V characteristics of PSJ hybrid diode with different finger quantities (5,10, and 20)(a)PSJ hybrid diode with LPSJ=10um(b) with LPSJ=20um and width=500um.

A typical multi-finger layout is used to design PSJ large hybrid diode and is depicted in Figure 4.3. The width (finger length) used for the large hybrid diode is 200 μm and 500 μm. The impact of finger quantity on the current density and specific R_{on}·A is discussed.

The I-V curves of a large PSJ hybrid diode with different finger quantities (5, 10, 20) are displayed in Figure 4.5.

It is evident that as the finger quantity for the PSJ hybrid diode increases, the current density of the PSJ large hybrid diode also increases, indicating that increasing the finger quantity is a feasible way to increase the current handling capability of the hybrid diodes based on the present fabrication technology. The increasing current density for the PSJ large hybrid diode with higher width (500 μm) is also shown in Figure 4.6.

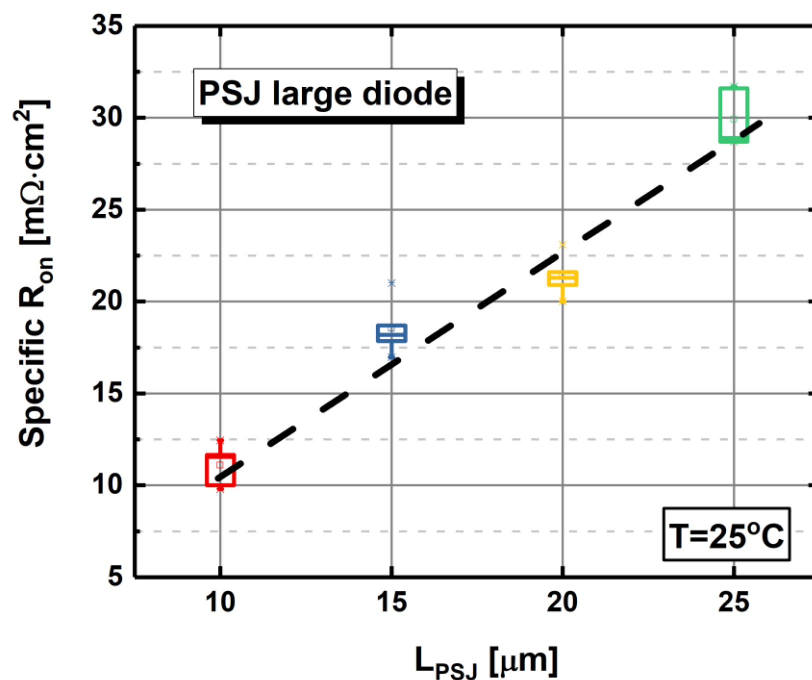


Figure 4.7 The specific R as a function L(10,15,20,25 um) for PSJ large hybrid diode.

The relationship between the specific R_{on}·A and L_{PSJ} for PSJ large hybrid diodes is built based on the identical PSJ large hybrid diodes. Furthermore, an almost linear relationship is observed, as shown in Figure 4.7. The increasing trend of the specific Ron of large-hybrid diodes is identical to that obtained from the

test-structure diodes shown in Figure 4.4. This indicates that the specific R_{on} shows a good consistency between the large-area and test-structures PSJ hybrid diodes.

4.4.3. Temperature effects on PSJ hybrid diodes

The high-temperature characterisation of current handling capability and specific $R_{on}\cdot A$ is essential for evaluating the GaN power devices 'performance [89]. This section presents the I-V characteristics of PSJ hybrid diodes (test structures with widths of 200 um) as a function of temperatures between 25 °C and 125°C in Figure 4.8.

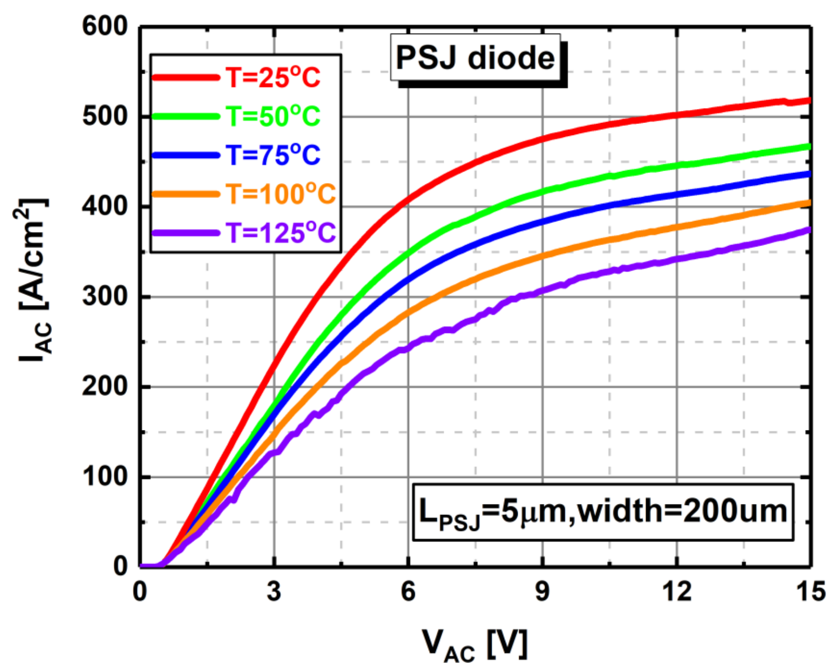


Figure 4.8 Typical PSJ hybrid diode I-V characteristics at elevated temperature from 25 °C to 125 °C with 25 °C step.

When the temperature rises, the current density of the PSJ hybrid diode tends to decrease. The drop in the current density of the PSJ hybrid diode at high temperatures is caused by the reduction of the 2DEG carrier mobility caused

by polar-optical-phonon scattering [89]. As Figure 4.9 illustrates, the PSJ hybrid diode with varying L_{PSJ} exhibits an increasing specific $R_{on}A$ as a function of temperature, which is caused by the reduction of 2DEG carrier mobility.

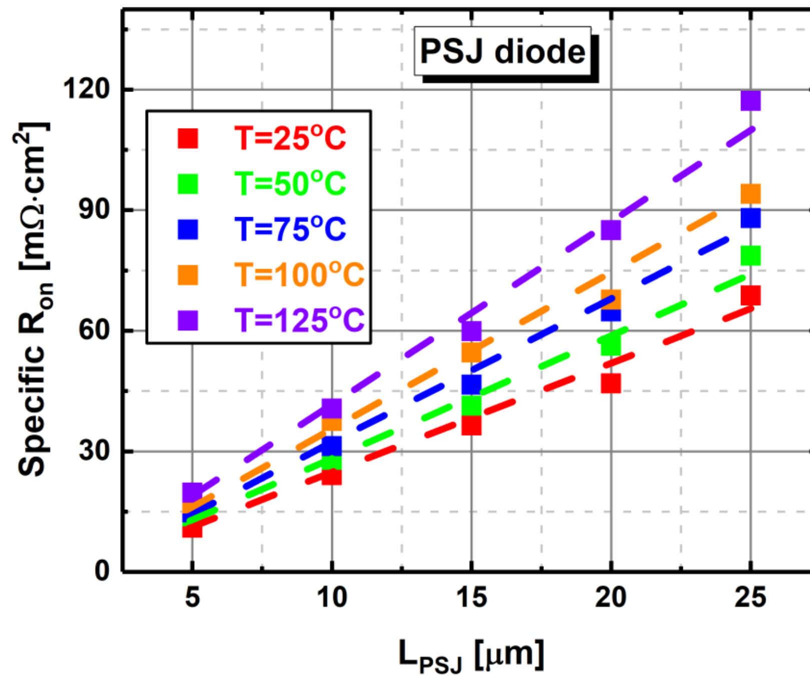
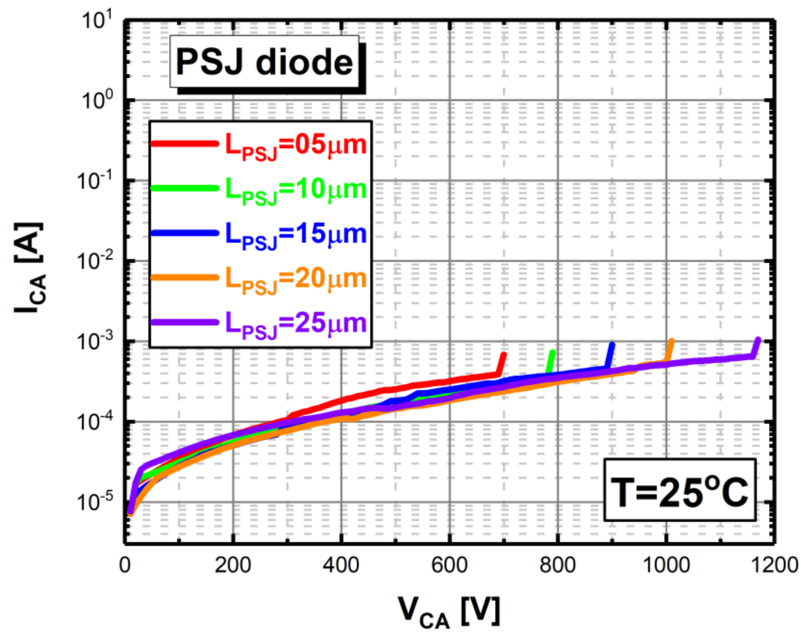


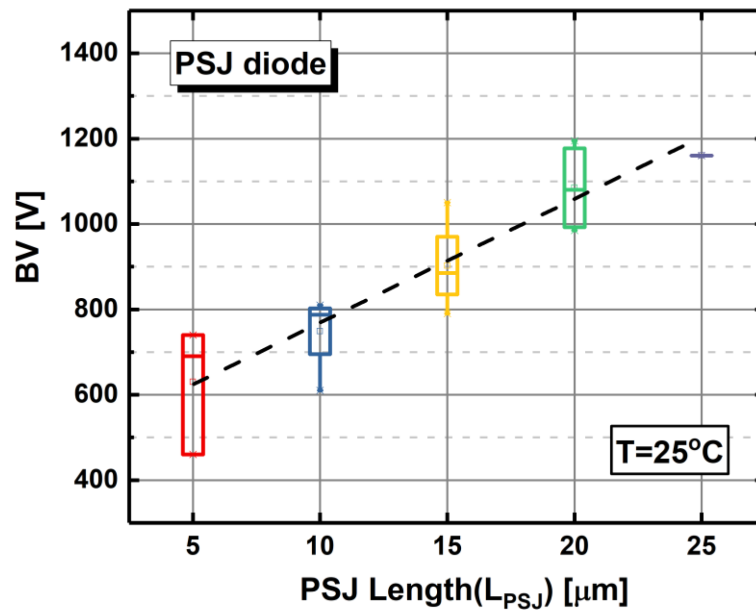
Figure 4.9 Specific R_{on}·A as a function of L_{PSJ} with the rise of temperature from 25°C to 125 °C with 25 °C step.

4.4.4. PSJ hybrid diode reverse blocking characteristics

In this section, the reverse blocking characteristics of PSJ hybrid diodes on Si substrate with varying L_{PSJ} are presented.



(a)



(b)

Figure 4.10 (a)Typical reverse blocking characteristics (b) breakdown voltage of PSJ diode as a function of L_{PSJ}, measured at 25°C.

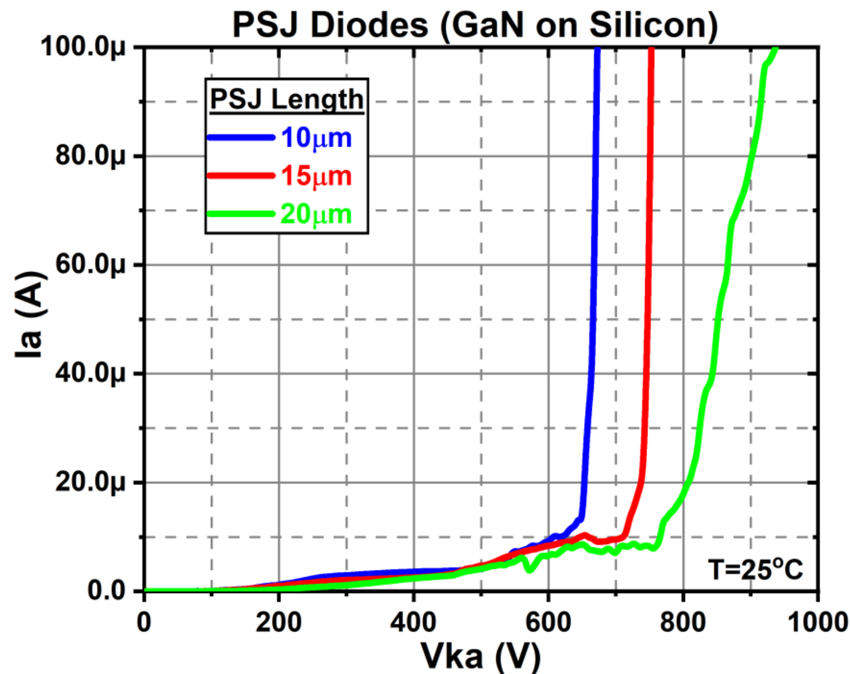


Figure 4.11 Typical reverse blocking characteristics of PSJ hybrid diodes-on-Si substrate provided by POWDEC.K.K as a function of L_{PSJ}, measured at 25°C.

PSJ hybrid diode reverse blocking characteristics and the breakdown voltage as a function of L_{PSJ} are displayed in Figure 4.10 (a) and (b), respectively. Figure 4.10(b) presents the statistical results of the measured BV of many PSJ-on-Si hybrid diodes with different L_{PSJ}. It is found that the average BV obtained from the PSJ hybrid diodes shows an almost linear relationship with L_{PSJ}. This trend is identical to the results reported on PSJ-on-Sapphire and PSJ-on-SiC substrates[69], [71]. As a comparison, the reverse blocking characteristics of PSJ diode-on-Si with similar device structures and dimensions provided by POWDEC.K.K is also measured under the same conditions presented in Figure 4.11.However,it is different from the measured results of Sheffield devices. The reasons of this discrepancy will be discussed in the next sections.

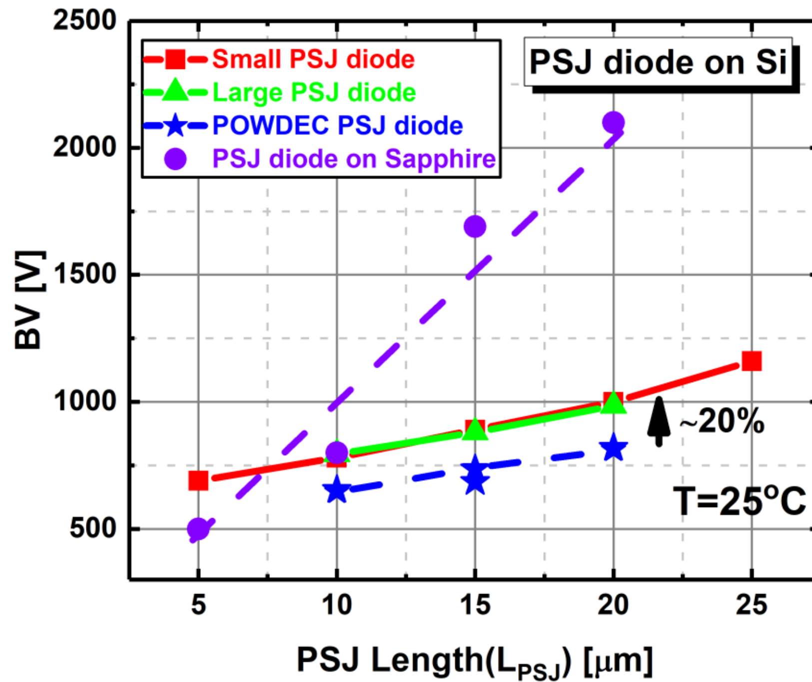


Figure 4.12 The BV of PSJ fabricated hybrid diodes are compared with the hybrid diodes-on-Si from POWDEC.K.K and diodes-on-Sapphire as a function of L_{PSJ}, which are measured at 25°C.

Measured BV of PSJ hybrid diodes, including small and large hybrid diodes as a function of L_{PSJ} from the fabricated sample, are presented in Figure 4.12. The measured BV obtained from the PSJ-on-Si sample of POWDEC.K.K and PSJ hybrid diode-on-sapphire fabricated at Sheffield with the same dimensions are simultaneously presented in Figure 4.12. PSJ-on-sapphire hybrid diodes have the same structures and dimensions as PSJ-on-Si hybrid diodes using the same fabrication technology.

From Figure 4.12, It can be observed that:

1. Breakdown voltages show an upward trend with the increasing PSJ length (drift region).

2. The BV for L_{PSJ} =5 μm and L_{PSJ} =10 μm for PSJ diodes on Si substrate are almost similar to that for PSJ diodes on Sapphire substrate. However, the BV for L_{PSJ} =15 μm and L_{PSJ}=20 μm of PSJ hybrid diodes on Sapphire substrate is much higher than PSJ-on-Si. This is possibly due to the difference in substrate resistivity. The insulating sapphire substrate has a relatively higher withstanding voltage capability in the vertical direction. Due to the vertical voltage limit, the PSJ-on-Si hybrid diodes cannot achieve the ultra-high breakdown voltage like those on sapphire substrates, similar to the challenge faced by the commercial GaN power devices on Si substrate[88], [90].

3. Compared with the PSJ hybrid diodes provided by POWDEC.K.K, the breakdown voltages of PSJ hybrid diodes fabricated at Sheffield are 20% higher than the POWDEC PSJ hybrid diodes. The possible reason for the enhancement of BV is the optimised buffer layer structure. POWDEC PSJ-on-Si utilised the undoped GaN buffer layer. However, the fabricated Sheffield PSJ-on-Si hybrid diodes have a C-doped GaN buffer layer with high resistivity[91]–[93], enhancing the vertical voltage withstanding capability. Sadahiro Kato et al. [94]reported that the C-dope GaN buffer layer is crucial for improving breakdown voltage for the AlGaN/GaN HEMTs on Si substrates. The breakdown voltage of the C-doped buffer layer is mainly related to the C-doping concentration. And it exceeds 800V when the C-doping concentration is 8e18 cm^{-3} [94].Yiqiang et al. [99] also reported that the carbon-doped GaN

buffer layer in the AlGaN/GaN HEMTs could suppress the leakage current and enhance the breakdown voltage（from 346V to 748V）.

4.4.5. PSJ HFETs (I-V static characteristics)

The fabricated PSJ HFETs are the three-terminal PSJ HFETs. Furthermore, the cross-section and dimensions of PSJ HFETs are illustrated in Figure 4.13.

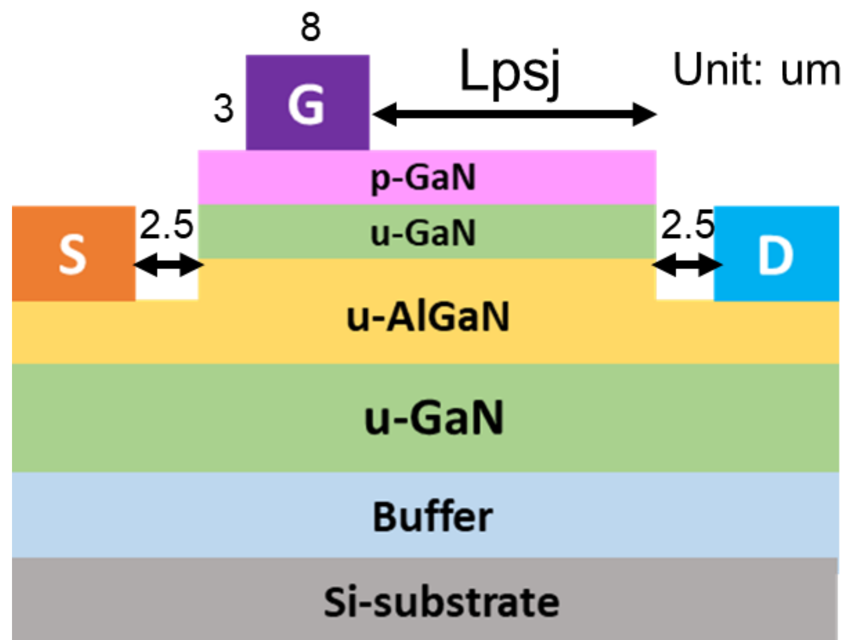


Figure 4.13 The schematic cross-section and device dimensions of the fabricated PSJ HFETs.

Typical I_d-V_d characteristics of the fabricated PSJ HFETs (gate width=50 µm and L_{PSJ}=5 µm) are presented in Figure 4.14. The measurement is carried through the Keysight B1500 semiconductor device analyser and measured at 25°C and in dark conditions.

Typical transfer characteristics of the fabricated PSJ HFETs are displayed in Figure 4.15. The kink phenomenon is observed from Figure 4.15 at V_{gs}=-3V. It is possibly related to the surface states along the upper GaN surface, and the effective surface passivation may possibly eliminate this phenomenon.

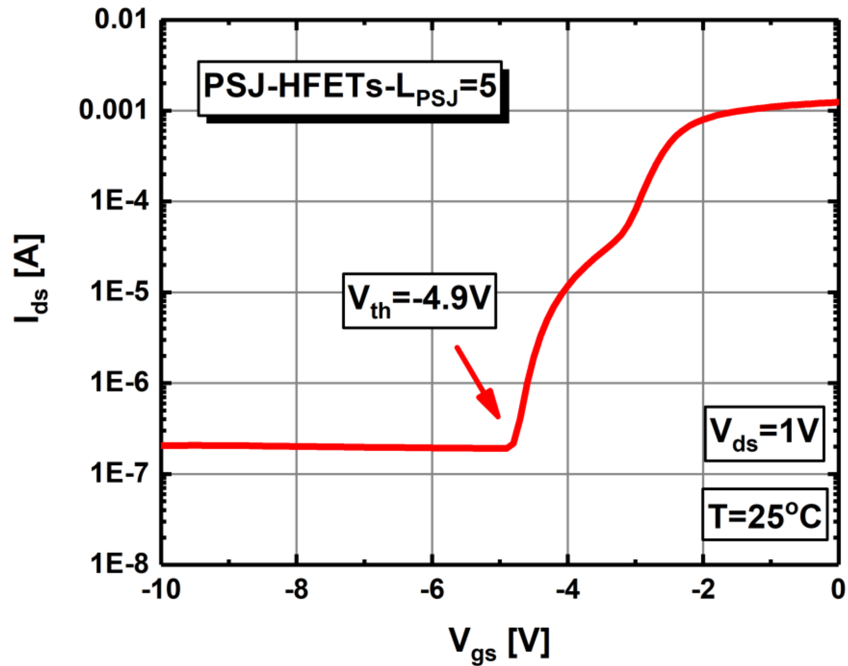


Figure 4.15 Typical transfer characteristics of the fabricated PSJ HFETs at 25°C.

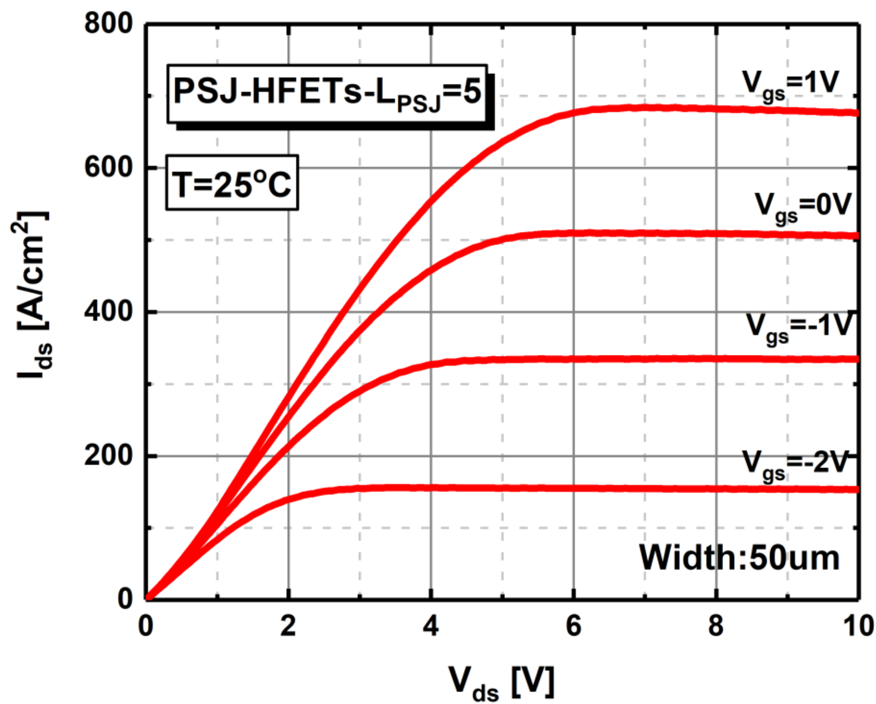


Figure 4.14 Typical I_d –V_d characteristics of the fabricated PSJ HFETs at 25°C.

However, the actual reason is under investigation and will be discussed in the future work.

The threshold voltage (V_{th}) is -4.9V, almost identical to the value reported in [69]. Therefore, the functionality of PSJ HFETs-on-Si substrate has been achieved.

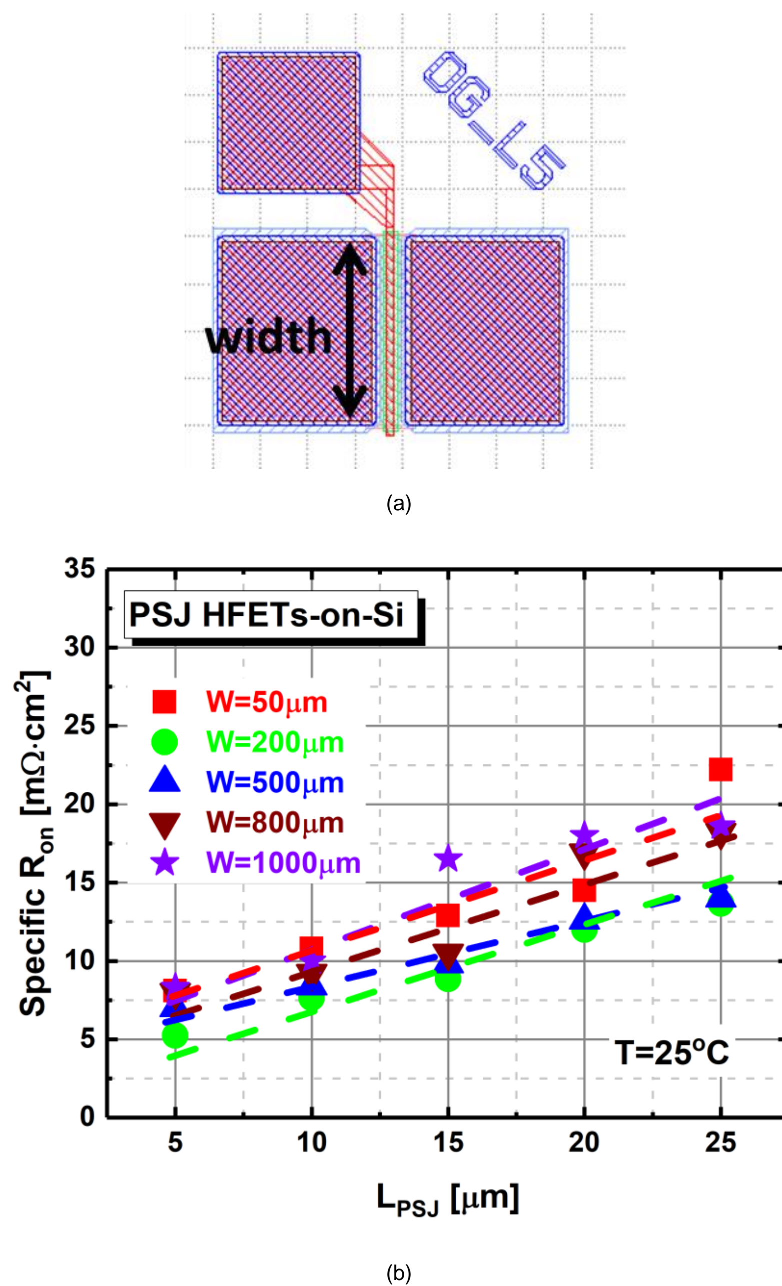
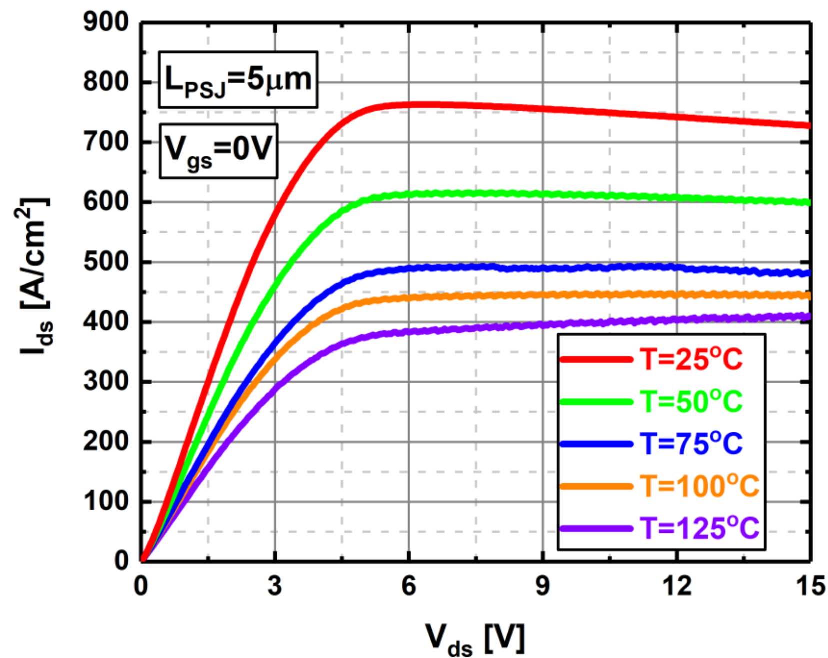
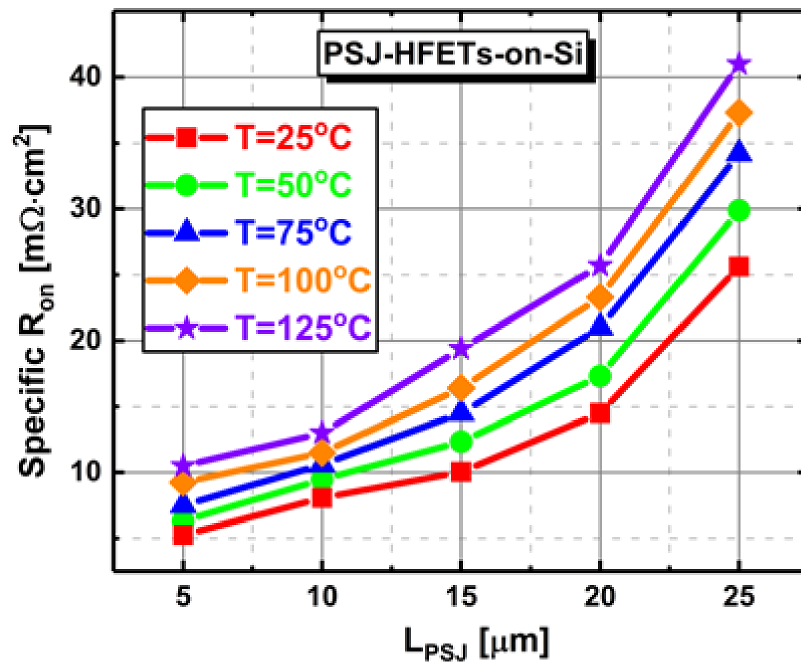


Figure 4.16 (a) The mask layout of the PSJ HFETs (b) the specific R_{on}·A as a function of L_{PSJ} of PSJ HFETs with different gate widths (50,200,500,800 and 1000 um).



(a)



(b)

Figure 4.17 (a) Typical I-V characteristics of PSJ HFETs with L_{PSJ} =5um as function of elevated temperature(25°C to 125°C) (b) the measured specific R_{on}·A as a function of L_{PSJ} (5um to 25 um)and elevated temperature(25°C to 125°C).

The mask layout of the fabricated PSJ HFETs is displayed in Figure 4.16 (a). It

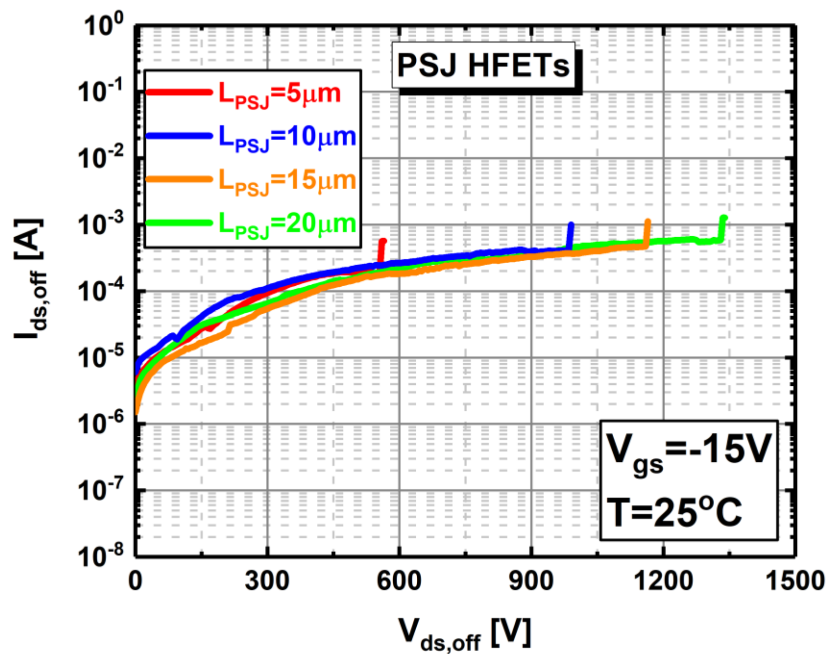
includes PSJ HFETs with various gate widths (50,200,500,800, and 1000 μm), and L_{PSJ} varies from 5 μm to 25 μm at certain gate widths. Therefore, the relationship between specific R_{on}·A and the length of PSJ region (L_{PSJ}) and gate Width impacts on specific R_{on}·A are plotted in Figure 4.16 (b).

Figure 4.16 (b) illustrates that when comparing all PSJ HFETs with various gate widths, the specific R_{on}A has a linear relationship with the L_{PSJ}. This is brought on by the channel resistance rising as the active area's length rises.

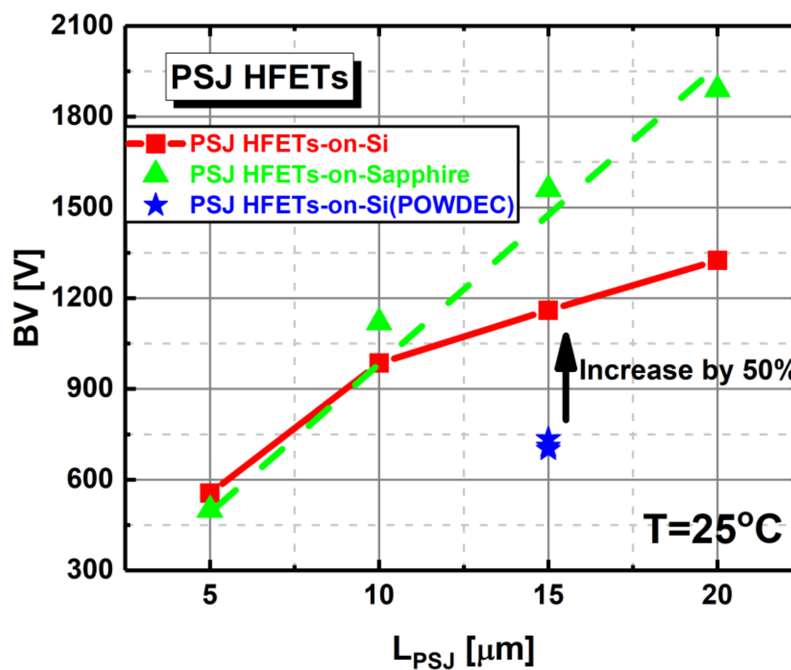
The device's scalability depends on the gate width effect on the specific R_{on}·A. The I_d-V_d curves of PSJ HFETs with L_{PSJ}=5 μm at V_{gs}=0V as a function of the temperature ranging from 25°C to 125°C are displayed in Figure 4.17 (a).

Moreover, the specific R_{on}·A shows an upward trend with the temperature rise, as presented in Figure 4.17 (b). The reason for the rise of the specific R_{on}·A is the carrier mobility reduction caused by the scattering [89].

4.4.6. The Off-state Breakdown Voltage(BV) for PSJ HFETs



(a)



(b)

Figure 4.18 (a) the off-state breakdown characteristics of PSJ HFETs with different L_{PSJ} ranging from 5 um to 20 um(b)the relationship between BV and L_{PSJ} of PSJ HFETs from Sheffield PSJ HFETs on Si and sapphire substrate and POWDEC PSJ HFETs-on-Si substrate.

The off-state breakdown voltage (BV) for PSJ HFETs is measured through Agilent Keysight B1505A Power Device Analyzer / Curve Tracer. All these measurements are processed under dark conditions and at room temperature. The off-state breakdown characteristics with varying L_{PSJ} ranging from 5 μm to 20 μm are illustrated in Figure 4.18 (a). V_{gs} is set at -15V, which guarantees the devices are fully turn-off. The relationship between BV and L_{PSJ} of fabricated PSJ HFETs is presented in Figure 4.18(b). The BV of fabricated PSJ-on-Sapphire substrate at Sheffield and PSJ HFETs-on-Si substrate provided by POWDEC.K.K are also shown in Figure 4.18 (b).

It can be found that:

1. The BV of PSJ HFETs increases with PSJ (L_{PSJ}) length.

2. The fabricated PSJ HFETs on Si substrate initially increase with L_{PSJ}, but then gradually saturates. However, BV for fabricated PSJ HFETs-on-Sapphire devices increases linearly with L_{PSJ} and the BV for L_{PSJ}=15 μm and 20 μm is much higher than that on Si substrate. This trend is identical to that obtained from PSJ hybrid diodes. This is due to the vertical BV limit of the GaN buffer grown on the Silicon substrate. GaN buffer thickness utilised in Sheffield is around 4 um.

3. Compared with the BV for PSJ HFETs from POWDEC (around 730V for L_{PSJ} =15 μm), the BV for Sheffield PSJ HFETs on Si substrate increased by approximately 50 %.

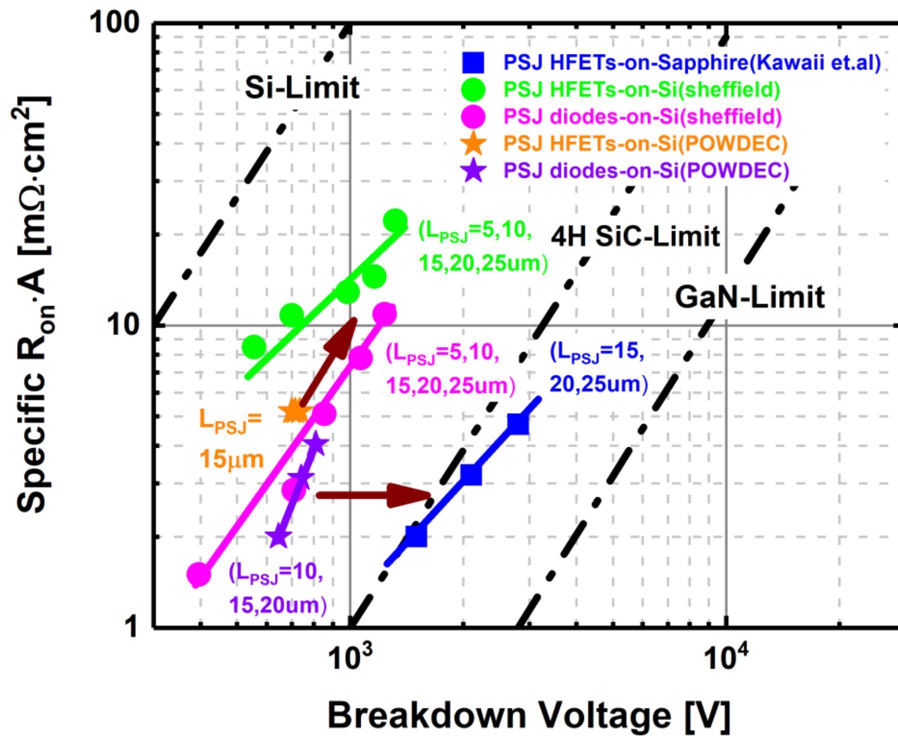


Figure 4.19 The relationship between the breakdown voltage and Specific Ron·A of the Sheffield PSJ-on-Si substrate, POWDEC PSJ-on-Si and PSJ-on-sapphire power devices from Kawaii et al. [69].

The relationship between the BV and Specific R_{on}·A for the Sheffield PSJ power devices on Si substrate is illustrated in Figure 4.19. The Specific R_{on}·A can be calculated based on the equation below:

$$R_{on} \cdot A = \frac{L_{SD}}{\rho_{V_{g=0}}}$$

Where L_{SD} is the distance between source to the drain, $\rho_{V_{g=0}}$ is the conductivity of the PSJ HFETs obtained from the I_{ds}-V_{ds} characteristics at V_g=0V. And L_{SD} is converted to L_{AC} (the distance of the Anode to cathode) in the PSJ diodes. Moreover, the trade-off relationship of POWDEC PSJ-on-Si power devices and PSJ-on-Sapphire power devices from Kawaii [69] are also plotted in the graph for comparison.

It can be found that:

1. Compared with the POWDEC PSJ-on-Si hybrid diodes, Sheffield PSJ-on-Si power hybrid diodes have a relatively higher breakdown voltage. However, the Specific $R_{on}\cdot A$ for the latter is slightly higher than that for the former. Similarly, the PSJ-on-Si HFETs from Sheffield have relatively higher BV and specific $R_{on}\cdot A$ than those from POWDEC.

2. PSJ-on-Sapphire power devices shown in [69] have a higher breakdown voltage than PSJ-on-Si power devices from Sheffield and POWDEC. Specifically, the BV for PSJ-on-Sapphire power devices with L_{PSJ}=20 μm is over 2100V. However, the BV for PSJ-on-Si power devices with L_{PSJ}=20 μm is around 1200V. Moreover, the Specific $R_{on}\cdot A$ of the PSJ-on-Sapphire power devices are similar to that of PSJ-on-Si power devices, representing that they are unsuitable for ultra-high voltage applications.

4.5. Summary

This chapter serves as the initial introduction to the presentation and discussion of the static on-state and off-state breakdown characteristics of the fabricated PSJ-on-Si HFETs and diodes at the University of Sheffield.

This chapter discusses the impacts of finger length and finger quantity on current handling capacity and the Specific $R_{on}A$ of PSJ hybrid diodes on Si substrate, which is crucial for the scalability of PSJ power devices. It is found that the specific on-state resistance increases with the length of the PSJ region. Moreover, the current handing capability increases with the finger quantity.

Furthermore, the effects of temperature on I-V characteristics are also evaluated. When the temperature rises, the current density of the PSJ hybrid diode tends to decrease. The drop in current density of the PSJ hybrid diode at high temperatures is caused by the reduction of the 2DEG carrier mobility caused by polar-optical-phonon scattering. However, the current can be further scaled up with increase in the length of the devices through using the thick metals, such as the Copper in the process.

The breakdown voltages of Sheffield PSJ hybrid diodes and HFETs are 20% and 50%, respectively, higher than those of POWDEC PSJ-on-Si power devices due to the high-resistivity C-doped GaN buffer layer, improving the vertical voltage withstanding capability. Moreover, it is also found that the BV of PSJ HFETs and diodes initially increases with PSJ (L_{PSJ}) length but then gradually saturates. This is because the GaN buffer grown on the Si substrate limits the breakdown voltage of PSJ HFETs or hybrid diodes.

In this chapter, the correlation between the breakdown voltage and Specific $R_{on}A$ for fabricated PSJ-on-Si power devices from the University of Sheffield is first published. Compared with the PSJ-on-Sapphire power devices reported in [69], Sheffield PSJ-on-Si power devices have a lower breakdown voltage at the given length of PSJ, which is due to the lower vertical breakdown voltage limit of the GaN buffer grown on the Si substrate.

Chapter 5. Investigation of Shift in Threshold Voltages of 1.2kV GaN Polarization Superjunction (PSJ) HFETs

The shift in threshold voltages (V_{th}) of 1.2 kV P-GaN ohmic-gate Normally-on Polarization Superjunction (PSJ) HFETs is reported for the first time in this chapter. Pulsed-mode measurement results of threshold voltage shifts under different gate stress biases are presented. A comprehensive analysis of threshold voltage shifts under different gate stress voltages and temperatures is discussed. Moreover, recovery processes are observed under positive and negative stress voltages. Temperature effects on the Vth are also evaluated through pulsed-mode measurements. The results also confirm that the current collapse is quite low in PSJ HFET. As a comparison, the Vth shift results from the Schottky gate PSJ HFETs are also reported in this chapter.

5.1. Threshold Voltage (V_{th}) shift in P-GaN gate PSJ HFETs

5.1.1. Introduction

The V_{th} shift phenomenon is widely existing in GaN power devices, and it determines the reliability and performance of devices. Several studies have demonstrated and discussed V_{th} shift mechanisms in the normally-off P-GaN gate HEMTs [95]–[98]. The main cause of the V_{th} shifts is the charge trapping/detrapping mechanism with typical acceptor trapping levels (Ea) in the GaN HEMTs reported in several studies. Bisi et al. [99]depicted a detailed summary of the catalogued deep levels for a range of activation energies, the

list of reference papers, the type of analysed samples, and one or more hypotheses on the origin of these traps as reported by various authors at the time of its publication. The spectrum of these defects is rather large and varies depending on many factors, such as growth conditions etc. [99]. Moreover, they also reported the typical trap levels of E_a from 0.14eV to 0.86eV[99].Moreover, Kuzuhara et.al[100](E_a=0.28eV to 0.64eV), Alberto.M.Angelotti et.al [101](E_a=0.36eV to 0.68eV) and Gaudenzio Meneghesso et.al [102](E_a=0.099 eV to 0.631eV) reported the very similar range of trap levels value.

This chapter reports the V_{th} shift mechanisms in the normally-on 1.2kV P-GaN ohmic gate GaN PSJ HFETs through pulsed-mode measurements. V_{th} shifts caused by the charge trapping mechanisms under positive and negative gate stress voltages are discussed separately. Recovery processes are also presented with varying measuring times. Moreover, the current collapse in PSJ HFETs is evaluated through the pulsed I_d-V_{ds} characteristics. Finally, the shifts in V_{th} as a function of temperature are also discussed.

5.1.2. Device structure and dimensions

The devices under test (DUTs) are 1.2 kV ohmic gate PSJ HFETs on Sapphire. The P-GaN ohmic gate is designed for charging/discharging 2DHG during the off-state/switching as well as depleting 2DEG under strong negative bias. Figure 5.1 illustrates the cross-section of the GaN PSJ HFETs. PSJ structures (u-GaN/AlGaN/u-GaN) are capped with the P+GaN ohmic gate contact. The Mg doping concentration of the P+ GaN and P-GaN layers is 1e20 cm^{-3} and 1e19 cm^{-3}, respectively. Their thicknesses are 43nm and 30nm, respectively. Moreover, the thickness of the top and bottom u-GaN layers are 20nm and 800nm, respectively. The AlGaN thickness is 25nm with an Al content of 0.3. The gate widths of DUTs are 1mm, and cross-sectional dimensions are shown in Figure 5.1.

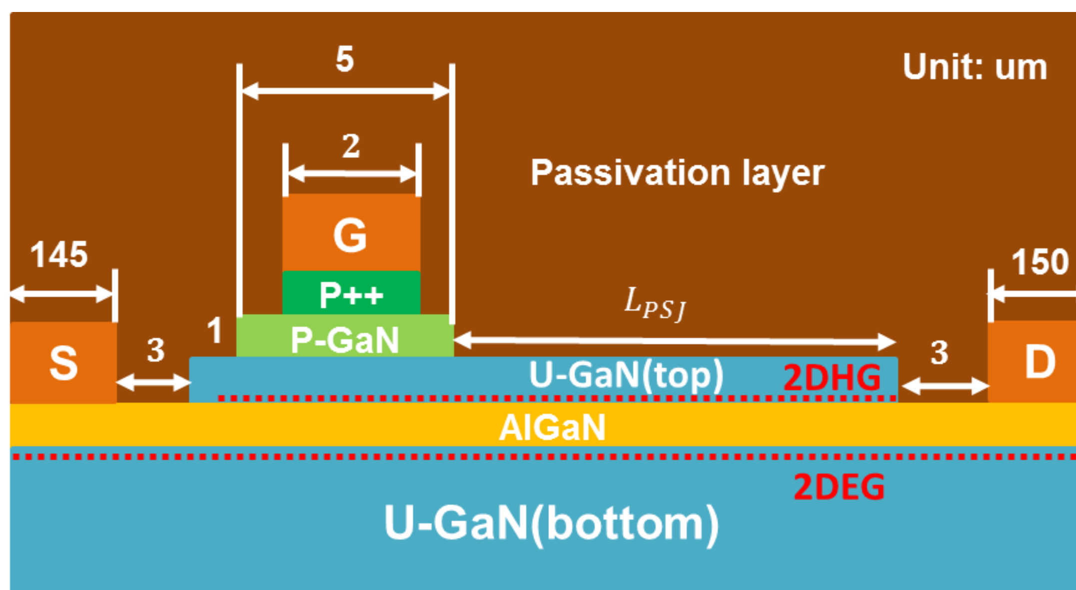
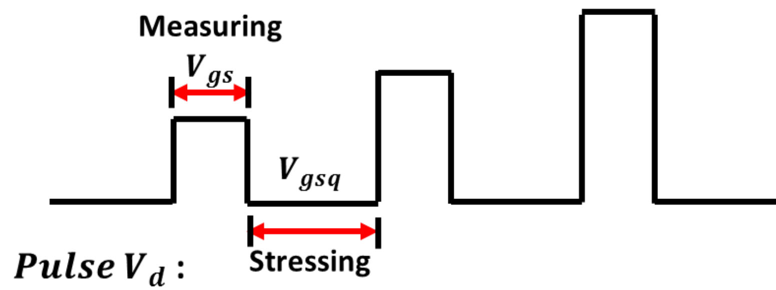


Figure 5.1 The Cross-section schematics of P-GaN ohmic gate PSJ HFETs.

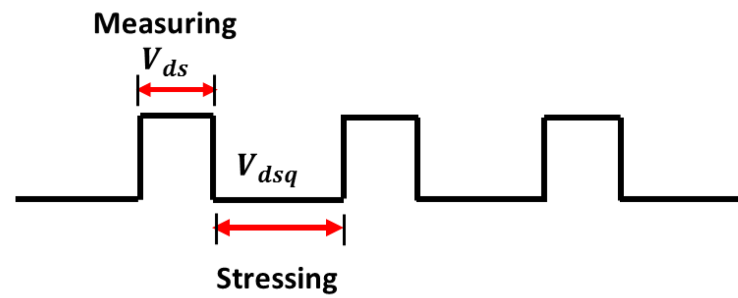
5.1.3. Pulse-mode measurement setup and conditions

Pulse-mode I_d-V_{ds} and transfer measurements are carried out using the Keysight B1500A device curve tracer at room temperature and under dark conditions. In a typical pulsed transfer measurement, during the stressing period, a constant voltage is applied to the gate. During the measuring period, pulsed gate voltages of increasing magnitude (V_{gs}) are applied in sequence at the gate, and the I_{ds}-V_{gs} curves are extracted during the measuring period. Under these conditions, applied drain voltages are pulsed voltages of fixed magnitude (V_{ds}). Typical test waveforms are shown in Figure 5.2(a). The pulse width is set at 0.5ms (limited by the equipment), the duty cycle is 0.1%, the quiescent drain voltages (V_{dsq}) are held at 0V, and Vds is 1V minimises the self-heating effects. The quiescent gate voltage (V_{gsq}), which is also defined as the stress voltage, is varied. The pulsed transfer measurement setup and conditions are shown in Figure 5.2 (a).

$Pulse\ V_g$:

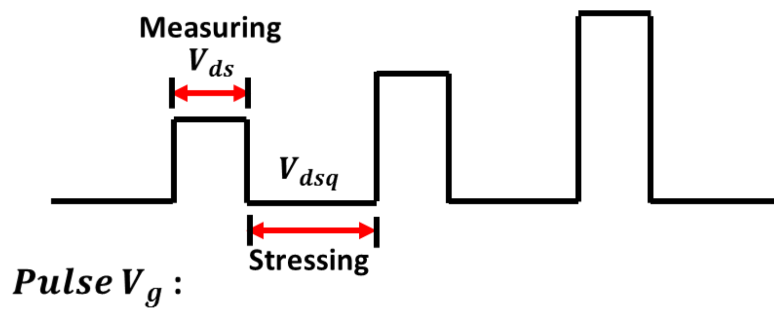


$Pulse\ V_d$:

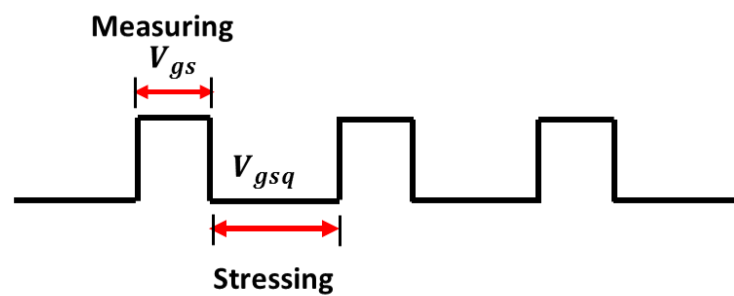


(a)

$Pulse\ V_d$:



$Pulse\ V_g$:



(b)

Figure 5.2 The measurement conditions and setup for (a) pulsed-transfer measurements; and (b) pulsed Ids-Vds characteristics for analysing the Vth shifts in PSJ HFETs.

5.1.4. V_{th} shift under positive gate stress voltages

Due to the nature of the field shaping and charge balance, PSJ HFETs with L_{PSJ} equal to 15um can achieve a breakdown voltage over 1200V[70]. For this study, we utilised small devices with similar dimensions (except in cases with different lengths of PSJ) to investigate the Vth shift. The gate leakage current is a typically observed reverse PiN junction current when the gate is negatively biased. Conversely, when the gate is positively biased, the current increases due to hole injection when the bias is higher than 3.4V, as shown in Figure 5.3.

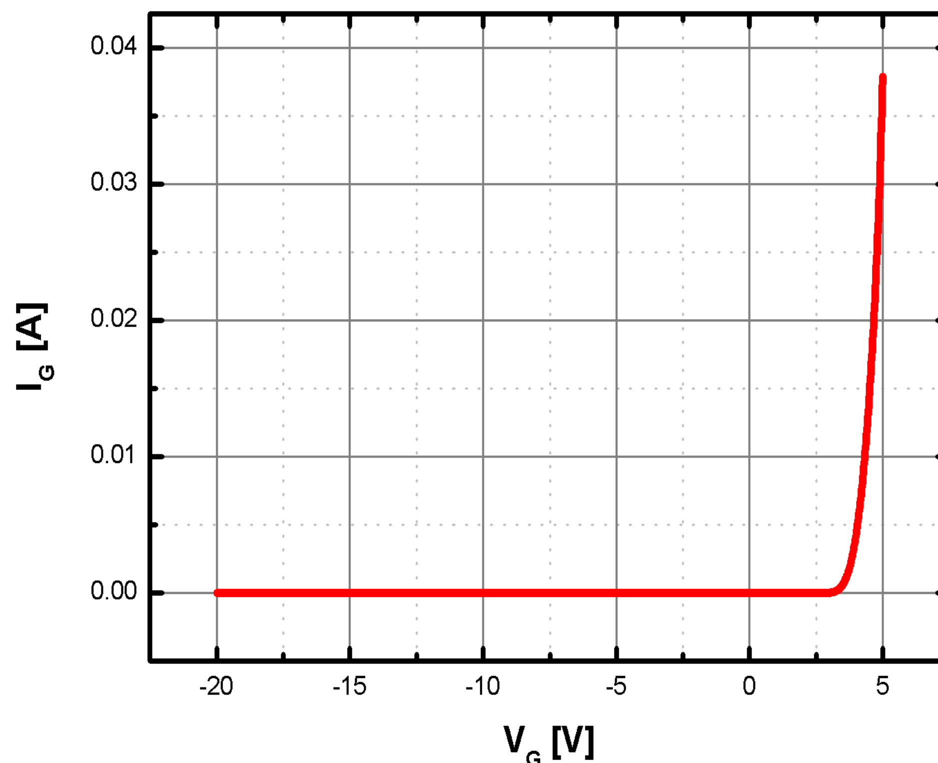
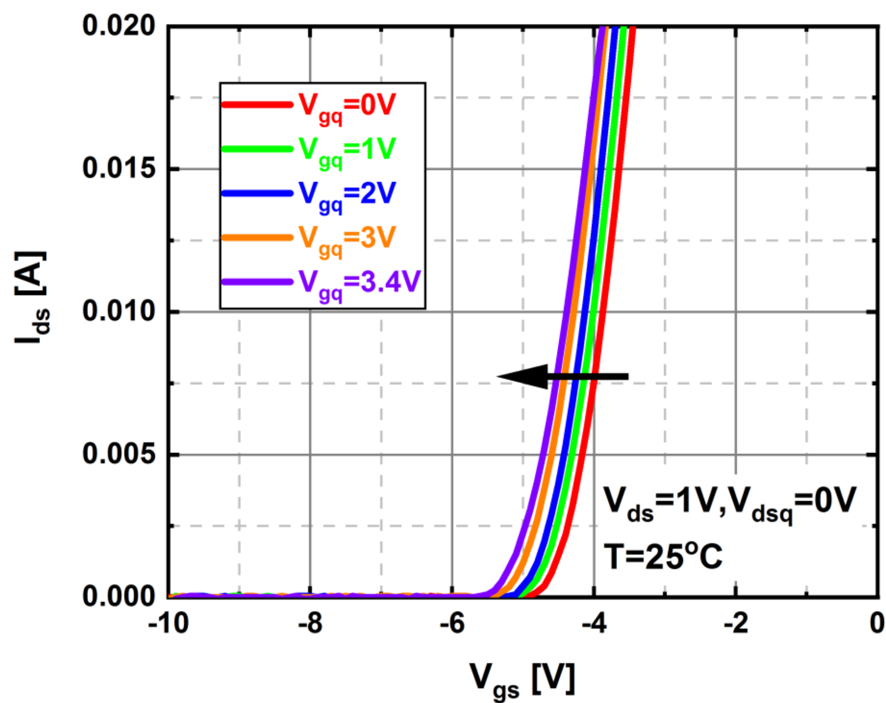


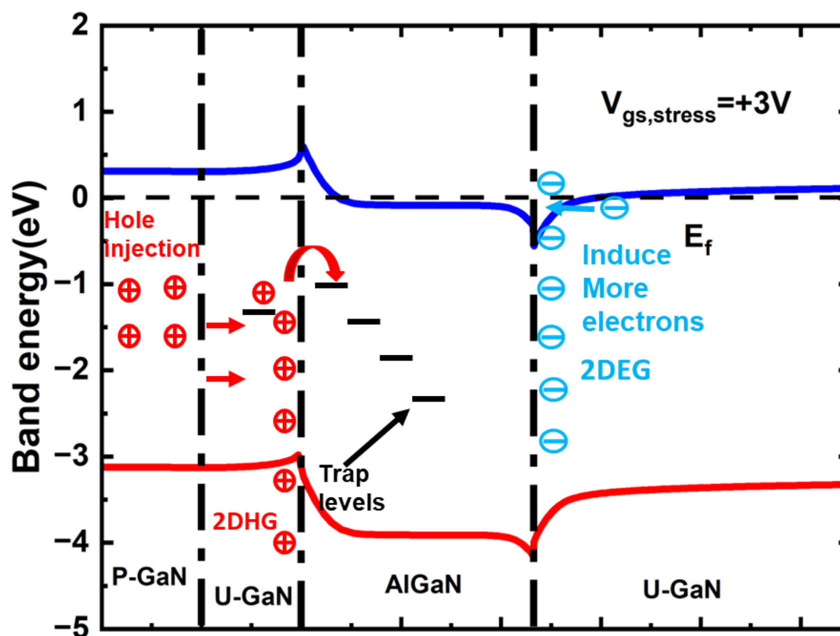
Figure 5.3 Typical Gate Current characteristics (Igs-Vgs) of the PSJ HFETs measured at Vds=1V.

We considered PSJ HFET with L_{PSJ}=15um, and the measured Vth is -5V when no gate stress is applied. As shown in Figure 5.4 (a), negative V_{th} shifts in the

PSJ HFETs can be observed under positive stress gate voltages from 0V to



(a)



(b)

Figure 5.4 (a)Typical pulsed transfer characteristics of PSJ HFETs measured at V_{ds}=1V and quiescent V_{dsq}=0V, under different stress gate bias V_{gsq}, ranging from 0V to 3.4V.(b) the trapping mechanisms under positive gate stress

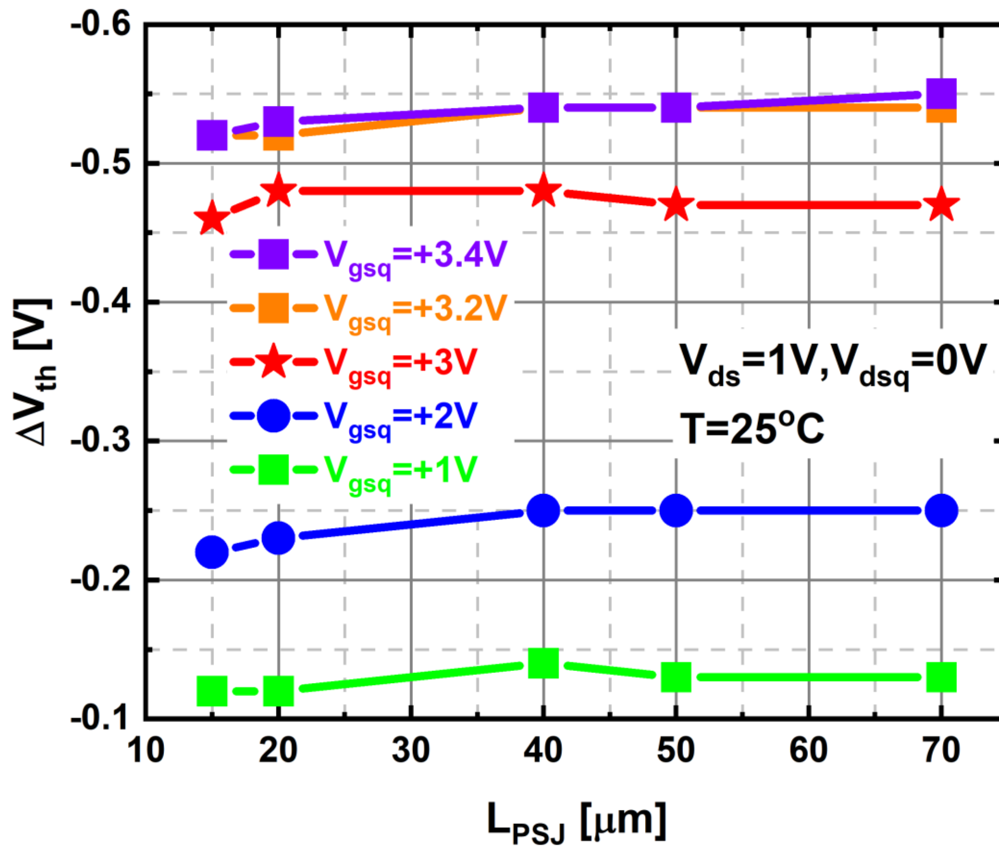


Figure 5.5 Vth shift value (ΔVth) with different L_{PSJ} =15um,20um,40um,50um and 70um.

+3.4V. The trapping mechanisms in the energy band diagram under the positive gate stress is illustrated in Figure 5.4(b). Holes are injected from the gate and P+GaN layer. Some holes are captured by the traps located in the top u-GaN layer or accumulated at the heterointerface of U-GaN/AlGaN due to the low mobility of 2DHG. Some of these could potentially move across the GaN/AlGaN band barrier, enter into the AlGaN layer, and be trapped by the hole traps. Therefore, more electrons are induced for charge neutrality, causing a rise in 2DEG. When the positive gate stress voltage is removed, the induced electrons are not reduced immediately, thus causing a negative V_{th} shift in a

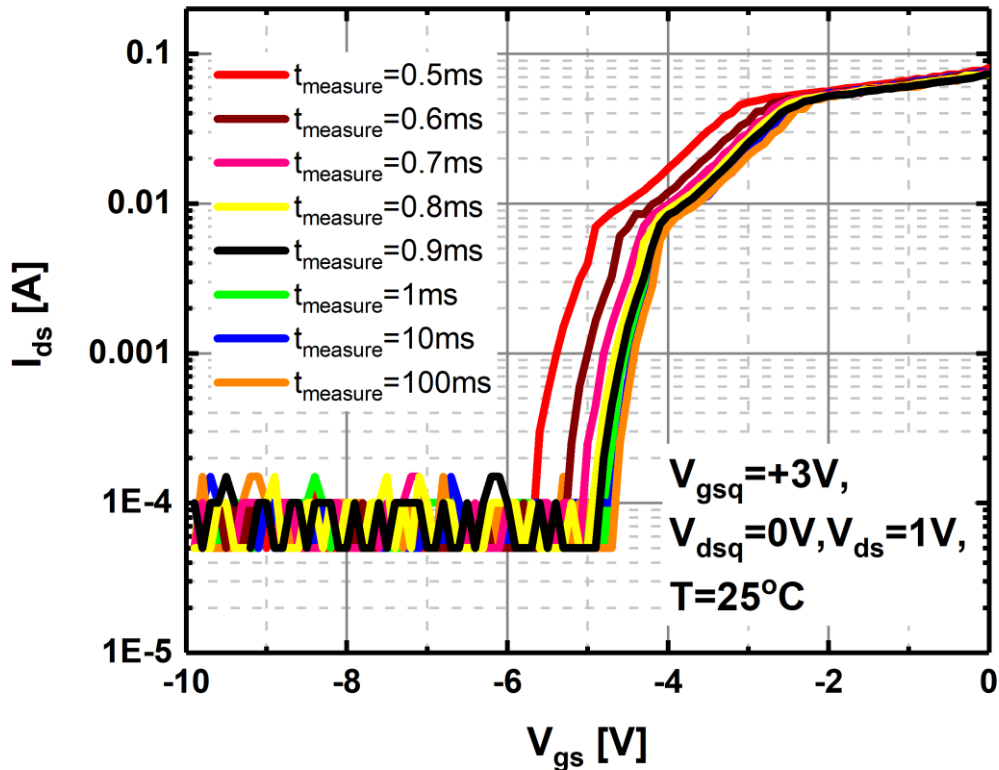


Figure 5.6 Typical pulsed transfer characteristics of PSJ HFETs were measured at V_{ds}=1V and quiescent V_{dsq}=0V. The measuring time ranges from 0.5ms to 100ms, and the stressing time is fixed at 500ms under gate stress voltages (a) V_{gsq} =+1V and (b) V_{gsq} =+3V

manner similar to those from normally-off P-GaN gate AlGaN/GaN HEMTs[95]–[98].

The relationship between the Vth shift value (ΔV_{th}) and different L_{PSJ} (from 15um to 70um) is presented in Figure 5.5. The V_{th} shift mechanisms of them under positive gate stress are identical to the L_{psj}=15um. Despite the fact that 2DHG exists at most of the drift regions, the heterointerface of top u-GaN/AlGaN along with the L_{PSJ}, the injected holes are mainly concentrated under the gate region and involved in the Vth shift, which is possibly due to the low mobility of 2DHG (lower than 16 cm^2/V-sec)[85].

The recovery process is observed through varied measuring period time presented in Figure 5.6. In these tests, the stressing time is fixed at 500ms, which is adequate to ensure that the holes are completely trapped. It can be observed that, with the increase of the measuring times, the positive Vth shifts gradually saturate over time. The mechanisms during the recovery process can be explained as follows: the holes are injected and trapped in the AlGaN layer under the positive stress voltages during the stressing period. However, during the measuring period, the gate voltages transit from positive biases (the stressing period) to negative biases (the measuring period). Thus, the trapped and accumulated holes are de-trapped because of the applied reverse bias. Therefore, with the increase in measuring time, more holes are released from the AlGaN layer, reducing the density of 2DEG. The positive V_{th} shifts gradually saturate because the trapped holes are fully de-trapped during the relatively long recovery period. Typical pulsed I_d-V_{ds} characteristics measured under different positive gate stress voltages to evaluate the current collapse due to the V_{th} shift are as shown in Figure 5.7. In these tests, during the stressing period, gate stress voltages of varying magnitudes (V_{gsq}) are applied to the gate and the applied drain voltage V_{dsq} is zero. During the measuring period, the V_{gs} is fixed at a steady value, pulsed drain voltages of increasing magnitude (V_{gs}) are applied to the drain and I_d-V_{ds} are extracted during the measuring period. The detailed measurement conditions are shown in Figure 5.2(b): The V_{gs}

maintains at 3V, and the stress gate voltages (V_{gsq}) range from 0V to 3V. The quiescent drain voltages (V_{dsq}) is 0V.

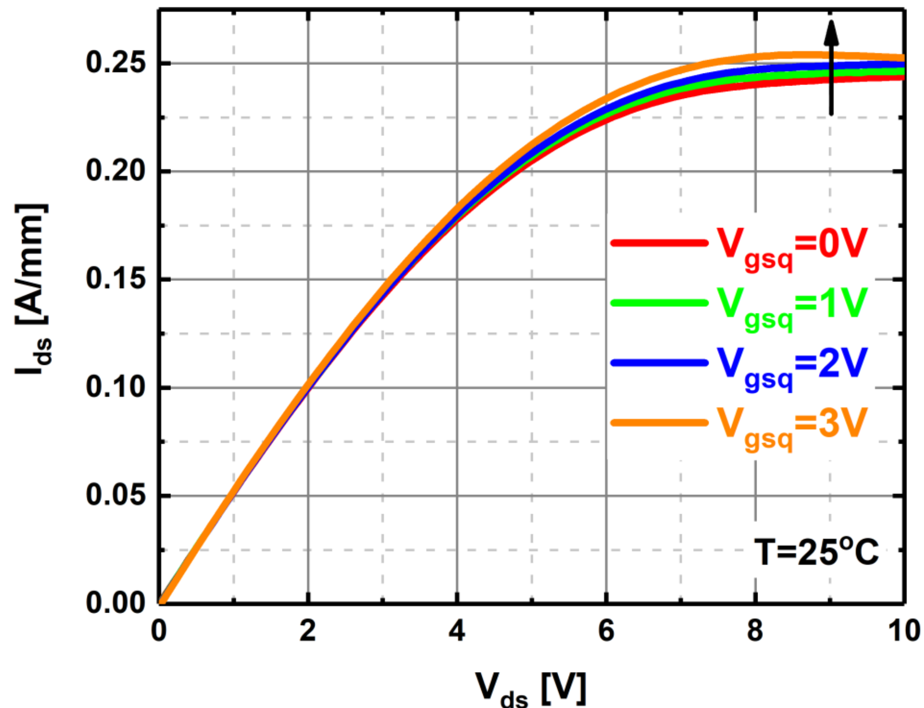


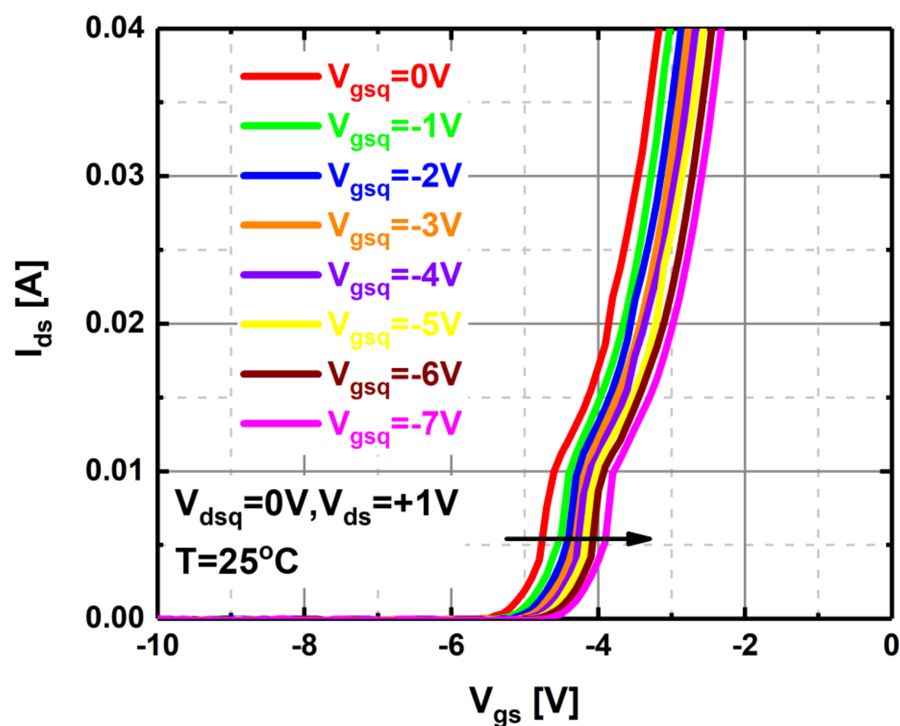
Figure 5.7 Typical pulsed Id-Vds characteristics of PSJ HFETs were measured at Vgs=3V with different stress gate voltages (Vgsq), ranging from 0V to 3V.

The positive gate stress voltages have not induced any significant differences in the on-state resistances in the linear region. Under the low drain voltage, the trapping is challenging to occur laterally from gate to drain. However, under the positive gate stress, it is more possible to happen under the gate, causing holes injection, trapping effects and negative V_{th} shifts. This is why no variation of on-state resistance but a marginal increase in the saturation Id is observed. This interpretation of this phenomenon is also reported in [95]. The I_d variation at the saturation region is around 0.065A/mm in[95], but it is only 0.02A/mm of PSJ HFETs (both measured at V_{ds}=6V and V_{gsq}=+3V) presented in Figure 5.7.

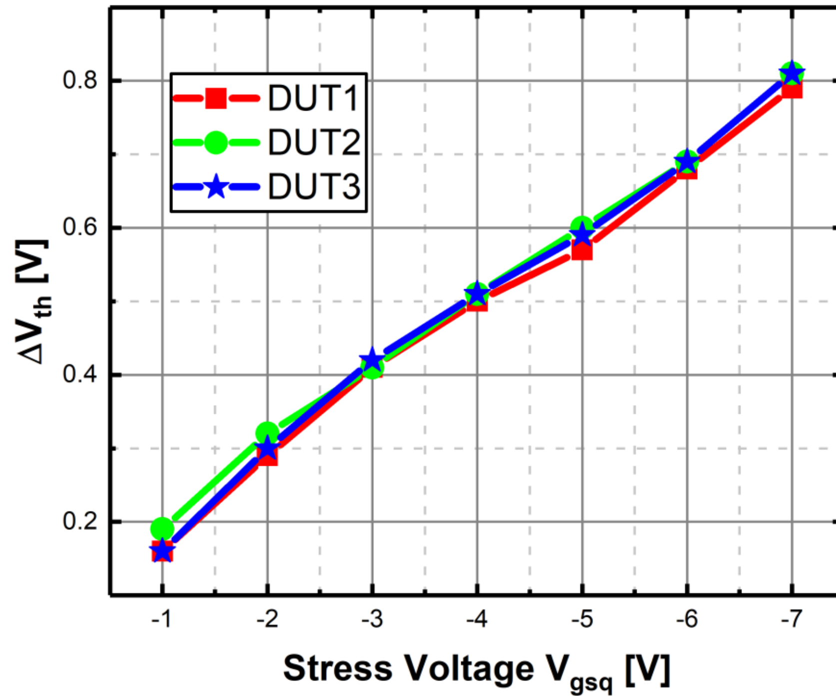
Compared to the P-GaN gate HEMTs in [95], PSJ HFETs show similar results but much lower magnitudes. The marginal Id increase is negligible in the PSJ HFETs, consistent with the results reported in [69], which show minimum current collapse.

5.1.5. Vth shift under negative gate stress voltages

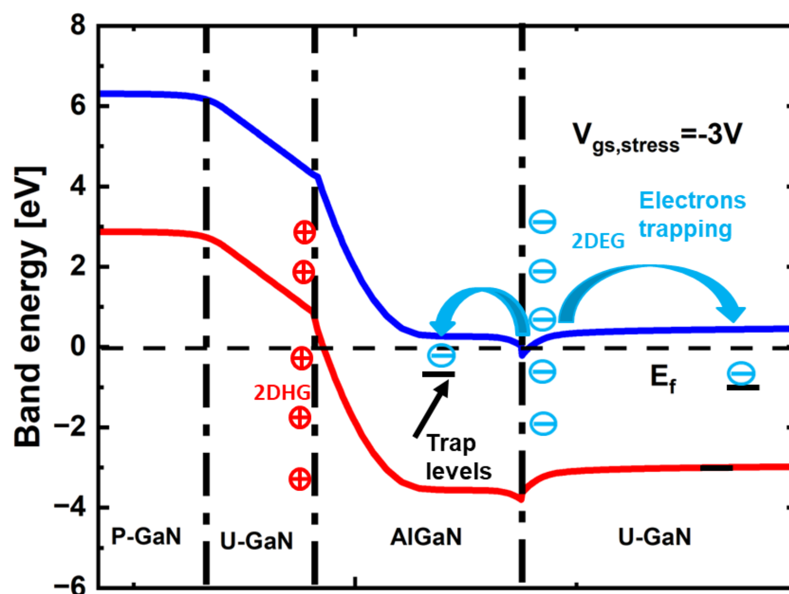
Pulsed transfer characteristics under different negative gate stress voltages are shown in Figure 5.8 (a). The positive Vth shifts with the increase in negative gate stress voltages (from -7V to 0V) present a reverse trend to the positive gate stress voltages test. The trapping mechanisms under the negative gate stress are illustrated in Figure 5.8(c). Similarly, the electron trapping process is also displayed in the band diagram at $V_{gs,stress}$=-3V. Under the negative gate stress,



(a)



(b)



(c)

Figure 5.8. (a) Typical pulsed transfer characteristics of PSJ HFETs were measured at V_{ds}=1V and quiescent V_{dsq}=0V under negative stress gate bias V_{gsq}, ranging from 0V to -7V. (b) the V_{th} shifts as a function of varying gate stress voltages in PSJ HFETs(C)The trapping mechanisms under negative gate stress.

some of the electrons are trapped by the GaN buffer traps. Some of the electrons

can potentially cross the AlGaN/GaN barrier and be captured by the electron traps in the AlGaN layer. The electron trapping causes the reduction of the 2DEG, resulting in the positive Vth shift when the gate stress voltage is removed. The magnitude of the Vth shift value shows a linear relationship with the magnitude of the negatively increasing stress voltages, as shown in Figure 5.8 (b).

The recovery processes at the off-state (V_{gsq} below -5V) during the stress period are presented in Figure 5.9. The measurement conditions are identical to the previous test shown in Figure 5.9 but with different gate stress voltages. As

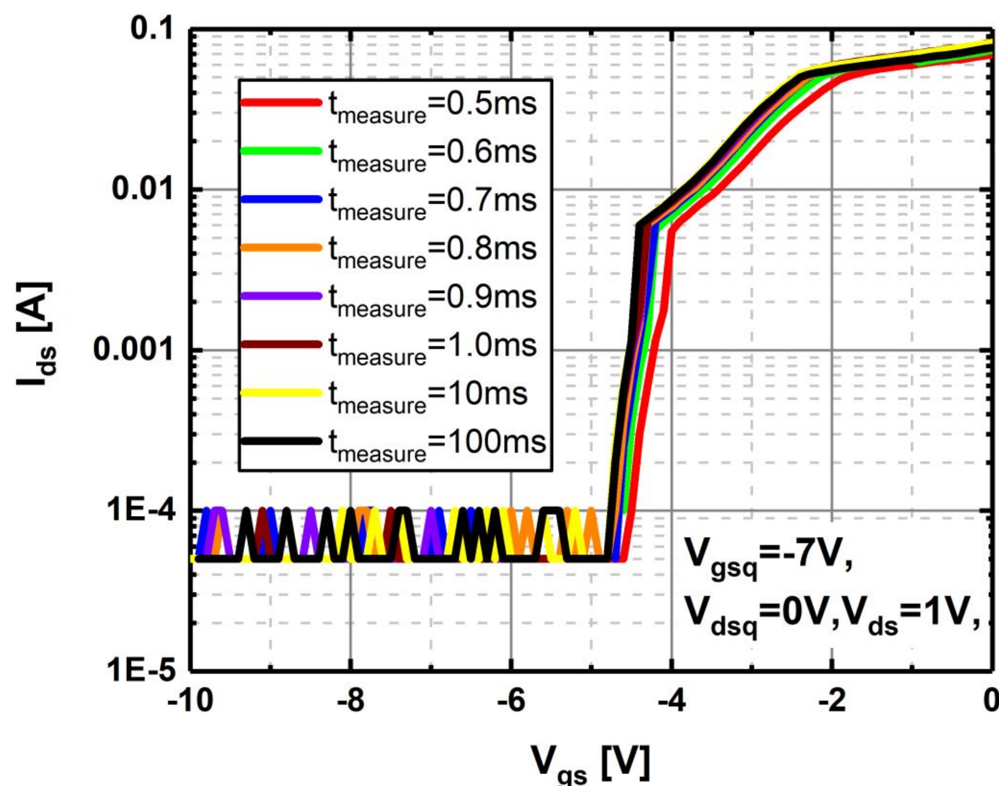


Figure 5.9 Typical pulsed transfer characteristics of PSJ HFETs measured at V_{ds}=1V and quiescent V_{dsq}=0V. The measuring time ranges from 0.5ms to 100ms, and the stressing time is fixed at 500ms under gate stress voltages V_{gsq}=-7V.

shown in Figure 5.9, negative V_{th} shifts gradually saturate when the measuring times increase from 0.5ms to 100ms at V_{gsq}= -7V. It can be explained as follows: During the negative stress period, electrons are captured by the traps in AlGaN or buffer layer. During the measurement, the gate voltages are less negative than V_{gsq}. Therefore, the electrons are de-trapped from the trap states in the AlGaN or bottom u-GaN buffer layer. With the increase in the measuring time, more electrons are de-trapped from the AlGaN or buffer layer, causing an increase in electrons in the 2DEG channel and accompanying the negative Vth shift. With the measuring time increasing further, all the trapped electrons saturate, and so do the Vth shifts.

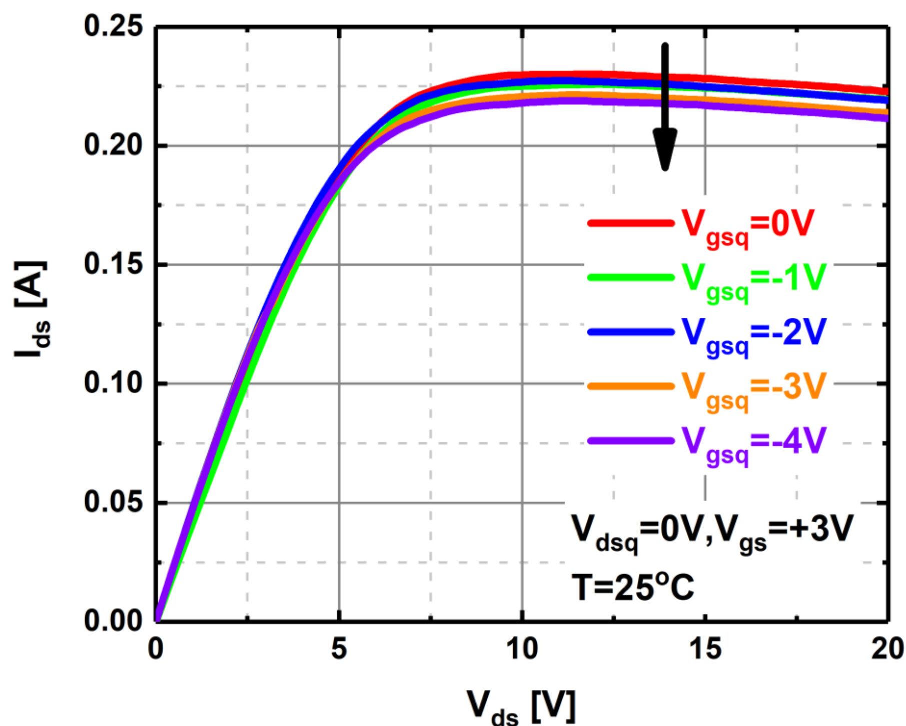


Figure 5.10 Typical pulsed Id-Vds characteristics of PSJ HFETs were measured at Vgs=3V with different stress gate voltages (Vgsq), ranging from 0V to -4V.

Similarly, pulsed I_d-V_{ds} characteristics are measured under negative gate stress voltages ranging from 0V to -4V, shown in Figure 5.10. V_{dsq} is kept at 0V. The measurement conditions are shown in Figure 5.2(b). Like the positive gate stress tests, the negative stress gate voltages do not cause any variation in the on-state resistance in the linear region. Due to the current collapse, the Id shows a slight downward trend in the saturation region with the negatively increasing gate stress voltages. Furthermore, these marginal variations also confirm the current collapse is negligible in PSJ HFETs.

5.1.6. The Vth shifts under positive stress voltages as a function of temperature

Pulsed transfer characteristics are measured under different temperatures, ranging from 20°C to 150°C. The gate stress voltages are set at 3V, and the steady V_{ds} is 1V (V_{dsq} is 0V). The V_{th} shift values are extracted from each measurement of three identical devices under different temperatures at a current density of 10mA/mm, as shown in Figure 5.11.

Initially, it can be observed that the magnitude of $|\Delta V_{th}|$ increases from 20°C to 100°C. However, with a further rise in temperature, $|\Delta V_{th}|$ gradually saturates[97][109]. This trend is similar to the results reported in [97], [98]. These V_{th} shift mechanisms in PSJ GaN HFETs can be explained as follows: at the start, an increase in temperature from 20°C to 100°C results in more holes being generated due to the rise in the activation of Mg. Thus more holes are

trapped and accumulated in the AlGaN layer, causing the negative V_{th} shifts at 100°C. However, with the temperature increasing further, although the hole density increases, the de-trapping behaviour becomes more dominant, compromising the further increase of the V_{th} shift value.

Additionally, another thermal mechanism of the 2DEG that can be responsible for this trend is mentioned in [97]: more 2DEG electrons are thermally activated

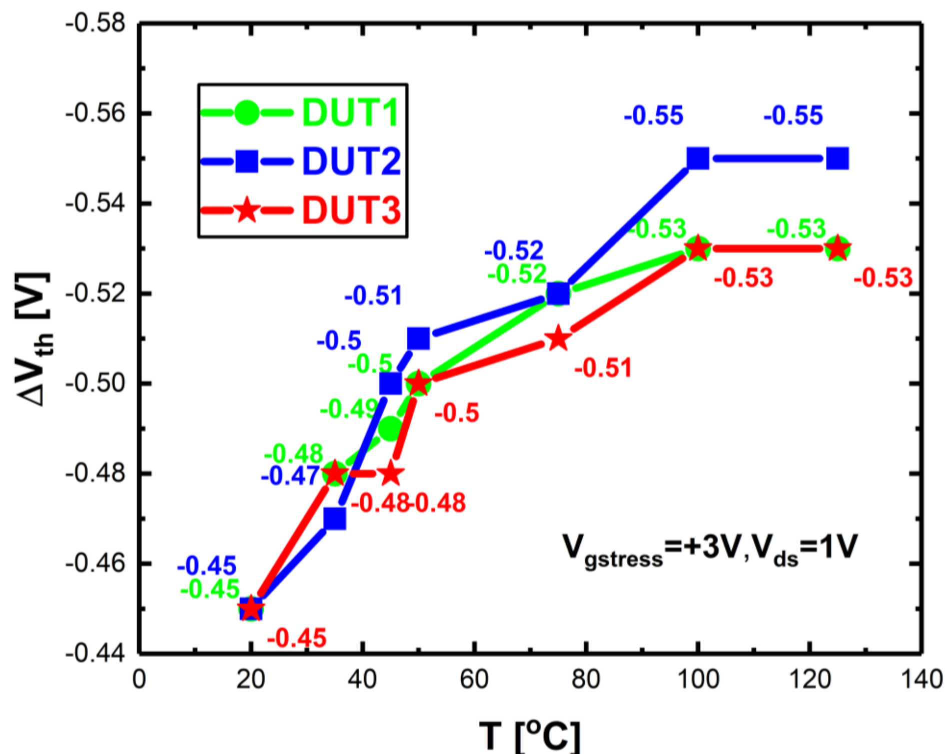


Figure 5.11 the Vth shifts as a function of different temperatures in PSJ HFETs, the gate stress voltage is +3V, and the steady Vds is 1V (Vdsq is 0V). The Vth is extracted at 10mA/mm.

from the channel states into the AlGaN layer with the temperature rise. This mechanism causes the positive V_{th} shifts, compensating for the negative V_{th} shifts caused by hole-trapping processes. Therefore, the $|\Delta V_{th}|$ saturates when the temperature increases above 100°C.

5.2. Threshold Voltage (V_{th}) shift in Schottky gate PSJ HFETs

The Vth shift in Schottky gate PSJ HFETs is also studied as a comparison. The samples were fabricated in the Fab Lab at the University of Sheffield.

5.2.1. Devices structures, parameters and fabrication details

Figure 5.12 (a) depicts the dimensions and cross-section of the manufactured Schottky-gate PSJ HFETs. The top and bottom u-GaN layers have 20 nm and 800 nm thicknesses, respectively. With an Al mole fraction of 0.23, the AlGaN thickness is 47 nm. The doping density of Mg is 1e20 cm^{-3} and 1e19 cm^{-3} in the P^{+}GaN and P-GaN layers, with thicknesses of 3nm and 17nm, respectively. Source and Drain electrodes (Ti/Al/Ni/Au) were deposited on the AlGaN layer and formed the ohmic contact with the 2DEG through thermal annealing at 800°C in N_2. P+ GaN ohmic contact (Ni/Au) is deposited on the P+GaN layer, defined as the base contact and assists in transporting holes. The additional metallisation (Ti/Au) connects the base and source contact. Figure 5.12 (b)

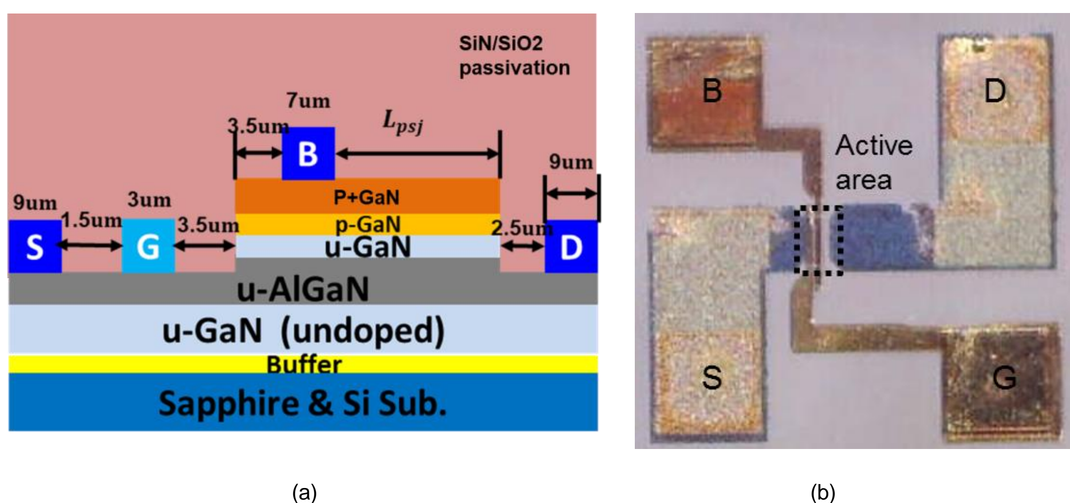


Figure 5.12 (a) The schematics cross-section and (b) the photograph of Schottky-gate PSJ HFETs.

presents the top view of the photograph of the fabricated PSJ Schottky-gate HFETs.

5.2.2. Vth shift under positive and negative gate stress voltage

Following the similar pulse-mode measurement setup and conditions mentioned, the V_{th} shift is measured under the positive and negative gate stress voltage.

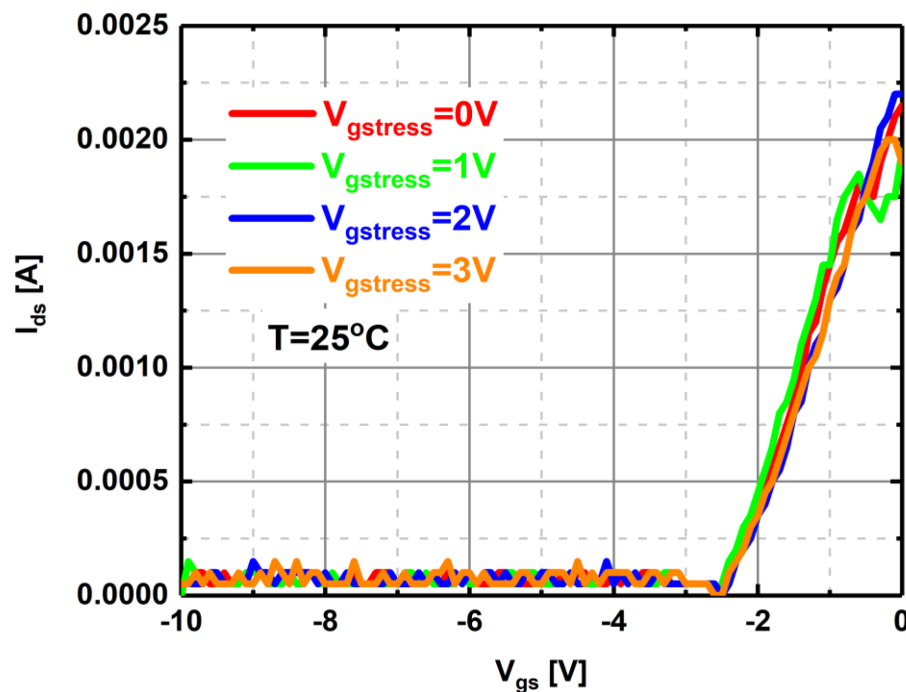


Figure 5.13 The pulsed transfer characteristics of PSJ schottky gate HFETs measured at Vds=1V and quiescent V_{dsq}=0V, under different stress gate bias $V_{gstress}$, ranging from 0V to 4V.(b) the Vth shift as a function of varying gate stress voltage in PSJ HFETs, V_{th} is extracted at 1mA/mm.

According to Figure 5.13, no V_{th} shift in the PSJ Schottky gate HFETs under positive stress gate voltages can be observed. This phenomenon is inconsistent with the results shown in P-GaN gate HFETs when the positive gate stress voltage is applied [97], [98]. This is because there aren't any injected holes from

the Schottky gate. Hence there isn't any Vth shift when the gate is under positive gate stress voltage.

V_{th} shift mechanisms are also analysed under the same conditions on these devices but with negative gate stress voltages. The pulsed transfer characteristics at the various negative gate stress voltages are displayed in Figure 5.14. Positive V_{th} shift with the negative gate stress voltage increase can be observed. Three identical devices are measured under the same conditions. We can find that the maximum average ΔV_{th} is +0.96 V at $V_{gstress}$=-4V. This phenomenon is similar to P-GaN gate PSJ HFETs. The shift mechanisms are also the same.

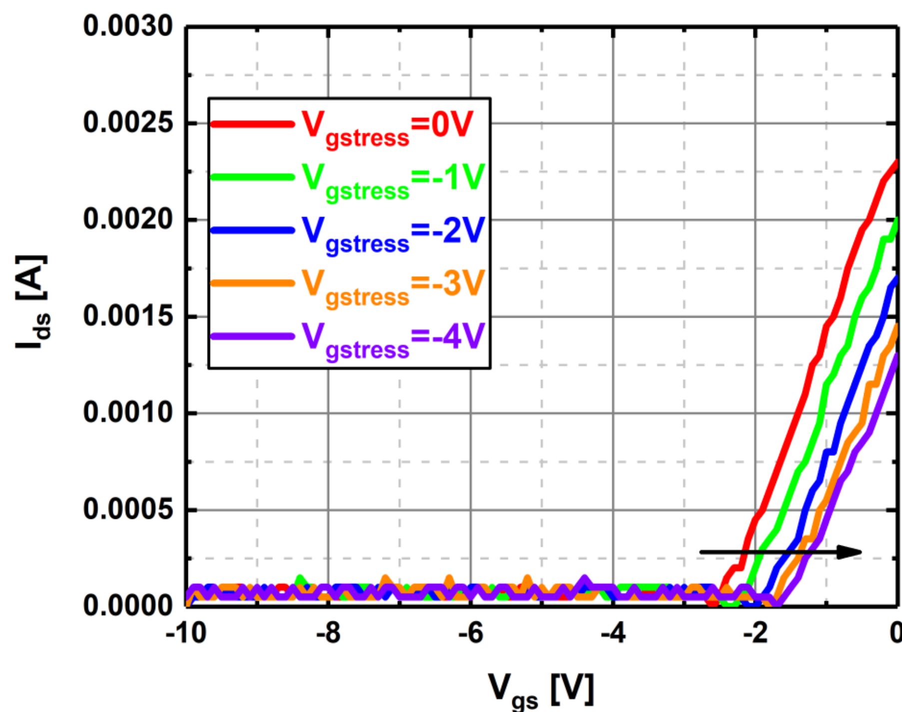


Figure 5.14 The pulsed transfer characteristics of PSJ schottky gate HFETs measured at Vds=1V and

5.3. Summary

Vth shift mechanisms in normally-on GaN PSJ HFETs through pulsed I_d-V_{ds} and transfer characteristics measurements under the positive and negative gate stress voltages are reported for the first time. Under positive gate stress voltage conditions, more holes are injected into the AlGaN layer or u-GaN/AlGaN hetero-interface and then trapped and accumulated by the hole trap states. Thus, the trapped or accumulated holes cannot escape immediately when the reversed negative gate voltages are applied during the measuring period, inducing more electrons in the 2DEG channel, and causing negative V_{th} shifts. Despite the presence of the 2DHG extended beyond the gate, the injection of holes is restricted to the gate contact regions. When the negative gate stress voltages are applied, electrons are trapped by the electron trap states in the AlGaN layer or GaN buffer layer, causing the positive V_{th} shifts. The Vth shifts are also presented during the recovery processes by varying the measuring times. With the increase in the measuring times, more trapped electrons and holes will be released, causing the Vth shifts. Moreover, from the pulsed I_d-V_{ds} characteristics, positive and negative gate stress voltages cause a much lower magnitude of the differences in the saturation current than P-GaN gate HEMTs, indicating that current collapse is significantly reduced in PSJ HFETs.

Furthermore, the temperature effects on the V_{th} shifts under the positive gate stress voltages are also discussed. $|\Delta V_{th}|$ increases when the temperature rises

from 20°C to 100°C. Thermally-activated holes and 2DEG electrons cause this phenomenon. As the temperature increases, more holes are trapped and accumulated in the AlGaN layer, causing the negative V_{th} shifts. However, the strengthened recovery processes cause the positive V_{th} shifts, which compensate for the negative V_{th} shifts caused by the enhanced holes injection and accumulation processes, which induce the saturation of the $|\Delta V_{th}|$.

Compared with the P-GaN gate PSJ HFETs, the V_{th} shift in Schottky gate PSJ HFETs has different performances. There is no V_{th} shift when positive gate stress voltage is provided since no injected holes are present. However, a positive V_{th} shift is observed under the negative gate stress voltage.

Chapter 6. GaN Polarization Superjunction diode current saturation behaviour

In this chapter, the current saturation behaviour observed in AlGaN/GaN diodes, PSJ hybrid diodes and PSJ PiN diodes fabricated on a sapphire substrate is discussed, and their operating mechanisms are highlighted. PSJ hybrid diodes and PSJ PiN diodes are 1.2kV capable power diodes.

6.1. Current saturation behaviour in conventional AlGaN/GaN diode

6.1.1. Device structures and Measurement results

AlGaN/GaN diodes have very similar device structures to the conventional AlGaN/GaN HEMTs, except that there is no gate structure. The schematic cross-section of the conventional AlGaN/GaN diode is presented in Figure 6.1. The cathode is composed of the metal stacks of Ni/Au and deposited on the AlGaN layer. And then, it forms the ohmic contact with 2DEG through rapid

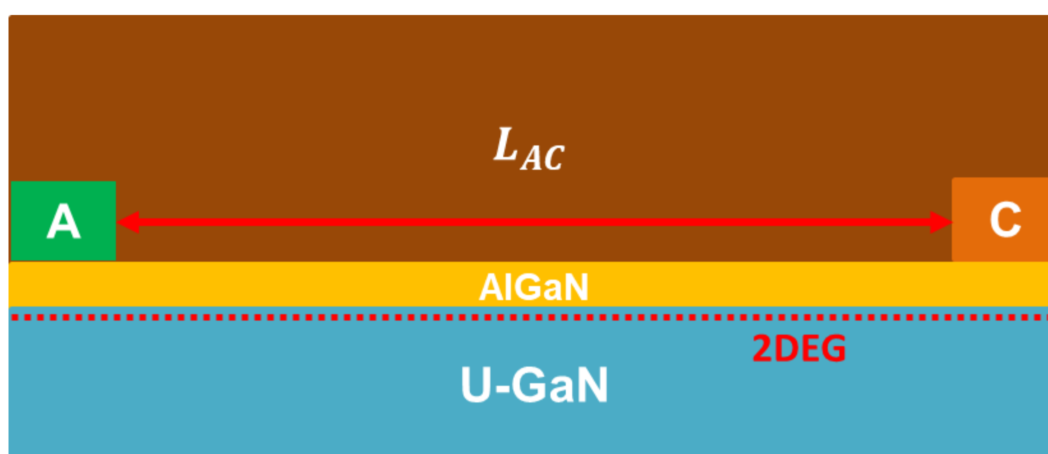
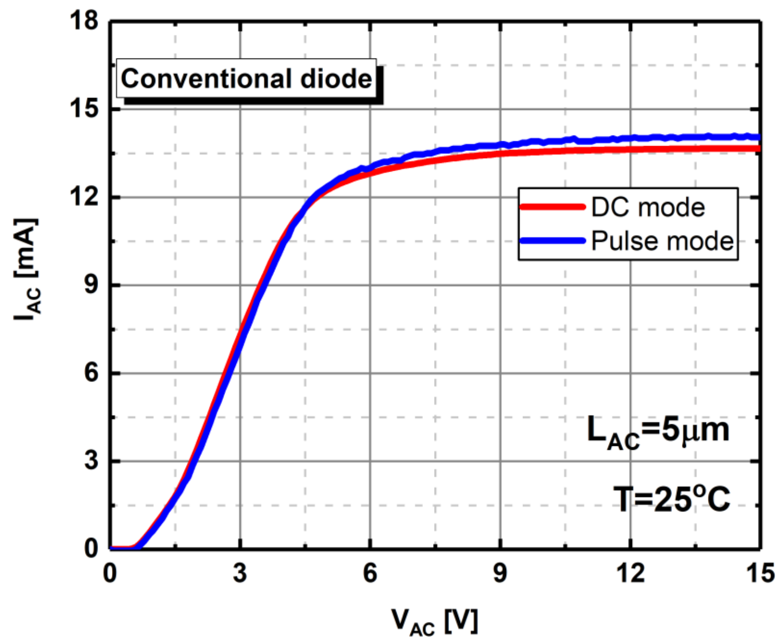
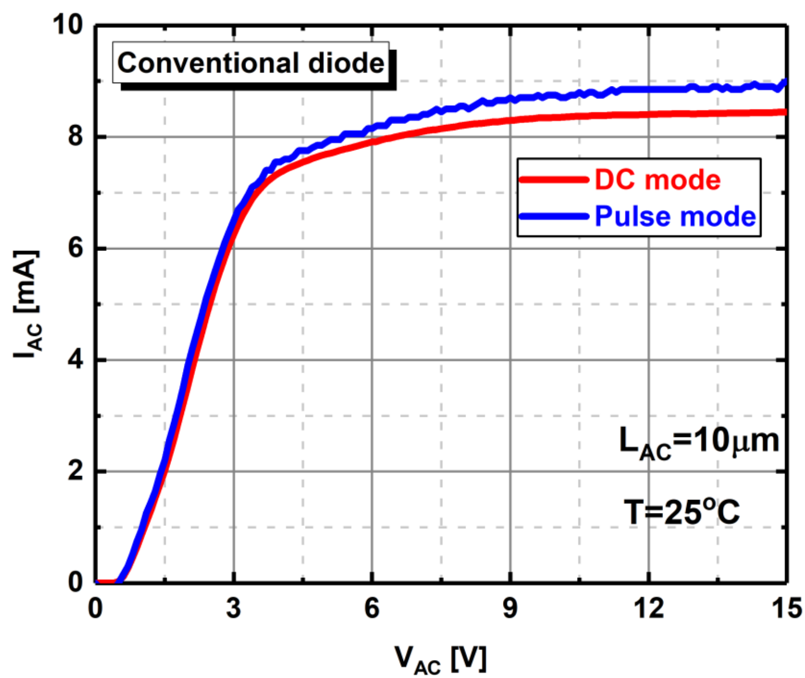


Figure 6.1 The schematic cross-section of conventional AlGaN/GaN diode.

thermal annealing (RTA). The condition is that 800°C in N_2 ambient for 1min.



(a)



(b)

Figure 6.2 The typical forward I-V characteristics of conventional AlGaN/GaN diode with(a)L_{AC}=5 µm and (b) L_{AC}=10 µm

The Anode composed of the metal stacks of Ni/Au was then deposited, forming the Schottky contact to the 2DEG. When the diode conducts forwardly, the

electrons flow from the Anode to Cathode through the 2DEG channel. Therefore, this diode's only carriers are electrons（2DEG）, indicating that it is a unipolar power device.

All these AlGaN/GaN power diodes are fabricated in the cleanroom fab lab in Sheffield.The widths of the test conventional AlGaN/GaN diodes are 50 μm. Their forward I-V characteristics with L_{AC}=5 and 10 μm are displayed in Figure 6.2, respectively. In this chapter, unless stated otherwise, the results are from measurements carried out via the B1500A Semiconductor Device Parameter Analyzer and processed under dark conditions and at room temperature. Pulse-mode tests are also presented in Figure 6.2, with a pulse width set at 500 μs and a duty cycle of 0.1%. This setup minimises the generated heat, and therefore self-heating effects are minimised.

Figure 6.2 illustrates that the AlGaN/GaN diodes present current saturation behaviour with the saturation voltage around V_{sat}=6V and $V_{on\text{-}set}$=0.5V (measured at 1mA/mm) at T=25°C for both L_{AC}=5 and 10 μm. The self-heating effects have marginal effects on the V_{sat}. However, a minor increase in I_{sat} is seen in the pulse-mode tests, and therefore, it can be presumed that the minimum differences are caused by the self-heating effects [103]. The generated heat causes the reduction of electron mobility. The same V_{sat} is obtained under the DC- and Pulse-mode tests, indicating that the influence of self-heating effects is minimal in terms of the current saturation behaviour.

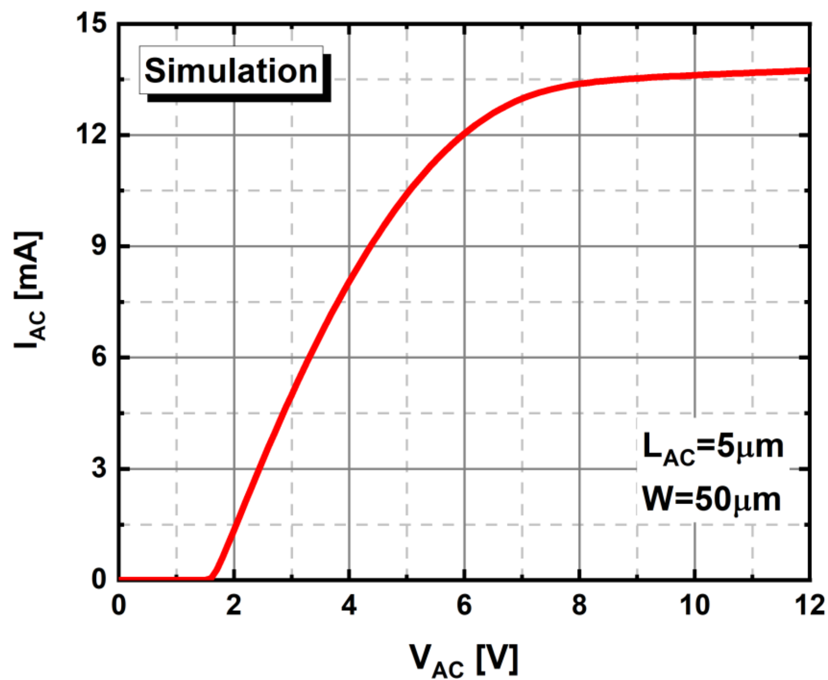
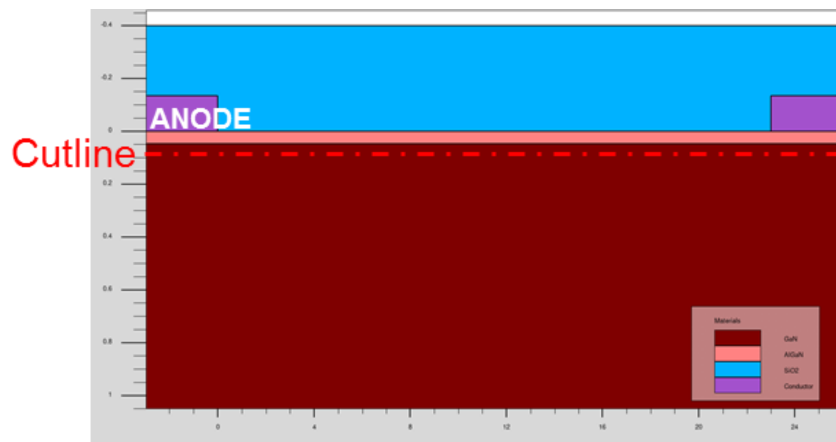


Figure 6.3 The simulated forward I-V characteristics of conventional AlGaN/GaN diode

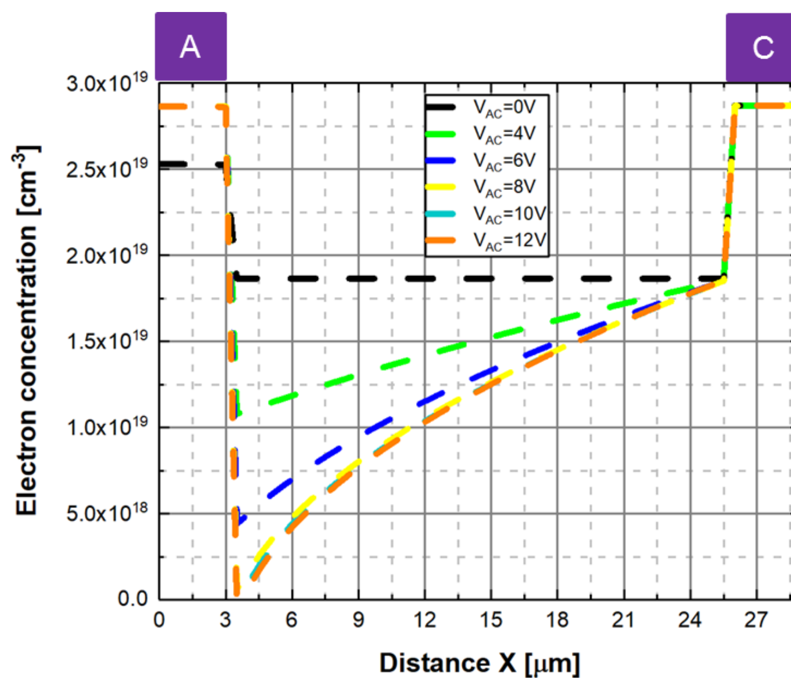
6.1.2. Simulation results and analysis

To understand the physical mechanisms underlying the current saturation behaviour, Silvaco Atlas TCAD is used to create the simulation model for the AlGaN/GaN diode. The physical models in the simulation include POLAR (spontaneous polarisation) and CALC.STRAIN (piezoelectric polarisation), SRH (Shockley-Read-Hall, carrier generation recombination). The defined mobility of 2DEG is 1500cm^2/Vs[35][43].The simulated devices are identical with the measured devices.

The simulated forward I-V curves are displayed in Figure 6.3(L_{AC}=5μm and width is 50μm) which also shows the current saturation behaviour. More specifically, V_{sat} is around 8V, and $V_{on\text{-}set}$ is around 1.6V (obtained at 1mA/mm) at T=25°C.



(a)



(b)

Figure 6.4 (a) the schematic cross-section of conventional AlGaN/GaN diodes with a cutline at the 2DEG channel. (b)the electron concentration distribution along the 2DEG channel.

The electron distribution along the 2DEG channel under increasing bias is shown in Figure 6.4(b). It can be observed that the electron concentration at the edge of the Anode decrease with the rise of the V_{AC} in the linear region (from V_{AC}=2V to 8V). However, it drops dramatically when V_{AC} exceeds 8V (at the saturation region).

Moreover, the electric field distribution along the 2DEG channel under various forward biases is presented in Figure 6.5. When the V_{AC} rises, the electric field peak at the edge of the anode increases substantially.

It can be inferred from the electron concentration and electric field distribution throughout the 2DEG channel that the current saturation behaviour in AlGaN/GaN diodes is caused by the velocity saturation of electrons. The reason for this is as follows: as the bias increases, the electric field near the anode's edge grows significantly due to the potential difference, leading to pinch-off effects in this area. As a result, the AlGaN/GaN diode experiences velocity saturation because the high electric field accelerates the electrons until they reach the saturated velocity.

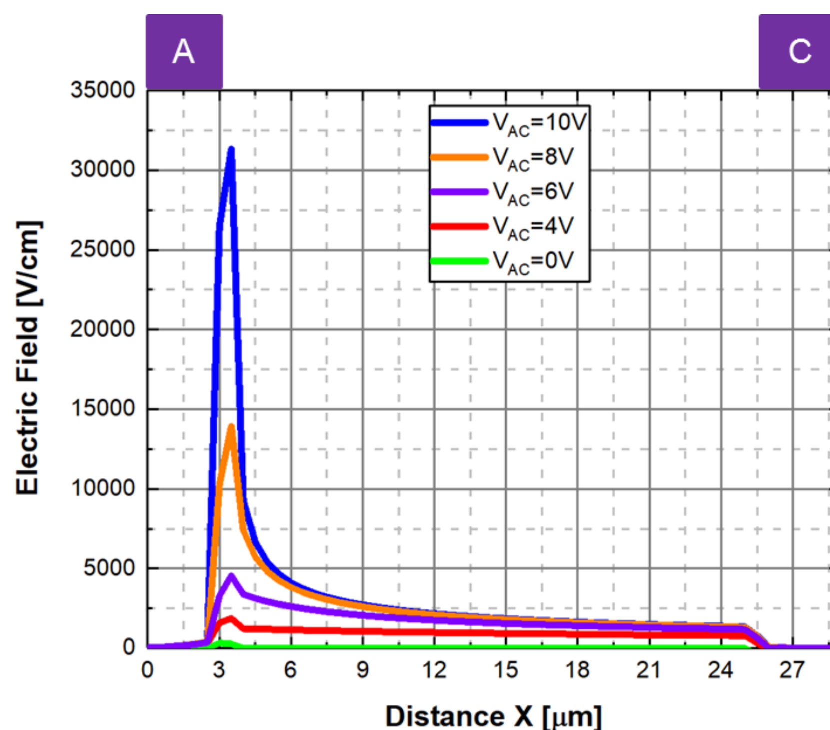


Figure 6.5 The electric field distribution along the 2DEG channel at different V_{AC} (from 0V to 10V).

6.2. PSJ Hybrid diode current saturation behaviour

6.2.1. Introduction

As stated in Chapter 4,PSJ hybrid diode is firstly reported in [71],which has the low on-set voltage(0.4V),low specific $R_{on}A$ (14mΩ·cm^2) and high BV(2.5kV) [71].It has a merged PSJ Schottky diode and PSJ PiN diode. PSJ Schottky diode only has a Schottky contact above the AlGaN layer together with PSJ heterostructures and ohmic Cathode. However, the PSJ PiN diode is composed of the p-type ohmic contact above the P-GaN layer, PSJ PiN heterostructures and ohmic Cathode. The schematic cross-section of the PSJ hybrid is illustrated in Figure 6.6. The anode is composed of the Schottky contact and P-type ohmic contact. The cathode forms an ohmic contact with 2DEG. Therefore, the PSJ Schottky diode and PSJ PiN diode are connected in parallel, and the resistance

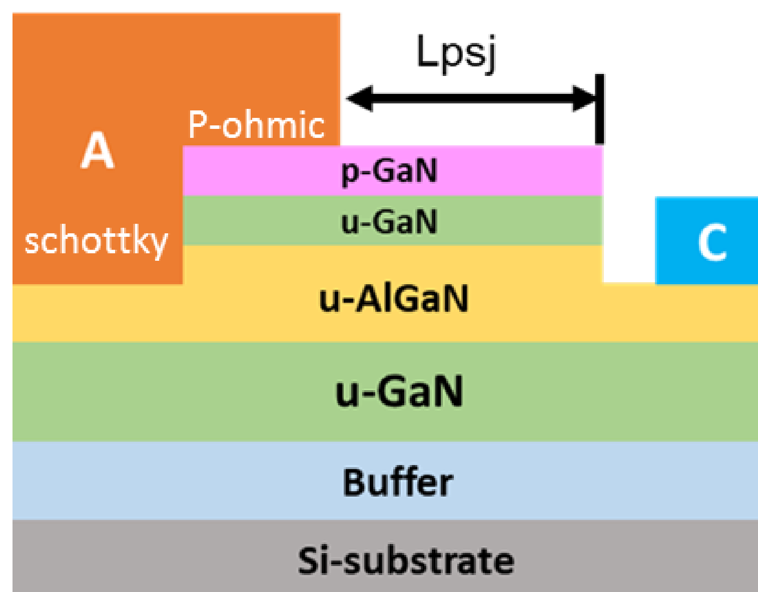


Figure 6.6 The schematic cross-section of PSJ hybrid diode.

of the 2DEG region beneath the 2DHG determines the bipolar on-set voltage of the PiN diode.

6.2.2. Measurement results

PSJ Hybrid diode also shows the current saturation behaviour. The forward I-V curves of three identical large-area 1.2kV and 8A-PSJ hybrid diodes with multi-finger layouts are shown in Figure 6.7. The measurement is processed at room temperature through Curve tracer 371B.

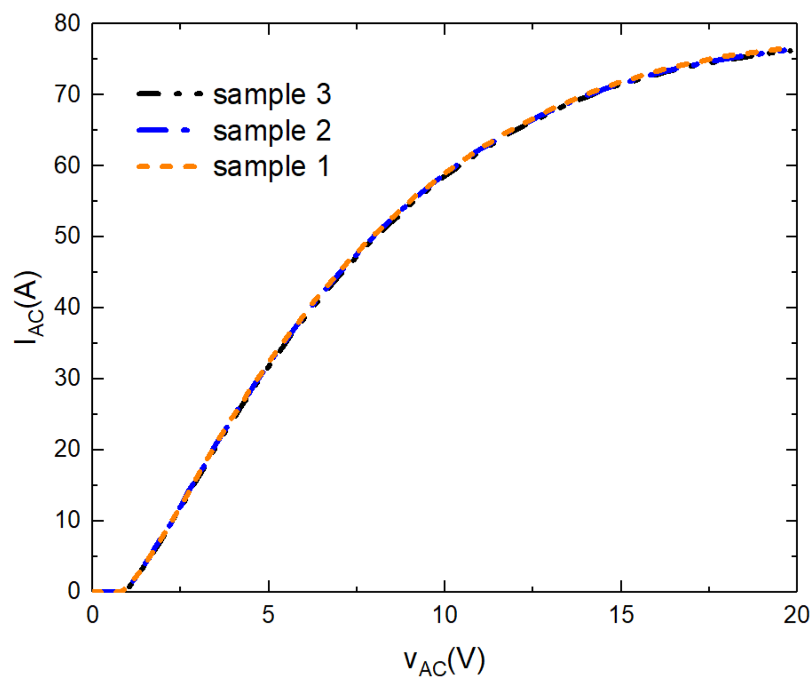
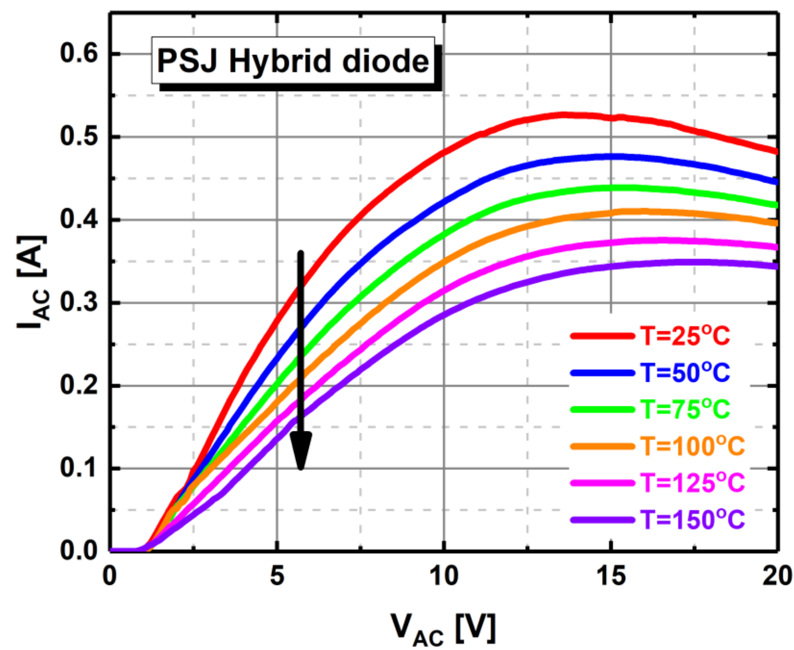


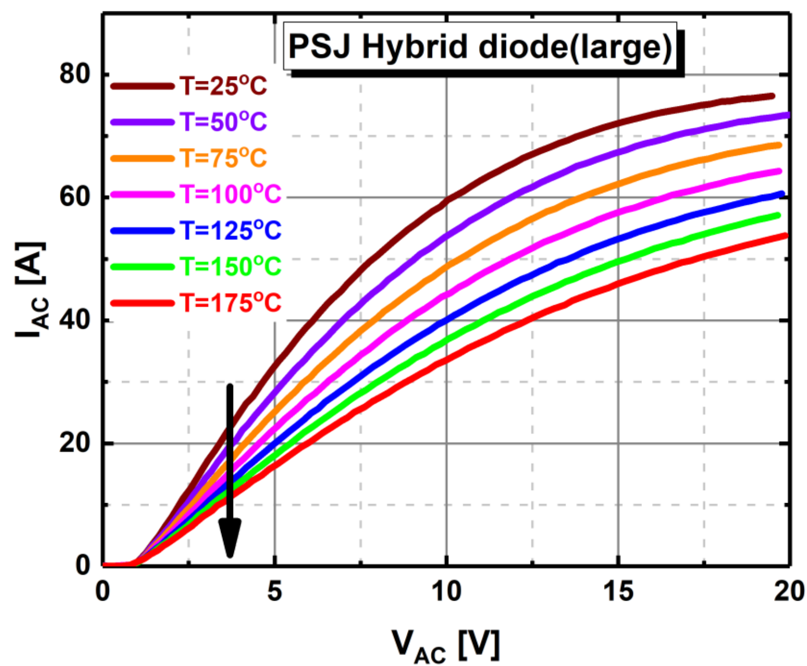
Figure 6.7 The typical forward I-V characteristics of three identical PSJ hybrid diode

It can be observed that all these devices show the current saturation behaviour, and the saturation voltage is around 15V at T=25°C.

Moreover, more PSJ hybrid diodes with shorter gate width (1mm) and simplified test structures, which is defined as the small devices in this chapter, are also measured at the same conditions and observed the same saturation



(a)



(b)

Figure 6.8 The typical forward I-V characteristics of PSJ (a)small (b) large-area hybrid diode as a function of temperature (from 25°C to 175°C).

behaviour. The I-V curves of large and small PSJ hybrid diodes at different temperatures are also presented in Figure 6.8, respectively. Similarly, the measured curves by using the pulse-mode and DC-mode are not identical with

each other and the pulse-mode curves are flatter in the saturation region, which is due to the self-heating effects. However, it does not influence the saturation behaviour significantly. Therefore, it can conclude that both large and small PSJ hybrid diodes exhibit the same trend with an increase in temperature. And even when the temperature increases, the saturation voltage almost remains constant in the pulse-mode tests and slightly dropped because of the self-heating effects.

6.2.3. Simulation results and analysis

Following a similar analytical method through the simulation, the forward I-V characteristics of the PSJ hybrid diode are simulated in SILVACO TCAD. The simulation models are identical to the previous section.

First, it is essential to figure out whether the PSJ hybrid diode is a bipolar device or not. Structurally, the PSJ hybrid diode merges a Schottky barrier diode and a PSJ PiN diode. As Figure 6.6 illustrates, 2DHG, AlGaN layer and 2DEG form

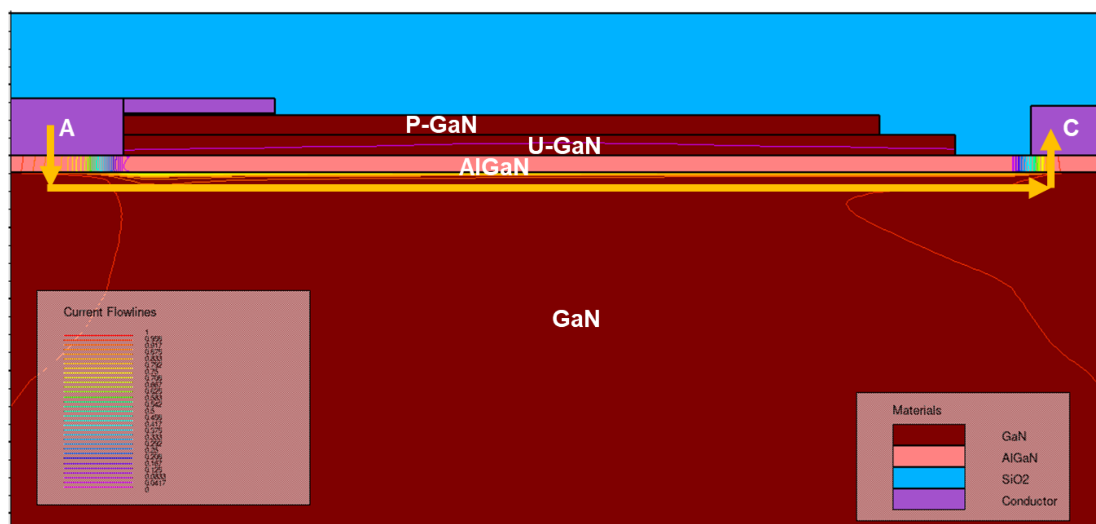


Figure 6.9 The simulated current flow-lines distribution at V_{AC}=10V in PSJ hybrid diode.

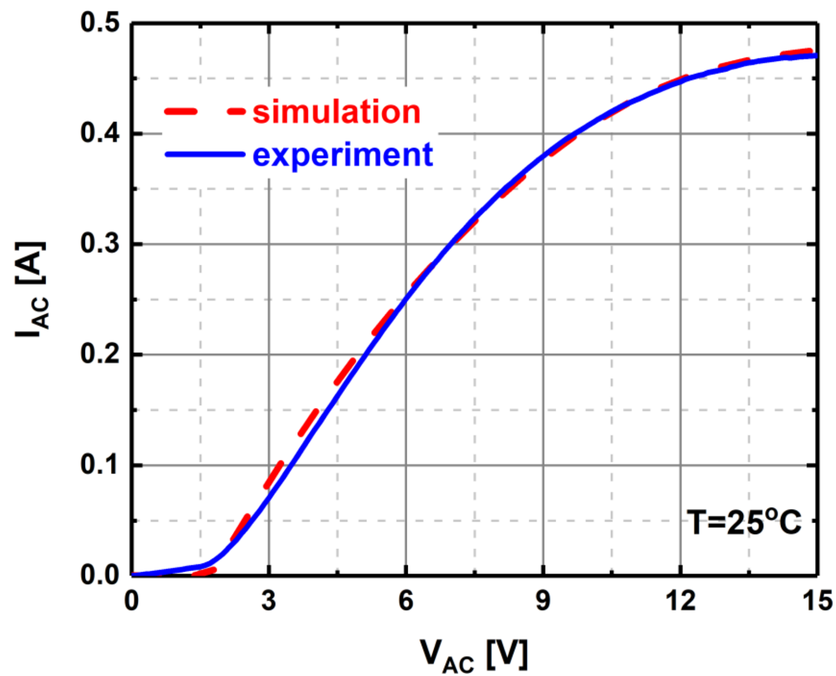
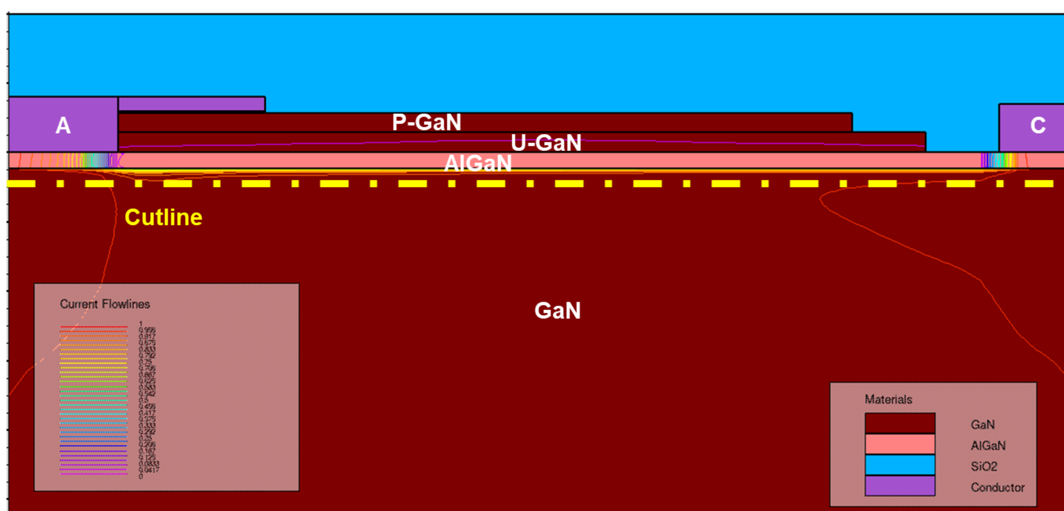


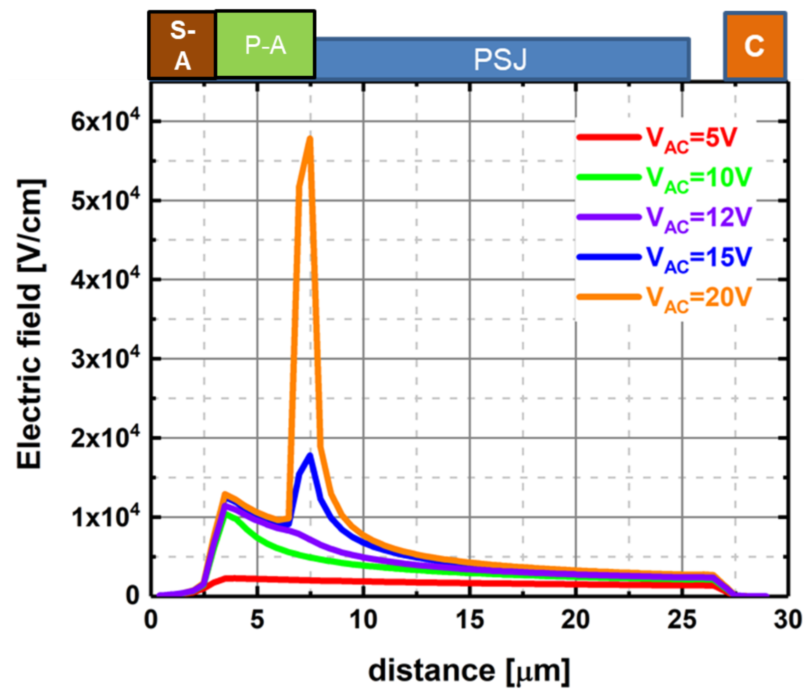
Figure 6.10 The typical I-V characteristics of the PSJ hybrid diode obtained from the simulation and experiment.

a PiN junction. The on-set voltage of the PiN junction is approximately 3.4V, which will be presented in the following sections. However, the on-set voltage for the Schottky diode ranges from 0.4V to 1V, indicating that when the voltage rises, the Schottky diode conducts first. Moreover, the turn-on mechanism of the PiN junction is resistive, which means the voltage drop across the 2DEG region beneath the PN region must be large enough to cause a resistive voltage drop of 3.4V. With the high concentration of 2DEG, this does not happen;

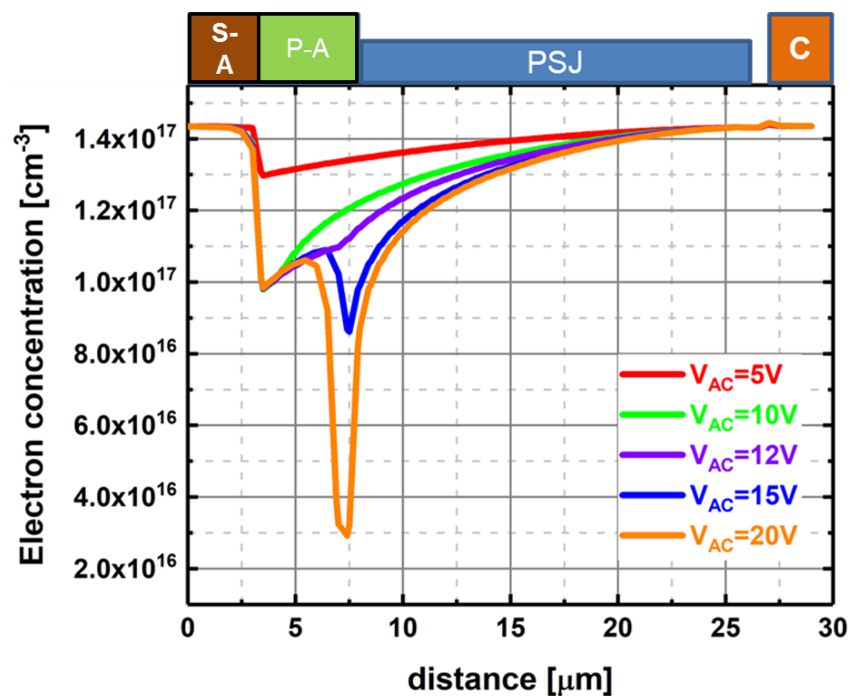
therefore, the PN junction does not turn on. Thus, the PSJ hybrid diode operates as a unipolar power diode.



(a)



(b)



(c)

Figure 6.11(a) the cutline is located along the 2DEG channel, (b)the electric field distribution, and (C) the electron distribution with the rise of the V_{AC}(from 5V to 20V).

The Simulated current flow lines of the PSJ hybrid diode at V_{AC}=10V are also shown in Figure 6.9. It also proves that the PiN diode barely contributes to the

forward current, with most of the current flowing from the Schottky barrier diode to the cathode.

Therefore, the PSJ hybrid diode are built in the simulation for analysing the saturation behaviour. It has the same dimensions with the measured small diodes with L_{psj}=15um and W=1mm. The simulated results of the PSJ hybrid diode are displayed in Figure 6.10, and it is well fitted with the experiment results. The saturation voltage is around 15Vat T=25°C. With a rise in forwarding bias, the electric field and electron concentration distribution along the 2DEG channel are displayed in Figure 6.11(a). As Figure 6.11 illustrates, the mechanisms of the current saturation behaviour of the PSJ hybrid diode are like the AlGaN/GaN diode. Due to the absence of the minority carrier injection, the electrons are the only carriers. They are accelerated by the high electric field peak at the edge of the anode as a result of the potential difference between the anode and the 2DEG channel as the bias increases, resulting in velocity saturation behaviour at the pinch-off area. Therefore, it can be concluded that the velocity saturation of electrons and minimal conductivity modulation induced by the minority carrier in the drift region result in the observed current saturation behaviour of the PSJ hybrid diodes.

6.3. Current saturation behaviour in PSJ PiN diode

The Bipolar GaN PSJ PiN diode is composed of the 2DHG, AlGaN intrinsic layer and 2DEG and has different mechanisms governing its current saturation behaviour.

6.3.1. Introduction

Figure 6.12 depicts the on-state characteristics of the Si PiN rectifier. When it conducts under forwarding bias but at relatively lower current levels, the low-level injection current is generated. And the current flow density is proportional to (qV_{on}/kT). When the injected carriers further increase and achieve the high-level injection conditions (the injected carrier concentration is higher than the majority concentration in the drift region), the conductivity

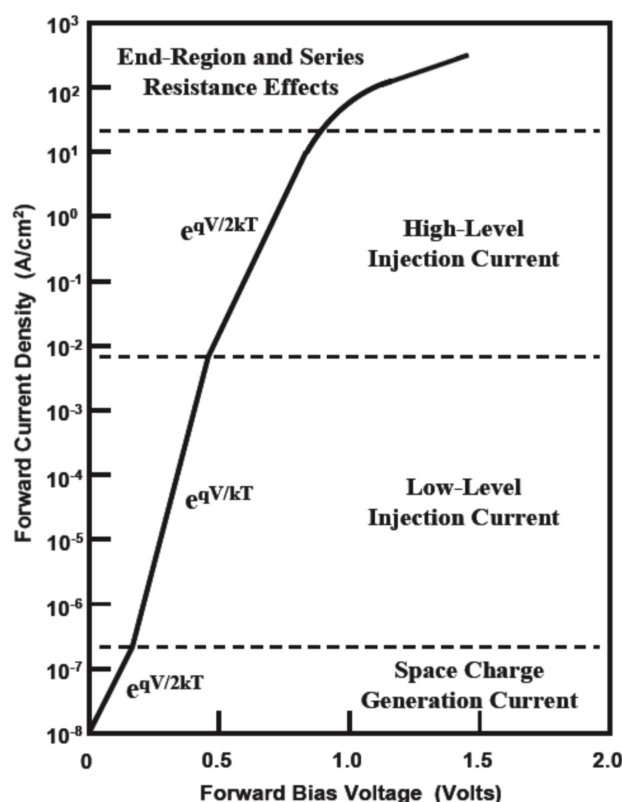


Figure 6.12 The on-state characteristics of Si PiN rectifier[104].

modulation occurs, thus causing the slope to become exponential [exp($qV_{on}/2kT$)]. That is because, under high-level injection, the injected hole concentration in the drift region is higher than the N-doping concentration when the high-level injection occurs in the P+/N-/N+ junction. To maintain charge neutrality in the drift region, an equal number of free electrons is also injected into the drift region. As a result, the drift region has a high concentration of free carriers, which exceeds its background doping concentration and lowers the on-state resistance. This phenomenon is named conductivity modulation [101]. Due to the conductivity modulation, the current density increases dramatically with the rising bias, and no current saturation behaviour can be observed in the Si PiN diode shown in Figure 6.12 [104].

6.3.2. Device structures and measurement results

PSJ heterostructures (u-GaN/AlGaN/u-GaN) are capped with the Mg-doped P-GaN and P++GaN layer, and their thickness is 43nm and 30nm, respectively. And the doping density of Magnesium (Mg) is 1e19 cm^{-3} and 1e20 cm^{-3}, respectively. 2DEG and 2DHG coexist spontaneously at the interface of the AlGaN (000$\bar{1}$)/GaN (0001) and GaN (000$\bar{1}$)/AlGaN (0001), respectively. The thickness of the top and bottom u-GaN layers is 20nm and 800nm, respectively. AlGaN layer thickness is 25nm, and the Al content is 0.3. Therefore, the high

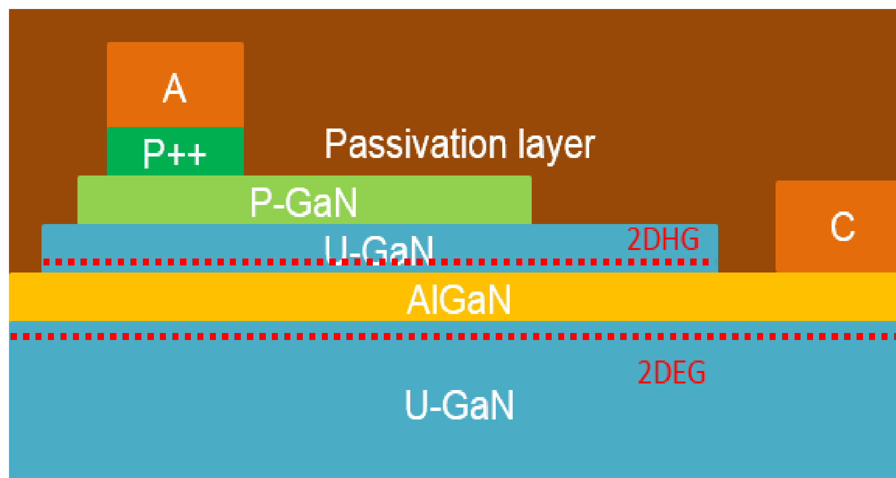


Figure 6.13 The schematic cross-section of PSJ PiN diode. The AlGaN thickness is 25nm, and the Al mole fraction is 0.3. A and C represented Anode and Cathode.

density of 2DHG and 2DEG, and the intrinsic area is the AlGaN layer will form the PiN junction. Moreover, the width of the device is 1mm.

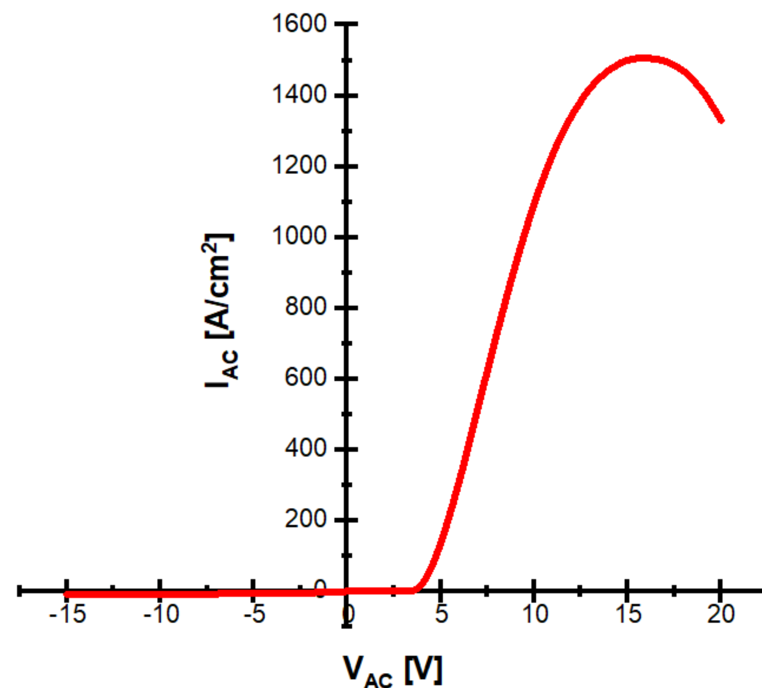


Figure 6.14 Typical DC-mode I-V characteristics of the GaN PSJ PiN diode.

Figure 6.14 shows the typical I-V characteristics of the GaN PSJ PiN diode. The bipolar turn-on voltage is measured to be 3.4V (@1mA/mm) at T=25°C.

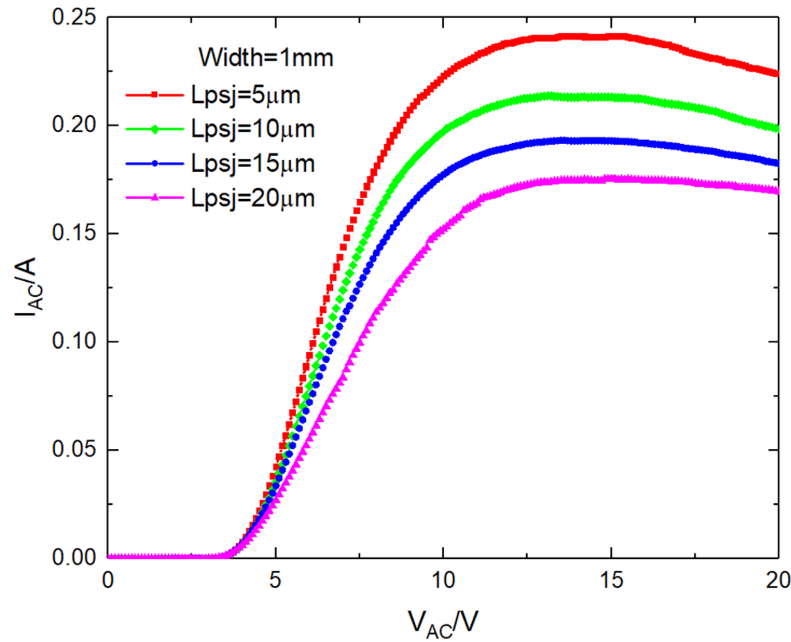
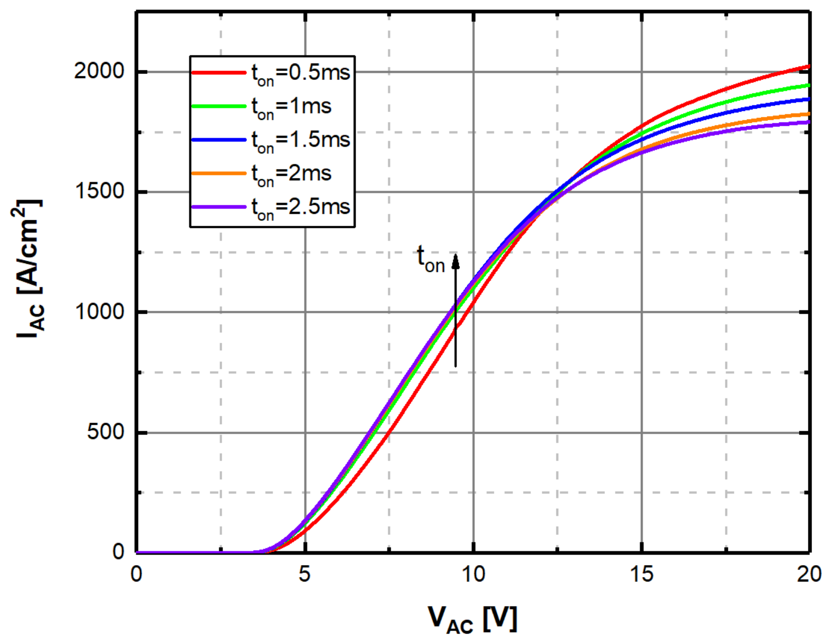


Figure 6.15 Typical DC-mode I-V characteristics of the GaN PSJ PiN diode with L_{PSJ}=5,10,15, and 20 μm.

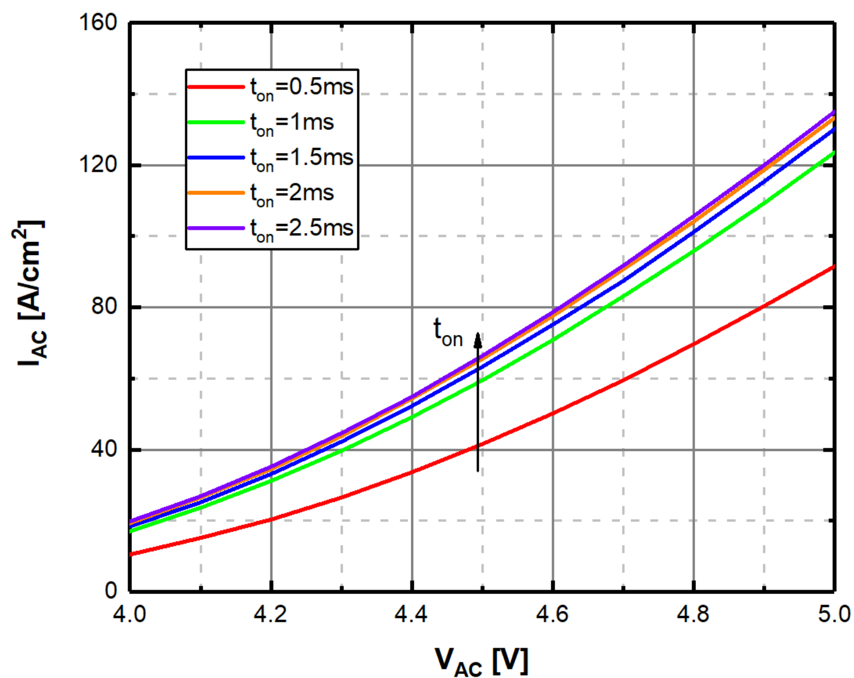
However, the forward conductive characteristics have a unique current saturation behaviour. PSJ PiN diodes with different L_{PSJ} are also measured, and their I-V characteristics are plotted in Figure 6.15. They all exhibit the current saturation behaviour, and the saturation voltage is unaffected by the PSJ length. All these results show identical current saturation behaviour with a similar saturation voltage independent of the length of PSJ.

6.3.3. Conductivity modulation evaluation in PSJ PiN diode

In this work, following the previous introductions, conductivity modulation in the PSJ PiN diodes is initially evaluated through the Pulse-mode forward I-V characteristics with different pulse widths[74]. With the increase of the pulse width, more holes are injected in the AlGaN layer, inducing more significant conductivity modulation. These tests are carried out using the Keysight B1500A



(a)



(b)

Figure 6.16 Forward pulsed I-V characteristics under different on-state periods varying from 0.5ms to 2ms with the step of 0.5ms, and the pulse period is fixed at 500ms.(a)V_{AC} from 0v to 20V (b) V_{AC} from 4V to 5V.

device curve tracer. The measurement conditions are similar to those for the vertical GaN PiN diode[74]. The pulse off-time is increased to 500ms to

eliminate the possible self-heating effects, and the pulse width (t_{on}) varies from 0.5ms to 2.5ms in steps of 0.5ms.

Figure 6.16(b) shows that the current density for t_{on}=0.5ms and 1.0ms is slightly lower than that for t_{on}=1.5ms and 2.0ms under the relatively low bias (4V to 5V) at T=25°C. However, it doesn't present a clear downward trend between R_{on} and the t_{on}, indicating that R_{on} has almost no variation with the t_{on}. Therefore, conductivity modulation can be argued to be negligible in the PSJ PiN diode. This is highly likely due to the very short carrier lifetime of the injected holes in GaN(around 1ns to 10ns)as well as low mobility of (less than 16 cm^2/V-sec) [85] [105]. This behaviour is comparable to the results found in the vertical GaN PiN diodes [74][105]. Furthermore, the conductivity modulation is localised and mainly happens only at the AlGaN layer under the Anode region.

Therefore, the insignificant and localised conductivity modulation in the PSJ PiN diode is one of the possible causes of the current saturation behaviour.

6.3.4. Trap effects on the current saturation

As reported in chapter 5, the marginal and localised conductivity modulation is also thought to be one of the causes of the current saturation behaviour in the PSJ PiN diode.

Various works of literature report the existence of electron and hole traps in the AlGaN layer, which is presented in chapter 5. In exploring the V_{th} shift in PSJ HFETs, it has been proved that both the electron and hole trap states existed in the AlGaN layer. Therefore, trap states are also introduced in the AlGaN layer to investigate the current saturation behaviour.

The physical models include POLAR (spontaneous polarisation) and CALC.STRAIN (piezoelectric polarisation), SRH (Shockley-Read-Hall, carrier generation recombination). The defined mobility of 2DEG and 2DHG 1500cm^2/Vs and 16cm^2/Vs [68], [85], respectively used in the simulation. The hole carrier lifetime is defined as 1ns [105]. The dimensions of the simulated structures and the relevant parameters are consistent with the actual devices. Moreover, the equal electron and hole trap density is defined in the AlGaN layer, and their carrier capture cross-section is 1e-15 cm^2[97].The simulated forward I-V characteristics with different trap concentration (6e18cm^{-3}, 6.5e18cm^{-3} and 6.7e18 cm^{-3}) shown in Figure 6.17. There is no saturation behaviour when no trap is defined in the AlGaN layer below V_{AC}=50V. However, the saturation voltage and current show a downward trend as the

trap density rises. The saturation current drops from around 1.5A for 6e18 cm^{-3} to 0.6A for 6.7e18 cm^{-3}, and the saturation voltage decreases from around 27V for 6e18cm^{-3} to 15V for 6.7e18cm^{-3} at T=25°C, demonstrating that the trap densities are a relevant cause for the current saturation behaviour in the PSJ PiN diode.

It is known that the diffusion current dominates the forward current of the PiN diode[104]. Thus the diffusion current density ($J_{diffusion}$) distribution of the PSJ PiN diode under various biases is presented in Figure 6.18. It rises initially with the increase of the bias(from 5V to 15V). However, it gradually saturates when the bias further increases from 15V to 25V in the AlGaN layer.

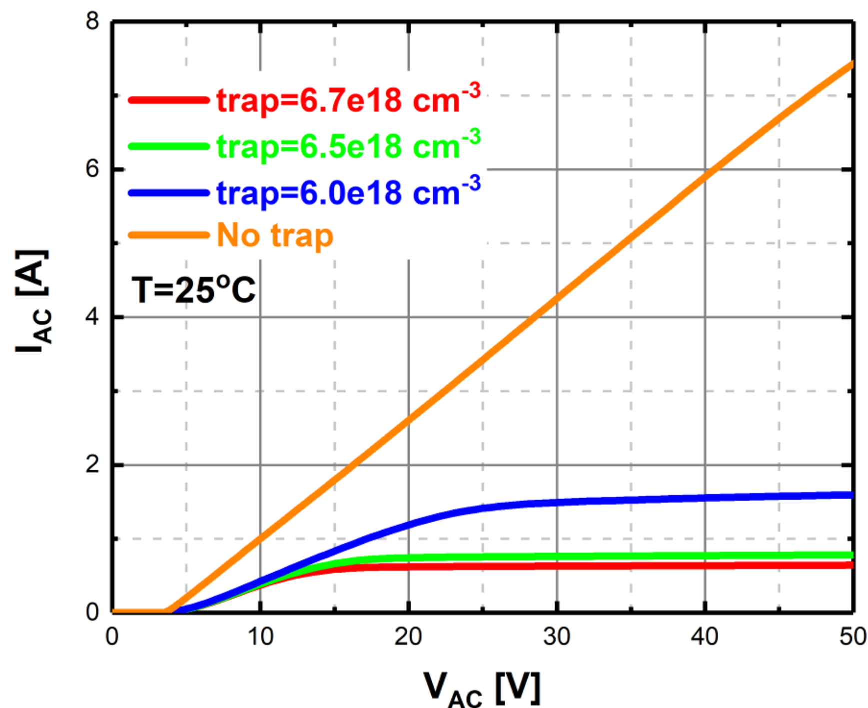
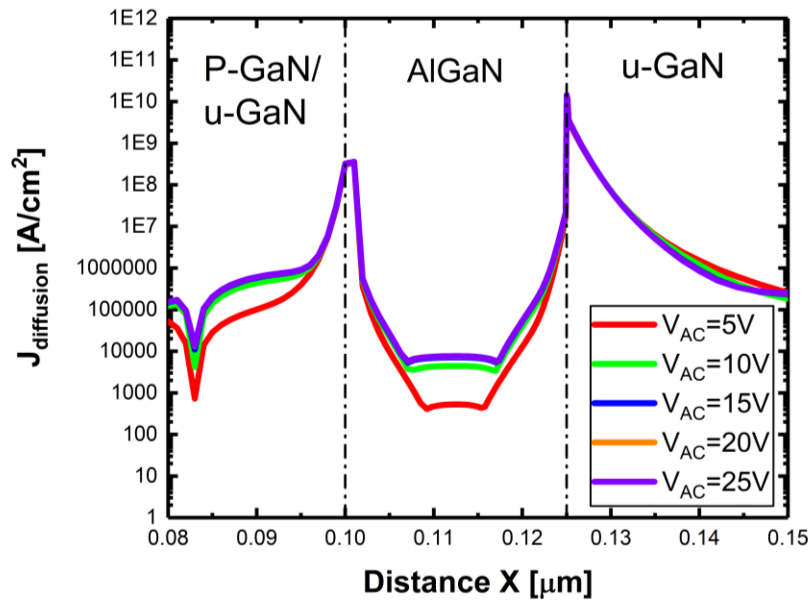
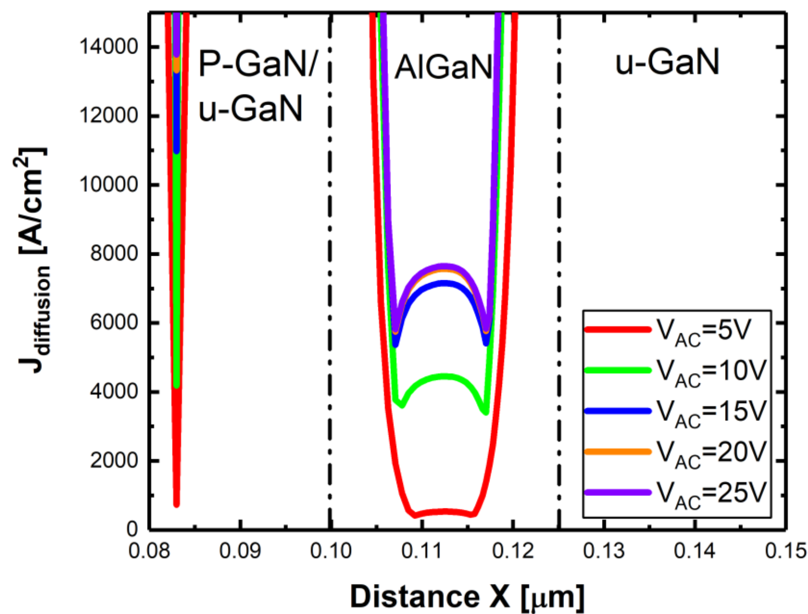


Figure 6.17 Simulation: forward I-V characteristics with different trap concentration

The electron and hole velocity distribution of the PiN junction in the PSJ PiN diode with Electron and hole trap densities equal to 6.7e18 cm^{-3} are also shown

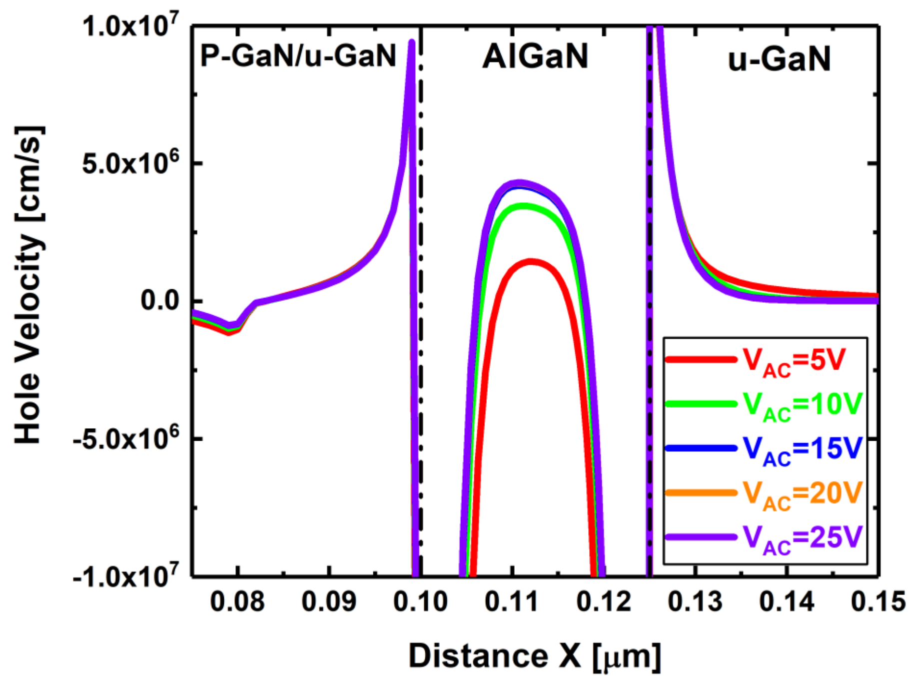


(a)

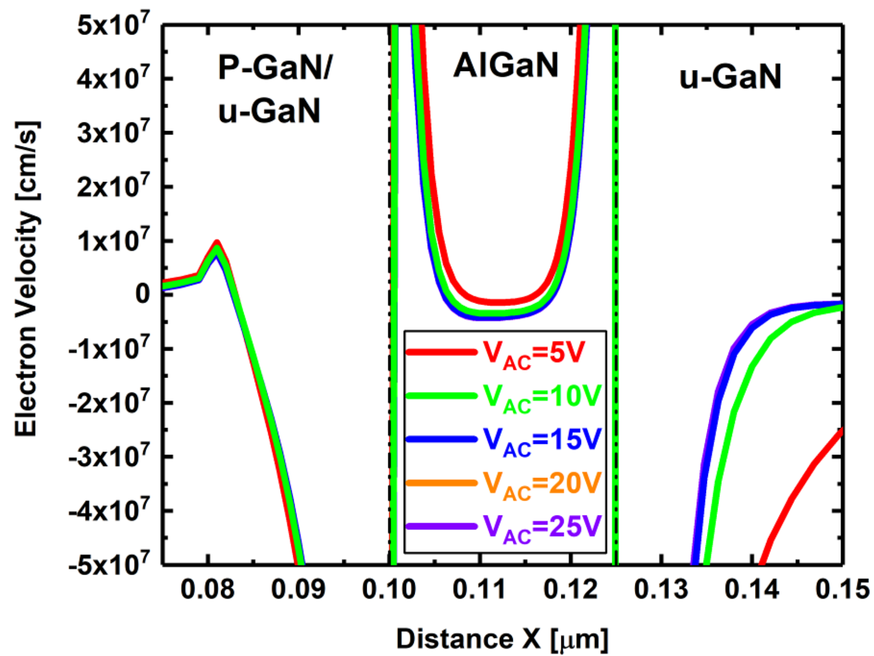


(b)

Figure 6.18 (a) The distribution of the diffusion current density of the PiN junction and (b) Zoom-in the AlGaN layer under different biases (from 5V to 25V, the step is 5V) at the trap states concentration equal to 6.7e18.



(a)



(b)

Figure 6.19 (a)The hole and (b) electron velocity distribution in the PiN junction under different biases (from 5V to 25V, the step is 5V) at the trap states concentration equal to 6.7e18 cm^{-3}.

in Figure 6.19(a) (b). Both initially increase with the bias (from 5V to 15V) and gradually saturate with the further increase of the voltages (from 15V to 25V)

in the intrinsic region (AlGaN layer). The trend is consistent with the distribution of the diffusion current in the PiN junction, indicating that the current saturation behaviour is related to the saturation velocity of carriers in the AlGaN layer.

Based on simulated results, the operation principles of the PSJ PiN diode are discussed. When a positive bias is provided to the anode less than the turn-on voltage (~3.4V), electrons and holes cannot pass through the GaN/AlGaN/GaN heterostructures.

However, when the V_{AC} exceeds the knee voltage, the electrons and holes can pass through the AlGaN layer. Trap-assisted transportation mechanisms refer to the tendency of the carriers to move via the trap energy levels because of the

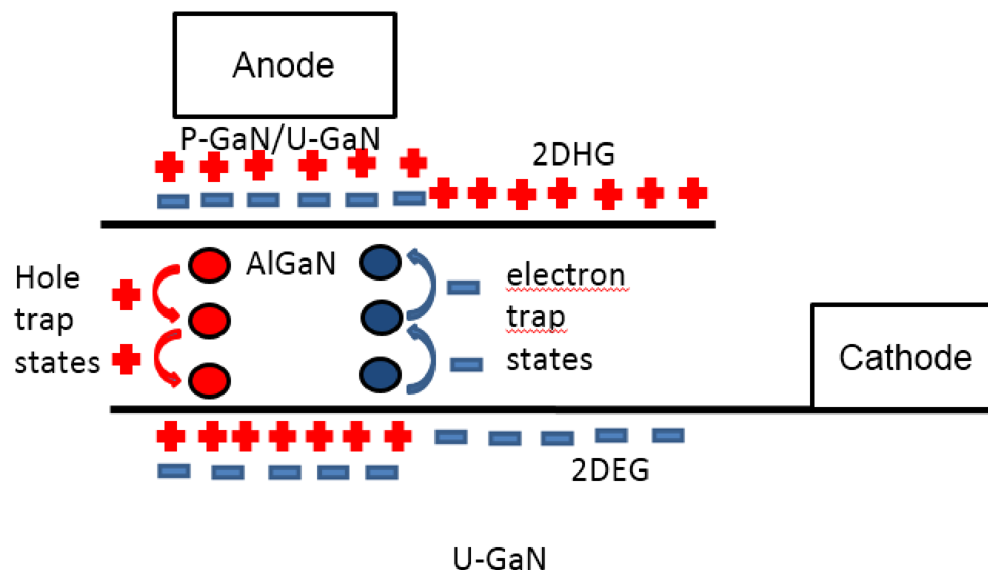
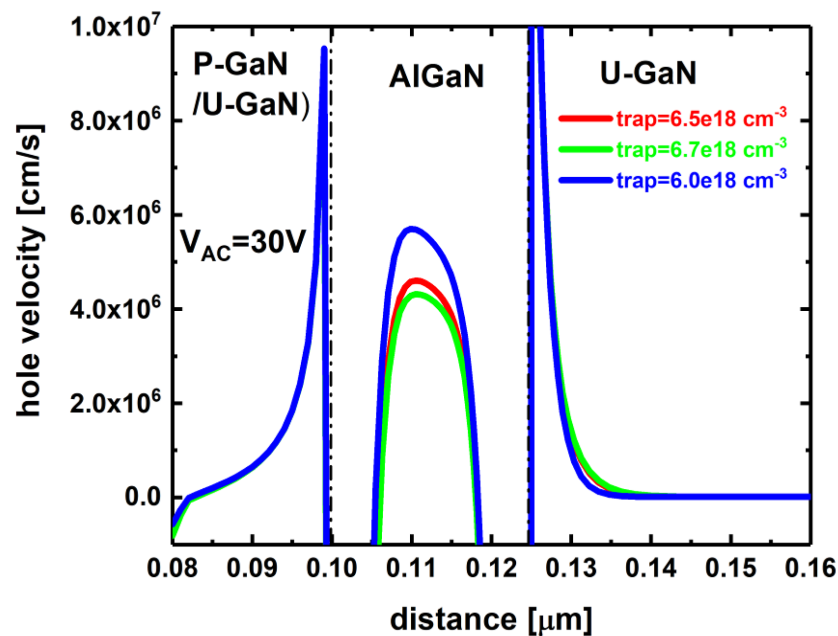
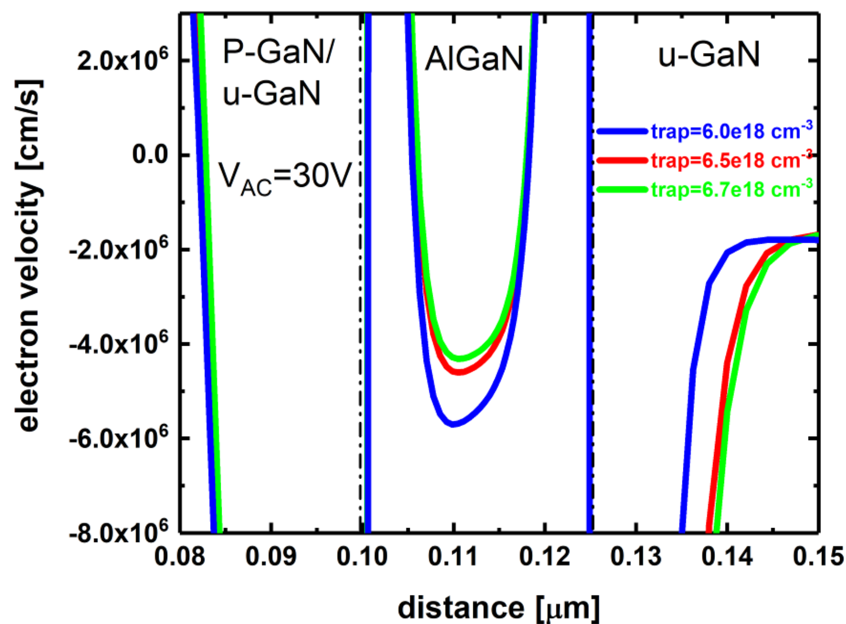


Figure 6.20 The operation principles of the trap-assisted mechanism for the PSJ PiN diode current saturation behaviour under the forward bias.



(a)



(b)

Figure 6.21 The distribution of the (a) hole saturation velocity of the PiN junction and (b) electron saturation velocity with different trap concentrations.

high bandgap of the AlGaN layer [106]. Furthermore, the mobility and recombination rate of electrons/holes are decreased because of the high density of electron/hole trap states [107], [108]. Therefore, according to the simulation

results, it was found that the high density of traps limits the velocity of the electrons/holes in the AlGaN layer at the saturation region. Unlike the velocity saturation mechanisms in the conventional AlGaN/GaN diode and PSJ hybrid diode, the carrier velocity saturation is caused by the high density of traps in the AlGaN layer instead of the high electric field. Therefore, the carrier concentration at either side of the PiN junction gradually saturates, causing the saturation of the diffusion current.

From Figure 6.21, in the saturation region (at V_{AC}=30V), the electron and hole saturation velocity drop when the trap density increases from 6e18 cm^{-3} to 6.7e18 cm^{-3}. These findings also explain the declining tendency of saturation voltage and current as a function of trap density in the AlGaN layer, shown in Figure 6.17. Therefore, the simulation results indicate that trap-induced velocity saturation could be a possible mechanism for the saturation behaviour. Combined with the negligible and localised conductivity modulation discussed in the last section, they can comprehensively explain the saturation behaviour in the PSJ PiN diode.

6.4. Summary

The current saturation behaviour and the saturation mechanisms of the unipolar power GaN diodes: AlGaN/GaN diode and PSJ hybrid diode are firstly reported and discussed. It is found that velocity saturation, together with the minimal conductivity modulation induced by the minority carrier in the drift region resulting in the current saturation behaviour, is the main reason for the saturation behaviour in these two diodes. The simulation results present the high electric field region caused by the potential difference between the Anode and 2DEG channel, also referred to as the pinch-off region. Therefore, the electrons are speeded up at this region until the electron velocity is saturated when the bias increases. In conclusion, the velocity saturation induced by the high electric field peak is responsible for the current saturation behaviour in the conventional AlGaN/GaN diode and PSJ hybrid diode.

Moreover, a unique current saturation behaviour of the forward I-V characteristics of the bipolar PSJ PiN diode is also discussed. Firstly, due to the low carrier lifetime and hole mobility, the conductivity modulation is negligible and localised in the PSJ PiN diode, indicating that it is one of the critical causes of this phenomenon. Moreover, trap effects are also discussed according to the simulation results. It is discovered that as the trap density in the AlGaN layer increases, the saturation voltage and current drop. Therefore, the saturation velocity in the AlGaN layer is thought to be constrained by the

high density of traps. In conclusion, trap-induced velocity saturation is also responsible for the current saturation behaviour in the PSJ PiN diode.

Chapter 7. Gate leakage current mechanisms of PSJ HFETs

This chapter discusses gate leakage current mechanisms in the P-GaN gate PSJ HFET. Measured I_g-V_g characteristics show unique saturation behaviour when gate voltage (V_g) is below the threshold voltage (V_{th}). Moreover, the gate leakage current mechanisms under reverse bias at the saturation and non-saturation regions are discussed. These are composed of the vertical PiN junction reverse currents (I_{gV}) and the lateral surface leakage currents (I_{gL}). The temperature-dependent I_g-V_g characteristics are also measured from 25°C to 150°C in steps of 25°C. The vertical PiN junction current becomes the primary current at the saturation region. In the non-saturation region, it was found that the surface leakage current is dominant, and the possible mechanism for the surface leakage current is the two-dimensional variable range hopping (2D-VRH).

7.1. Introduction

GaN HEMT performance and reliability at high voltages are critically dependent on gate leakage current. The reverse gate leakage currents affect the power losses and gate breakdown voltages in the off-state. Moreover, the relationship between the p-GaN gate leakage current and the avalanche capability of P-GaN gate HEMTs is also reported [109].

The temperature-dependent gate current and voltage (I_g-V_g) measurements are used to assess the mechanisms governing gate leakage current in normally-off

P-GaN gate AlGaN/GaN HEMTs [110]. It was discovered that the vertical leakage current at the intersection of the PiN junction current and the P-type Schottky junction might be separated from the gate leakage current. The two-dimensional variable range hopping (2D-VRH) mechanism causes gate surface leakage current under the comparatively low positive gate bias and reverse bias [110].2D-VRH is a carrier transportation mechanism along with the surface electronic states [110]. Under the positive gate bias, thermionic field emission (TFE) is the dominant mechanism of gate current transport. The Poole-Frenkel emission (PFE) [111]and Trap-assisted tunnelling (TAT) [111]–[113]are widely thought to be the dominant leakage mechanisms for vertical gate leakage current in P-GaN Schottky gate/Schottky gate GaN HEMTs under negative gate biases.

The PSJ HFETs considered herein are normally-on devices. Therefore, to turn these off, negative gate biases are required. Furthermore, it is crucial to investigate the gate leakage current mechanisms in such devices. Considering that the p-type ohmic gate contact is used in PSJ HFETs, the Poole-Frenkel emission (PFE) [111] and Trap-assisted tunnelling (TAT) [111]–[113] are considered to be not applicable. Therefore, this work addresses the gate leakage current mechanisms of the p-GaN ohmic gate PSJ HFETs through gate leakage current-voltage (I_g-V_g) measurements and simulation.

7.2. Device structures and parameters

The device structure and dimensions are shown in Figure 7.1.

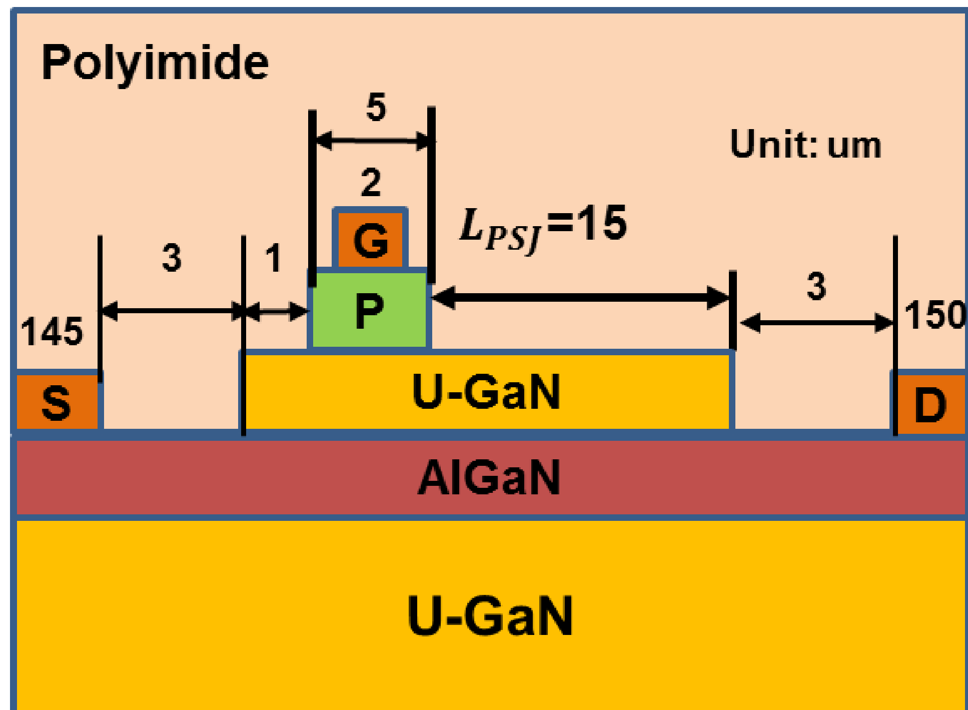


Figure 7.1 The schematic cross-section of the PSJ P-GaN ohmic gate HFETs.

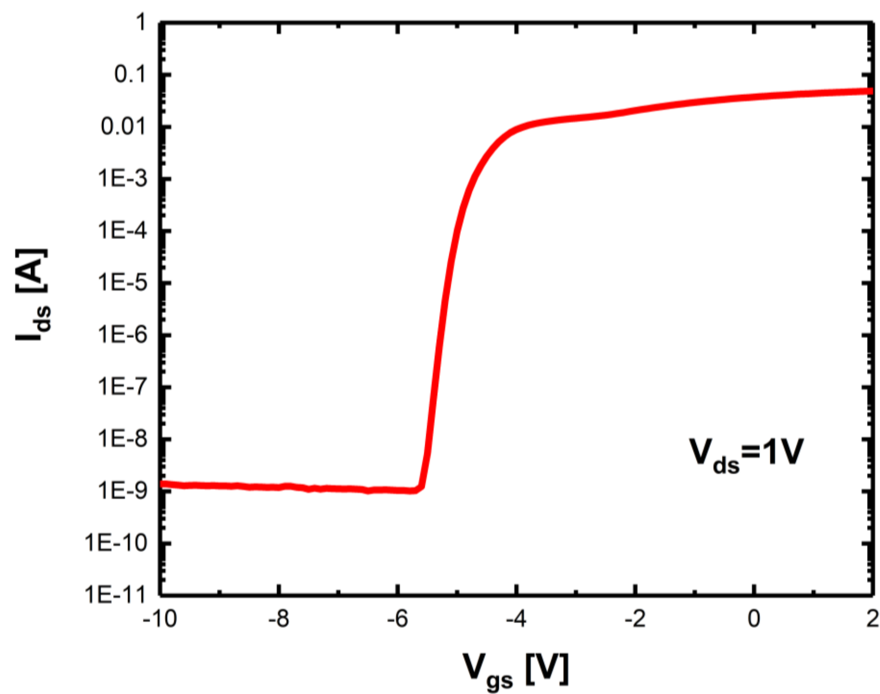


Figure 7.2 Typical transfer characteristics (Ids-Vgs) of the PSJ HFETs were measured at Vds=1V.

7.3. Electric static characteristics of devices

Typical transfer characteristics are measured at V_{ds}=1V, and V_{th} is -5Vshown in Figure 7.2. Furthermore, typical pulsed I_d-V_d characteristics are measured at V_{gs}=-5V to 2V with the step of 1V and presented in Figure 7.3. The pulse width is 1ms, and the duty cycle is 1%.

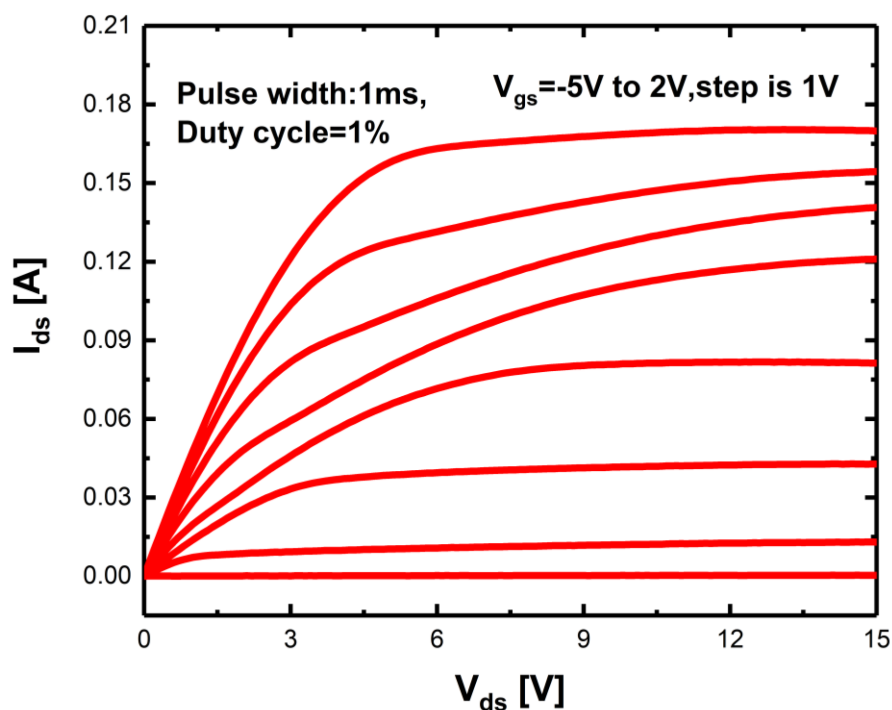
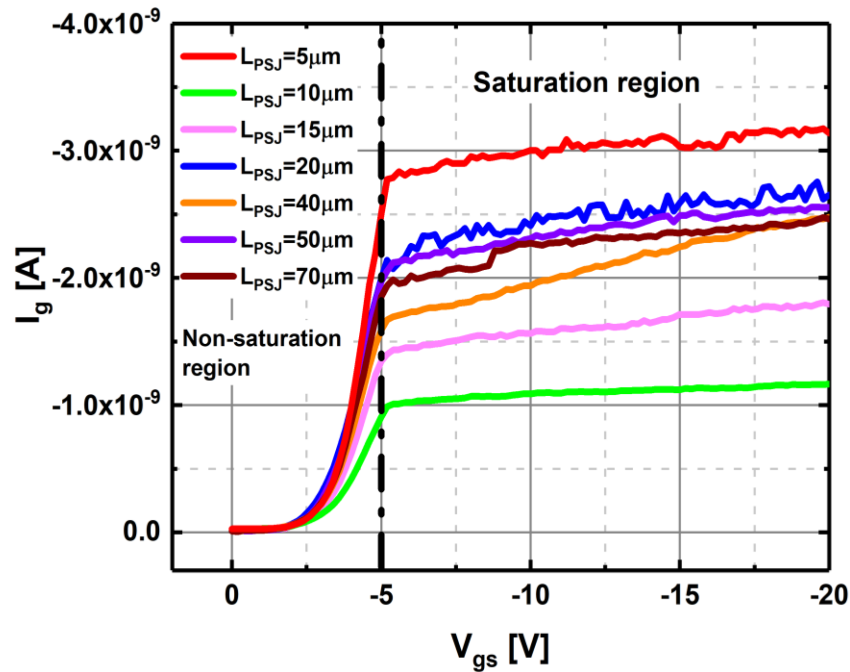


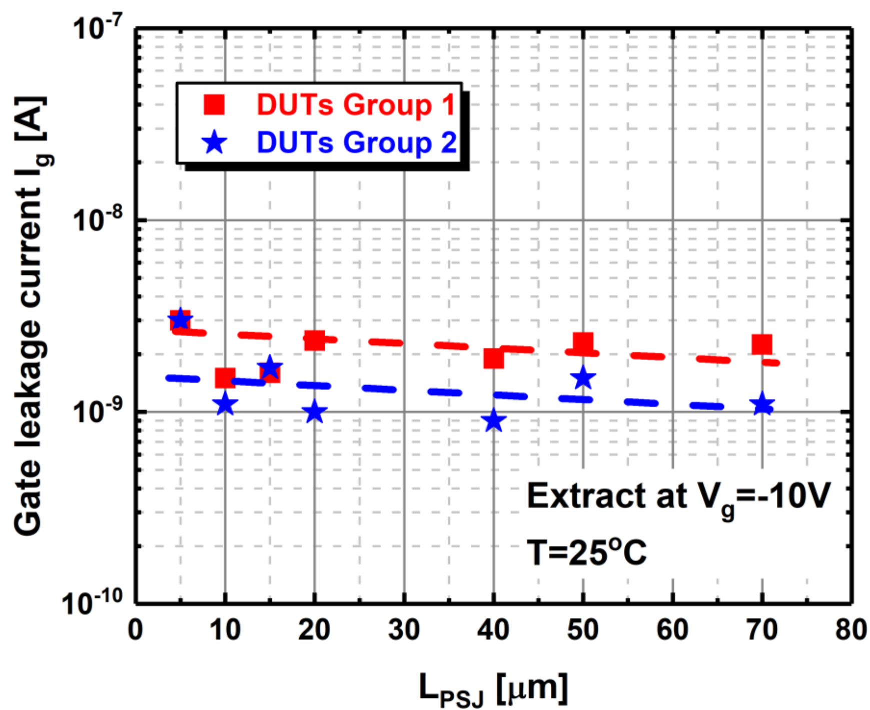
Figure 7.3 Typical pulsed Id-Vd characteristics of the PSJ HFETs were measured at V_{gs}=-5V to 2V with the step of 1V. The pulse width is 1ms, and the duty cycle is 1% at room temperature.

7.4. Gate leakage current measurement results

The I_g-V_g measurement is carried through the 4200A-SCS Semiconductor Devices Parameter Analyzer under dark conditions and at room temperature. Generally, the gate leakage current of AlGaN/GaN HEMTs is composed of two components: a vertical component that travels through the Schottky gate



(a)



(b)

Figure 7.4 (a)Typical gate leakage characteristics (Ig-Vg) of the PSJ HFETs with different lengths of PSJ(LPSJ):5,10,15,20,40,50,70 um at room temperature under dark conditions. (b) gate leakage current of PSJ HFETs with different LPSJ is extracted at Vg=-10V.

contact and a lateral component that travels through two-dimensional variable

range hopping (2D-VRH) mechanisms [110], [114]. Similarly, the gate leakage current in PSJ HFETs can be split into the lateral surface leakage current (I_{gL}) and the vertical reverse PiN junction current (I_{gV}), as shown in Figure 7.1.

The threshold voltage (V_{th}) is -5V (measured at 1mA/mm). Gate leakage current characteristics (I_g-V_g) of the DUTs with different L_{PSJ} are shown in Figure 7.4 (a). It can be observed that gate leakage currents initially increase with the rise in the negative gate voltages. However, the leakage currents gradually saturate when the gate voltages are below -5V. Thus, the saturation voltage is -5V, which is identical to V_{th} (measured at 1mA/mm). Based on this saturation behaviour, the non-saturation region for gate voltages is defined as voltages above -5V. The saturation region is defined as values below -5V, as presented in Figure 7.4(a).

The gate leakage current tests are carried out on more devices, and the values extracted from I_g-V_g characteristics are depicted in Figure 7.4(b). It can be observed that the measured gate leakage current is mainly between 1nA to 3nA, with no clear trend associated with L_{PSJ}, indicating that it is independent of L_{PSJ}.

7.5. Mechanisms of gate leakage Current at the saturation region ($V_g \leqslant V_{th}$=-5V)

A theoretical analysis of the PiN junction current is discussed further to investigate the gate leakage current at the saturation region. It is widely known

that the PiN junction reversed leakage current consists of diffusion current (J_{diff}) and space-charge generation current (J_{SC}) [104]. Under room temperature, the space-charge generation current density is:

$$J_{SC} = \frac{qW_D n_i}{\tau_{sc}} \tag{7.1}$$

W_D is the depletion region's width, n_i is the intrinsic carrier concentration, q represents the elementary charge, and τ_{sc} is the carrier lifetime in the intrinsic area. n_i, q, and τ_{sc} are the constants at room temperature.

In the PSJ PiN junction, the depletion region is the AlGaN layer, and the W_D is its thickness. Therefore, the right side of equation (1) is constant at room temperature, representing that J_{SC} is independent of negative gate voltages.

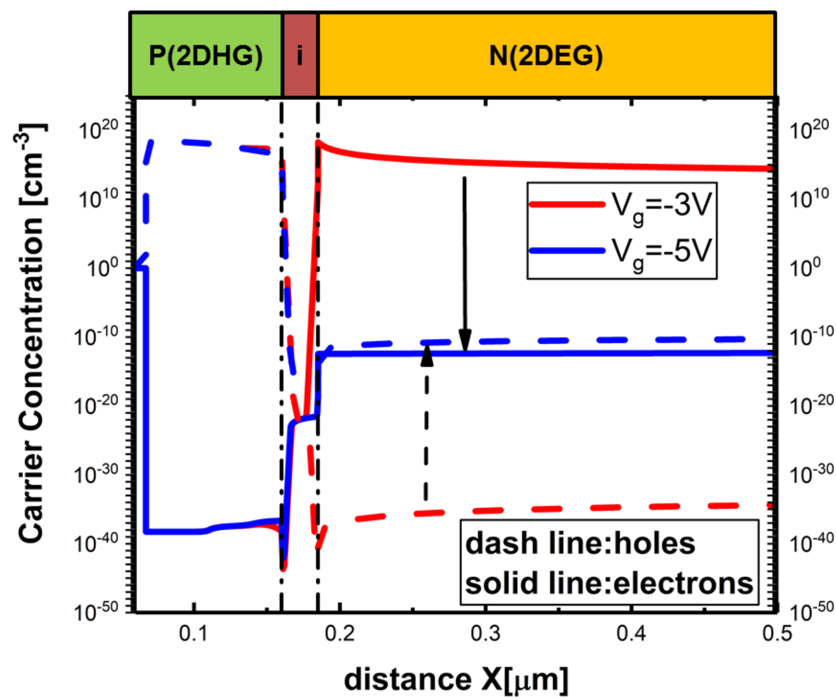


Figure 7.5 The electron and hole concentration distribution along the PSJ PiN junction under different gate biases (V_g=-3V and -5V). The blue line is for -5V and the red line is for -3V. The solid line represents the electron Concentration, and the dashed line is the hole concentration.

The J_{diff} can be divided into the electron diffusion current density (J_{dn}) and the hole diffusion current density (J_{dp}). In the vertical PiN junction of the PSJ HFETs, the expressions of J_{dn} in the N-region and J_{dp} in the P-region are [104]:

$$J_{dn} = \frac{qD_n}{L_n}\frac{{n_i}^2}{N_A}\left[\exp\left(\frac{qV_g}{kT}\right) - 1\right] \tag{7.2}$$

$$J_{dp} = \frac{qD_p}{L_p}\left[p_n(V_g) - p_{n0}\right] \tag{7.3}$$

D_n and D_p represent the electron and hole diffusion coefficients, respectively. L_n and L_p represent the electron and hole diffusion lengths, respectively. N_A is the 2DHG sheet density, and T represents the temperature. $p_n(V_g)$ represents the concentration of holes at the edge of the depletion region, which is dependent on the gate bias. p_{n0} is the minority carrier density (hole) in the N-type region(2DEG).

The electron and hole concentration distributions under different gate biases are extracted from the simulation. Figure 7.5 shows that, the electrons and holes in the P-region remain consistent with various gate biases, indicating that J_{dn} remains constant. Thus the expressions of J_{dn} in the P-region can be simplified as follows:

$$J_{dn} = \frac{qD_n}{L_n}\frac{{n_i}^2}{N_A}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] = -J_{dn0} \tag{7.4}$$

Which represents $that\ J_{dn}$ is constant.

Therefore, the reverse diffusion current of the PiN junction is dependent on J_{dp}. As Figure 7.5 illustrates, when gate bias increases from -3V to -5V, hole concentration in the N-region (2DEG) rises dramatically, causing an increase in

the J_{dp}. However, when 2DEG is completely depleted, the sheet density of 2DEG in the N-region keeps steady, resulting in $a\ J_{dp}$ constant in the saturation region. Therefore, when the gate bias is below -5V, the reversed PiN junction current is constant.

Gate leakage current characteristics of the L_{PSJ}=15um under different temperatures are shown in Figure 7.6. Gate leakage current illustrates an upward trend with the rise of the temperatures, from 25°C to 150 °C in the step of 25°C. This trend is similar to the P-GaN gate GaN HEMTs shown in [110], but I_g for PSJ HFETs has a much lower magnitude.

For the vertical PiN junction current, the gate current (I_{gV}) is proportional to the $n_i{}^2$ from equations (2) and (3). Additionally, lnn_i is proportional to $\frac{2}{T}$ [115].

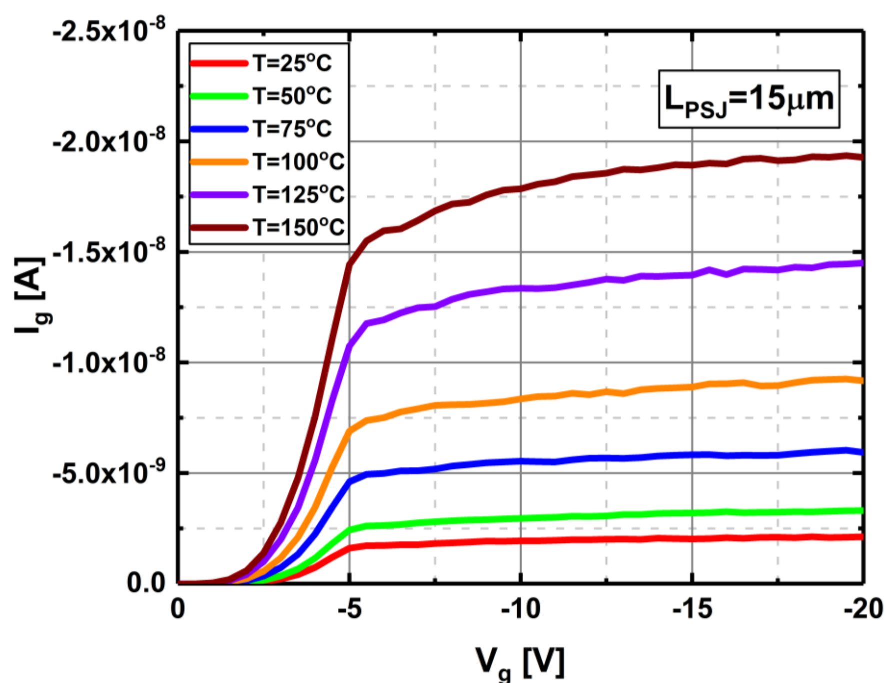


Figure 7.6 The gate leakage characteristics (Ig-Vg) of the PSJ HFETs with the length of PSJ (LPSJ) =15 um with the temperature rising from 25 °C to 150°C in steps of 25 °C.

Thus, a linear relationship between the vertical gate current (I_{gV}) and temperature ($\frac{2}{T}$) can be obtained:

$$\ln\left(I_{gV}\right) \propto \frac{2}{T} \tag{7.5}$$

Figure 7.7 presents the relationship between the I_{gv} and temperature. The linear relationship between the $\ln\left(I_{gV}\right)$ and $\frac{2}{T}$ under different gate biases can be observed. Moreover, the curves of V_g=-10V, -15V, and -20V almost coincide, but the curves of V_g=-3V and -4V are not identical with the former curve groups. These findings show that the vertical PiN junction current dominates the saturation region with the same gate leakage mechanism.

7.6. Mechanisms of gate leakage current at the non-saturation region (Vg ⩾ Vth=-5V)

Different mechanisms govern the gate leakage current in the non-saturation zone. The dominating leakage current changes to the surface leakage current at

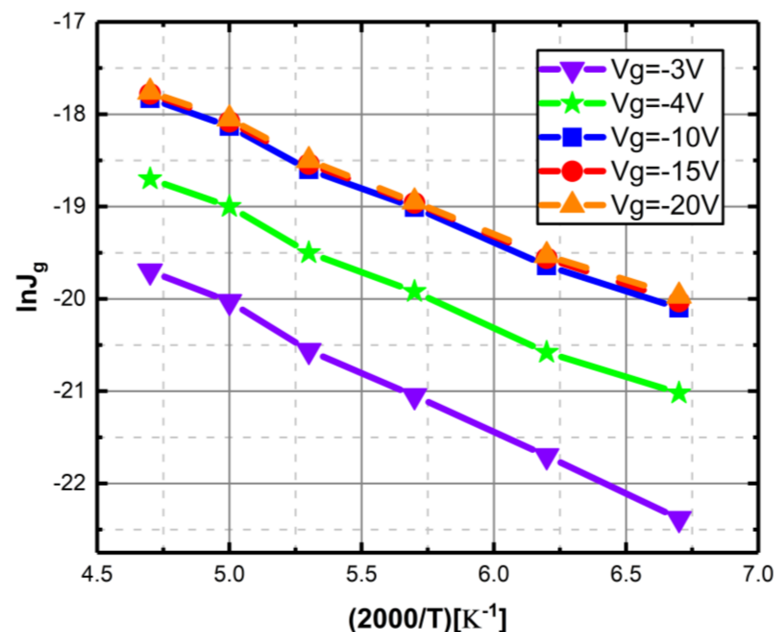


Figure 7.7 lnJg of PSJ HFETs with LPSJ=15 um as a function of the (2/T).

the comparatively low gate bias [104], [116]. The carriers are transported through the surface traps or defects, forming a conductive path between the gate and the drain or source[117].

One of the primary mechanisms that could account for the surface gate leakage currents in P-GaN gate HFETs is two-dimensional variable range hopping (2D-VRH) [110] at the low reverse gate bias and positive bias. The relationship between them can be expressed below [116]:

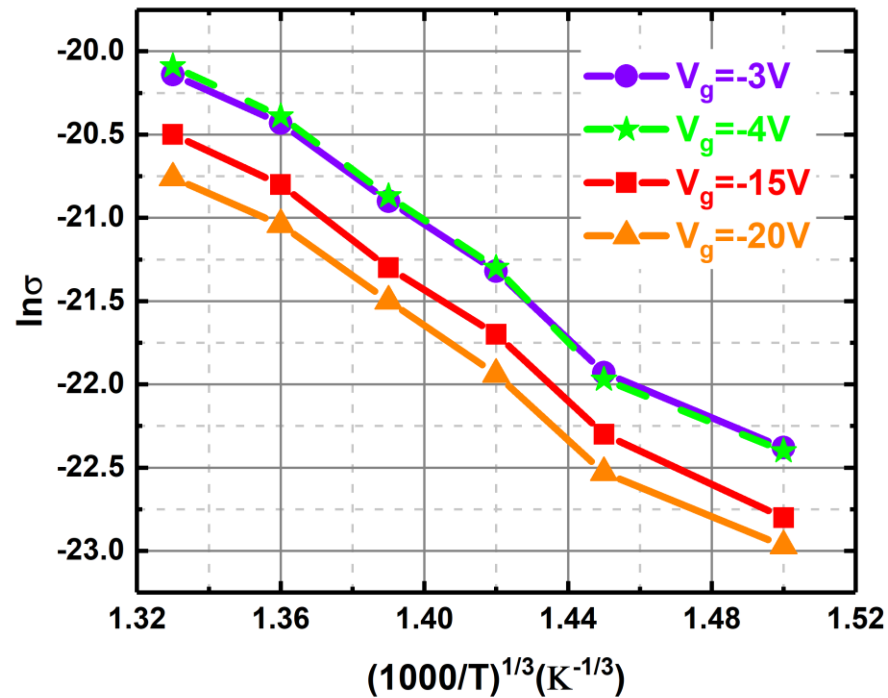
$$\sigma \propto \exp\left[-\left(\frac{1}{T}\right)^{\frac{1}{3}}\right] \tag{7.6}$$

Where σ is the conductance and T denotes the absolute temperature.

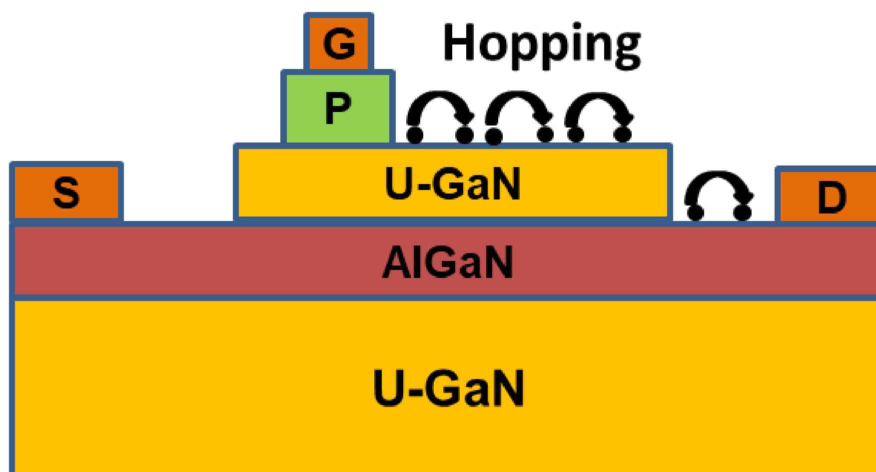
Therefore, the results of the above relationship are presented in Figure 7.8(a) at different gate biases (V_g=-3V, -4V, -15V, and -20V).

The $ln\sigma$ shows a linear relationship with $(\frac{1}{T})^{\frac{1}{3}}$, and the curve of V_g=-3V almost coincided with V_{gs}=-4V, indicating that 2D-VRH is the possible mechanism for the surface gate leakage current transportation mechanisms in the PSJ HFETs at the non-saturation region. This is identical to the gate leakage mechanism at low negative biases in P-GaN gate GaN HEMTs [110]. The 2D-VRH mechanism in PSJ HFETs is displayed in Figure 7.8(b). Carriers are transferred through the high-density electronic states along with the top u-GaN layer. However, the curves of V_g=-15V and -20V are not identical to those of V_g=-3V and -4V,

representing that the surface leakage current becomes negligible when gate biases are negatively increased.



(a)



(b)

Figure 7.8 (a)The lnσ of the PSJ HFETs as the function of $(1/T)^{1/3}$ (b) the mechanism of 2D-VRH hopping effects in PSJ HFETs.

7.7. Summary

In this chapter, the mechanisms of gate leakage current in normally-on P-ohmic gate PSJ HFETs are discussed for the first time. It can be divided into vertical PiN junction reverse current and lateral surface current in PSJ HFETs. The gate leakage current shows a unique saturation behaviour caused by the diffusion current. Moreover, the gate leakage current mechanisms are also discussed at the saturation and non-saturation regions through temperature-dependent I_g-V_g characteristics. The vertical PiN junction currents become the dominant currents at the saturation region. However, the gate leakage currents are dominated by the lateral surface current caused by the 2D-VRH mechanisms at the non-saturation region (when the gate bias is higher than -5V).

Chapter 8. Conclusions and Future work

8.1. Conclusions

GaN Polarization Superjunction (PSJ) technology utilises charge balance concepts and polarisation effects, extending the GaN power semiconductor devices to high-voltage applications. As an emerging technology, more topics on the characterisation of GaN PSJ power devices are still under investigation to further understand their mechanisms and improve their performances.

The impacts from top u-GaN and AlN nucleation layer thickness on the sheet density of 2DEG and 2DHG in the PSJ heterostructures are discussed through theoretical analysis. Moreover, the simulation and measurement results are also presented to validate and support the theoretical analysis. In u-GaN/AlGaN/u-GaN heterostructures, the relationship between the sheet density of 2DHG and the top u-GaN layer thickness mainly depends on the surface potential of the top u-GaN layer. Similar conclusions can be drawn from the PSJ heterostructures with a P-GaN cap layer. When the ohmic surface condition is applied, similar to the findings in A. Nakajima's article[85], 2DHG density slightly rises with the thickness of the top u-GaN layer. Furthermore, an investigation is being done into how the AlN nucleation layer affects 2DEG sheet density. It concludes that the relationship between the thickness of the AlN nucleation layer and the buffer GaN layer plays a critical role in determining the sheet density of 2DEG.

The introduction and discussion of the static on-state and off-state breakdown characteristics of the fabricated PSJ-on-Si HFETs and diodes at the University of Sheffield are presented. It discusses the impacts of finger length and finger quantity on current handling capacity and the Specific $R_{on}A$ of PSJ hybrid diodes on Si substrate, which is crucial for the scalability of PSJ power devices. Moreover, the effects of temperature on I-V characteristics and Specific $R_{on}A$ are also evaluated. The breakdown voltages of Sheffield PSJ hybrid diodes and HFETs are 20% and 50%, respectively, higher than those of POWDEC PSJ-on-Si power devices due to the high-resistivity C-doped GaN buffer layer, improving the vertical voltage withstanding capability. Compared with the PSJ-on-Sapphire power devices reported in [69], Sheffield PSJ-on-Si power devices have a lower breakdown voltage at the given length of PSJ, which is due to the lower vertical breakdown voltage limit of the GaN buffer grown on Si substrate.

V_{th} shift mechanisms in normally-on GaN PSJ HFETs through pulsed I_d-V_{ds} and transfer characteristics measurements under the positive and negative gate stress voltages are reported for the first time. The V_{th} shifts are also presented during the recovery processes by varying the measuring times. With the increase in the measuring times, more trapped electrons and holes will be released, causing the V_{th} shifts. Moreover, from the pulsed I_d-V_{ds} characteristics, positive and negative gate stress voltages cause a much lower magnitude of the

differences in the saturation current than P-GaN gate HEMTs, indicating that current collapse is significantly reduced in PSJ HFETs. Furthermore, the temperature effects on the Vth shifts under the positive gate stress voltages are also discussed. Compared with the P-GaN gate PSJ HFETs, the V_{th} shift in Schottky gate PSJ HFETs has different performances.

The current saturation behaviour and the saturation mechanisms of the unipolar power GaN diodes: AlGaN/GaN diode and PSJ hybrid diode are firstly reported and discussed. It is found that velocity saturation, together with the minimal conductivity modulation induced by the minority carrier in the drift region resulting in the current saturation behaviour, is the main reason for the saturation behaviour in these two diodes. Moreover, a unique current saturation behaviour of the forward I-V characteristics of the bipolar PSJ PiN diode is also discussed. Firstly, due to the low carrier lifetime and hole mobility, the conductivity modulation is negligible and localised in the PSJ PiN diode, indicating that it is one of the critical causes of this phenomenon. Moreover, trap effects are also discussed according to the simulation results.

The mechanisms of gate leakage current in normally-on P-ohmic gate PSJ HFETs are discussed for the first time. It can be divided into vertical PiN junction reverse current and lateral surface current in PSJ HFETs. The gate leakage current shows a unique saturation behaviour caused by the diffusion current. Moreover, the gate leakage current mechanisms are also discussed at

the saturation and non-saturation regions through temperature-dependent I_g-V_g characteristics. The vertical PiN junction currents become the dominant currents at the saturation region. However, the gate leakage currents are dominated by the lateral surface current caused by the 2D-VRH mechanisms at the non-saturation region (when the gate bias is higher than -5V).

8.2. Future work

This thesis presents the research on developing next-generation GaN Polarization Superjunction (PSJ) power devices. It will provide the basic knowledge for further optimisation and investigations. Therefore, future work could focus on several topics:

1. PSJ PiN diode current saturation mechanisms. The hypothetical model of explaining the PSJ PiN diode current saturation mechanisms is proposed and discussed in this thesis. It assumed that the high trap density in the AlGaN layer limits the carrier saturation velocity, causing the velocity saturation in the AlGaN layer. Although this hypothetical model has been verified in the simulation, it has no comprehensive and strong evidence from the physical theory and measurement results to support it. Therefore, investigating more evidence to validate this hypothetical model will become one of the most essential next-step works.

2. Avalanche capability of PSJ HFETs and PSJ diode. Power semiconductor devices' avalanche capability and robustness under extreme conditions are

essential for high-power applications. Unclamped Inductive Switching (UIS) is the standard method to evaluate the avalanche capability of power devices. PSJ power devices include an inherent PiN diode compared to AlGaN/GaN HEMTs, which may improve avalanche capability.

3. Comparison of the Avalanche capability and mechanism between GaN and Si or SiC power devices. Some research has reported the avalanche capability of Si or SiC and GaN power devices separately. Therefore, evaluating their avalanche capability is essential.

4. Current Collapse of PSJ HFETs. One of the essential dynamic properties of GaN power devices is the current collapse, also known as the degradation of dynamic on-state resistance. Power loss during switching increases as the dynamic R_{on} increases. Moreover, three main factors are responsible for the current collapse: surface trap, buffer trap and V_{th} instability. PSJ HFETs have a flat electric field during the off-state, which minimises the influence of the surface trap. The relatively low current collapse induced by the V_{th} instability is reported in this thesis. However, the trend analysis of the current collapse of PSJ HFETs requires further investigation.

5. PSJ Hybrid drain HFETs. PSJ HFETs have relatively higher specific on-state resistance than conventional AlGaN/GaN HEMTs, indicating the higher conduction loss of PSJ HFETs. Therefore, lowering the on-state resistance of PSJ HFETs is becoming a heated topic. PSJ hybrid drain HFETs utilised a similar

structure to the Panasonic Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT). The holes are injected from the P-type drain, causing conductivity modulation and reducing on-state resistance. Moreover, the current collapse can also be minimised by the injected holes during the off-state. However, the impacts from injected holes on the charge balance in PSJ HFETs need to be evaluated. More measured data from them is required from the actual devices to support this concept further.

6. PSJ HFETs switching performance. PSJ switching simulation and modelling are crucial to determine the turn-on and turn-off performance. It might be possible to reduce power loss based on switching performance. At present, P-GaN gate PSJ HFETs have relatively slower switching speeds. Thus improving the switching speed and lowering the switching loss is very significant for PSJ HFETs. The main cause is the low charging/discharging speed of the 2DHG through the P-GaN gate. Therefore, optimising the gate structure of PSJ HFETs may be one of the possible solutions. Moreover, several topics could be investigated: (1) Investigation of dV/dt Controllability of PSJ FETs. For example, gate resistance may influence the controllability of PSJ HFETs. (2) Impact of Gate Voltage on Inductive Switching Performance of PSJ FETs. For example, the positive gate turn-on and negative gate turn-off levels impact the switching performance. (3) the switching performance between PSJ P-GaN gate HFETs and PSJ Schottky-gate HFETs.

Appendix-1

Mask design

According to the process flow, it requires 11 masks in total. The mask layers information is shown in detail in Table A-0-1.

Table A-0-1 Mask layer information.

Mask No.	Alias	Abbr	Aligned to	Toner	Process
0	Alignment Mark	AM	--	C	--
1	Device Isolation	DI	AM	D	Etch
2	Pad Insulation	PI	AM	C	Etch
3	Mesa Etch	ME	AM	D	Etch
4	N Contact	NC	AM	C	CVD
5	P Contact	PC	NC	C	CVD
6	P-GaN Etch	PE	PC	C	Etch
7	Gate Contact	GC	PC	C	CVD
8	Via	VIA	NC	C	Etch
9	Metal 2	M2	PC	C	CVD
10	Passivation	PV	PC	C	Etch

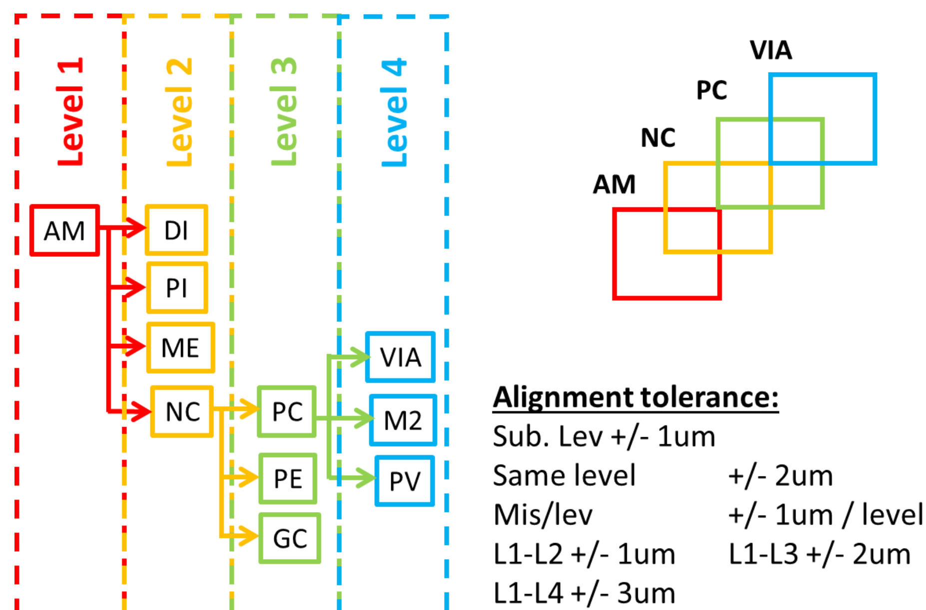


Figure A.0.1 Mask alignment sequence and alignment tolerance rules.

And the multi-level mask alignment is utilised in the mask design for minimising misalignment between each mask layer. The alignment sequence and the alignment tolerance rules are shown in Figure A.0.1 Mask alignment sequence and alignment tolerance rules. The alignment tolerances between the mask from the same level are +/- 2um, but the misalignment between different levels of the mask layer is +/- 1um. And based on the alignment sequence and misalignment rules, the unit cell dimensions of PSJ HFET are shown in Figure A.0.2.

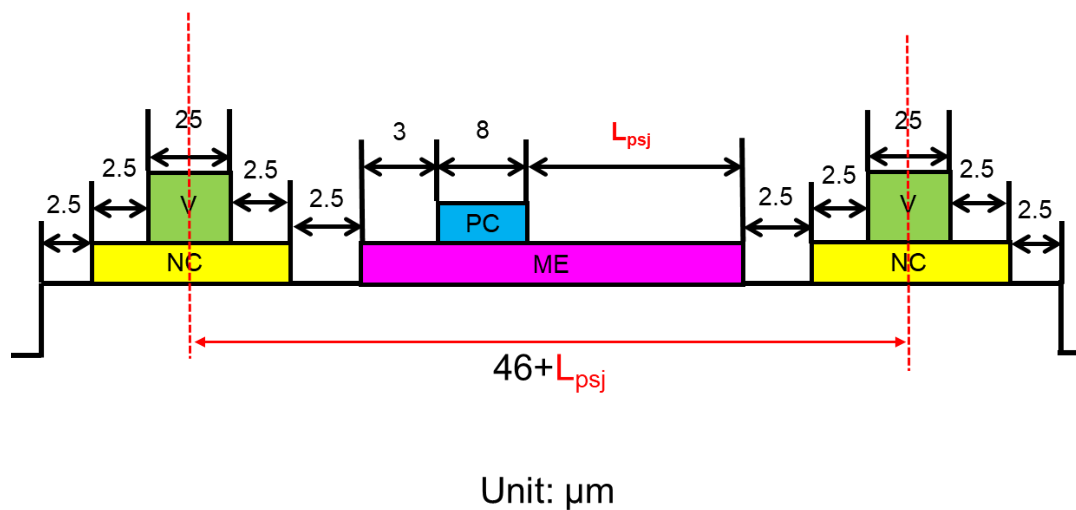


Figure A.0.2 The unit cell dimensions of PSJ HFET are based on the mask alignment tolerance rules.

The mask design is drawn through the software Klayout. It is important to note that the toner of each mask shown in Table A-0-1 depends on each mask's

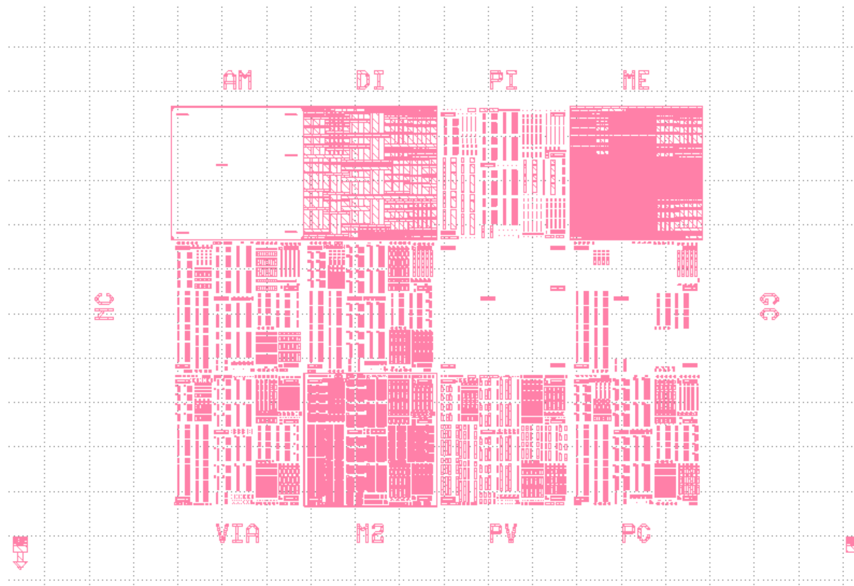


Figure A.0.3 The final photograph of the mask layout.

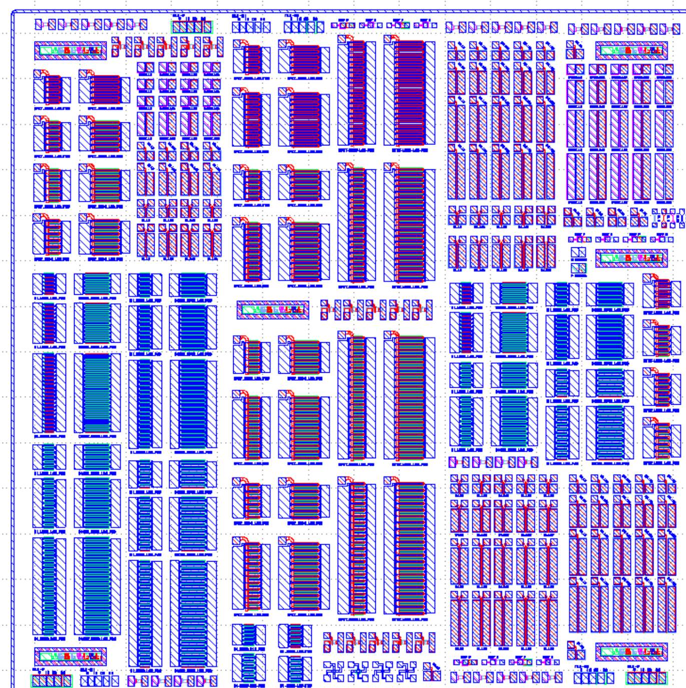


Figure A.0.4 The photograph of the mask design.

functionality and photoresist polarisation. All the photoresist used for the fabrication is positive photoresists. C and D represent the clear and dark field, respectively. The photograph of the mask design and the final mask layout is illustrated in Figure A.0.4 and Figure A.0.3, respectively.

Sample dicing size and cleaning preparation steps

Before the fabrication started, the 3-inch wafer was diced into small-piece samples according to the mask size (15mm×15mm). Therefore, the sample size is 18mm×18mm, which meets the requirement for tolerances during the fabrication process.

The typical 3-step cleaning procedures:

1. Put the sample into the n-butyl Acetate and cook them on a hot plate for 1 min. This step aims to remove the oil or oily solution from the sample.

2. Then, the sample is transferred to the Acetone for 30 seconds and gently dipped.

3. Finally, the sample is rinsed into the Isopropyl Alcohol (IPA) for 30 seconds. After that, the sample is blow-dried through an N_2 flow gun. The dry samples are checked under the microscope to ensure that surface is clean. If not, they repeat the 3-step cleaning procedures until the sterile surface is obtained.

It is important to note that this cleaning procedure was employed before each step started during this fabrication process.

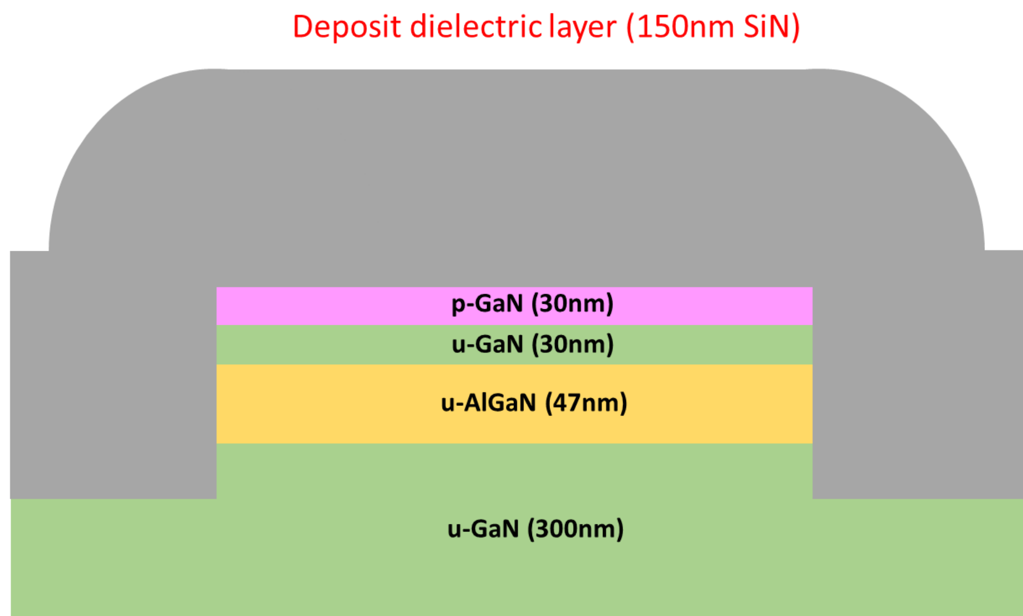
Fabrication process flow

1. Alignment Mark

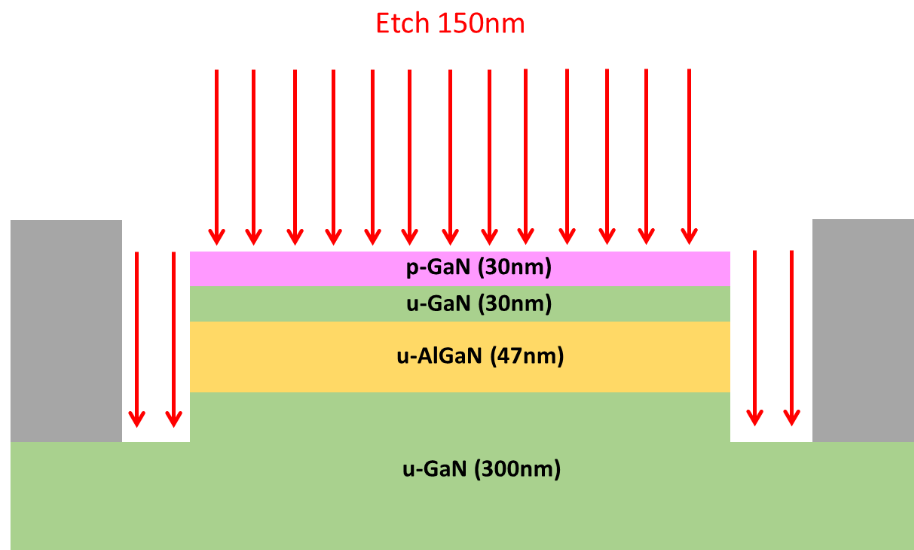
2. Isolation etching

Figure 0.5 The schematic cross-section of devices after device Isolation etching.

3. Pad Insulation



(a)



(b)

Figure 0.7 The schematic cross-section of devices (a)after depositing the 150 nm-SiN dielectric layers (b) after etching the 150 nm-SiN dielectric layers on the active area.

4. Mesa Etching

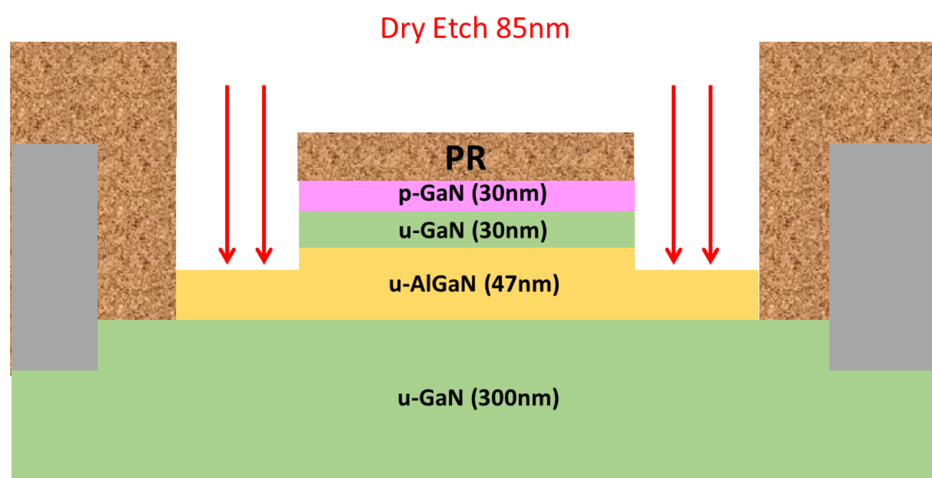


Figure 0.6 The schematic cross-section of devices after mesa etching.

4. N-ohmic Contact

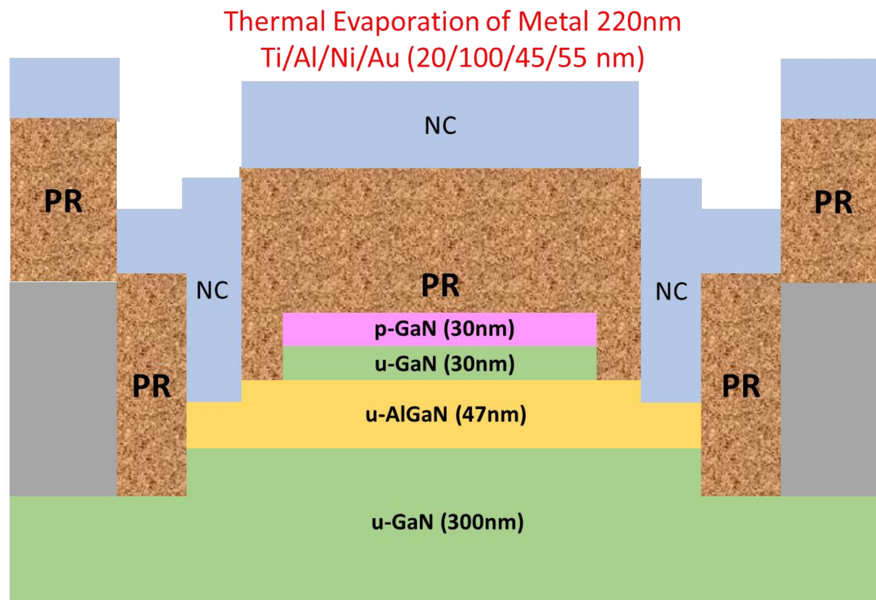


Figure 0.9 The schematic cross-section of the device after N-contact metallisation.

5. P-ohmic contact

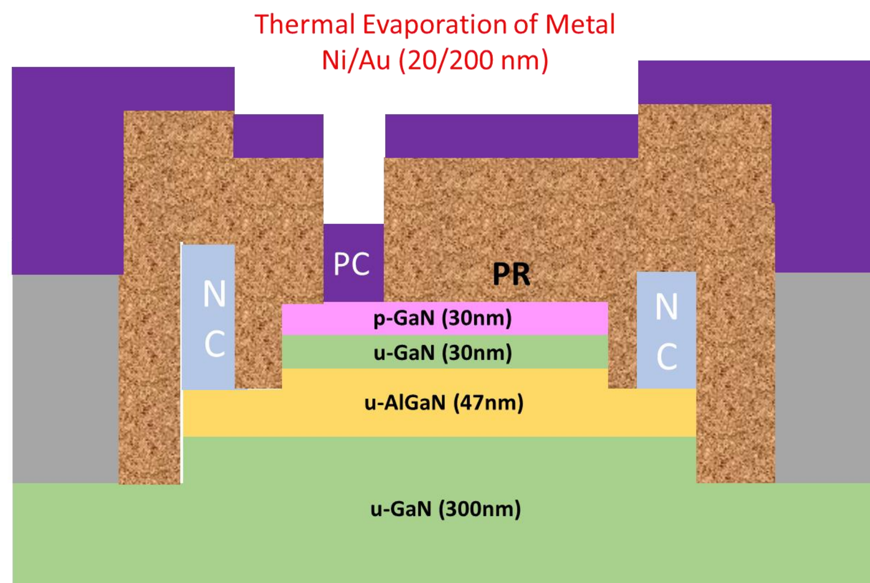
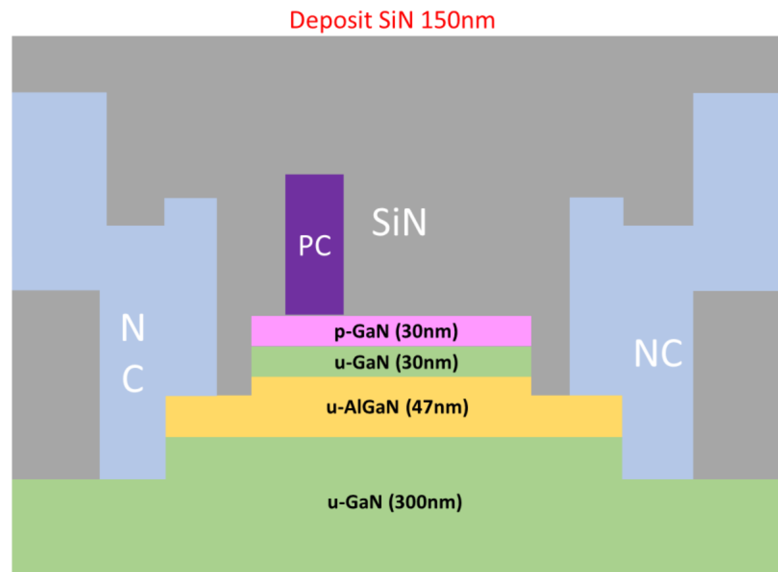
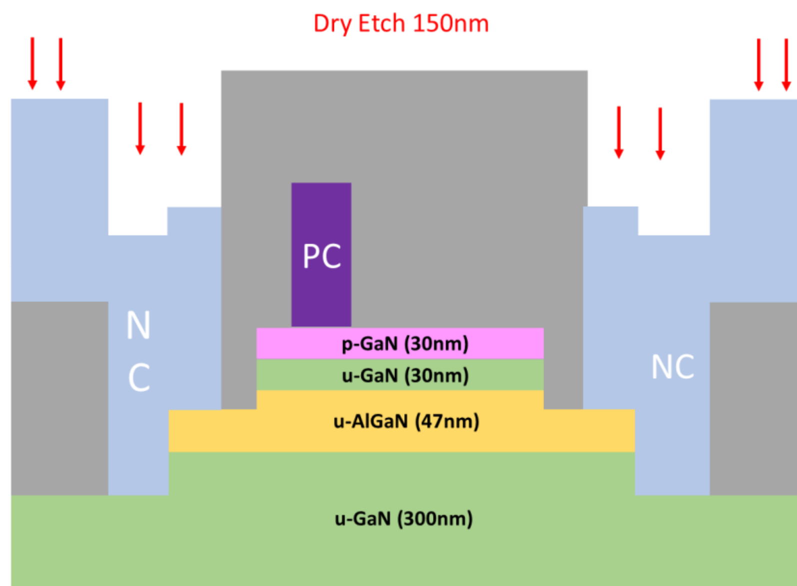


Figure 0.8 The schematic cross-section of devices of P-ohmic deposition.

6. Via etching



(a)



(b)

Figure 0.10 The schematic cross-section of devices(a) PECVD 150nm-SiN (b)SiN via etching through RIE.

7.Second Metallisation(M2)

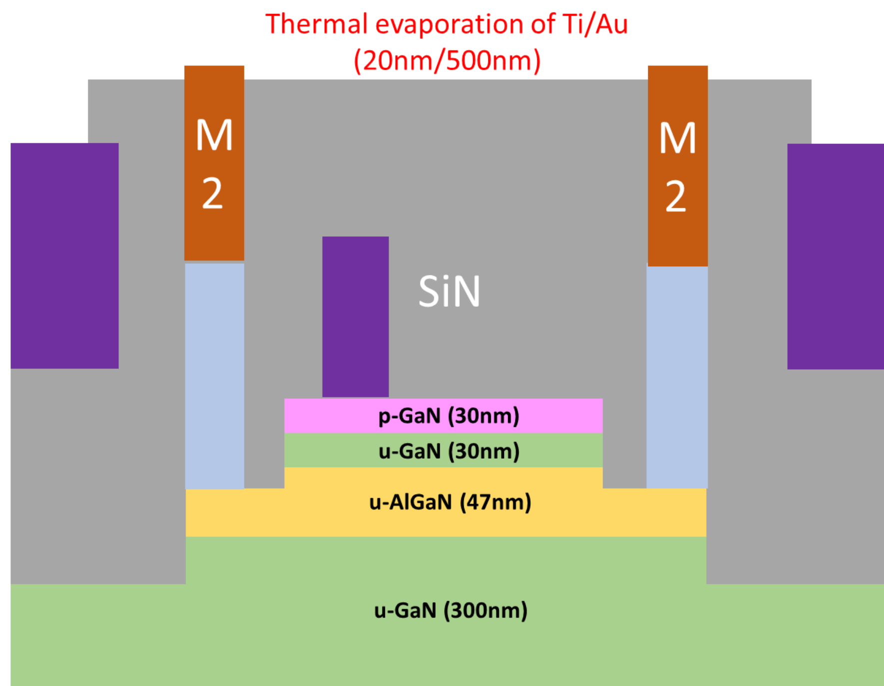
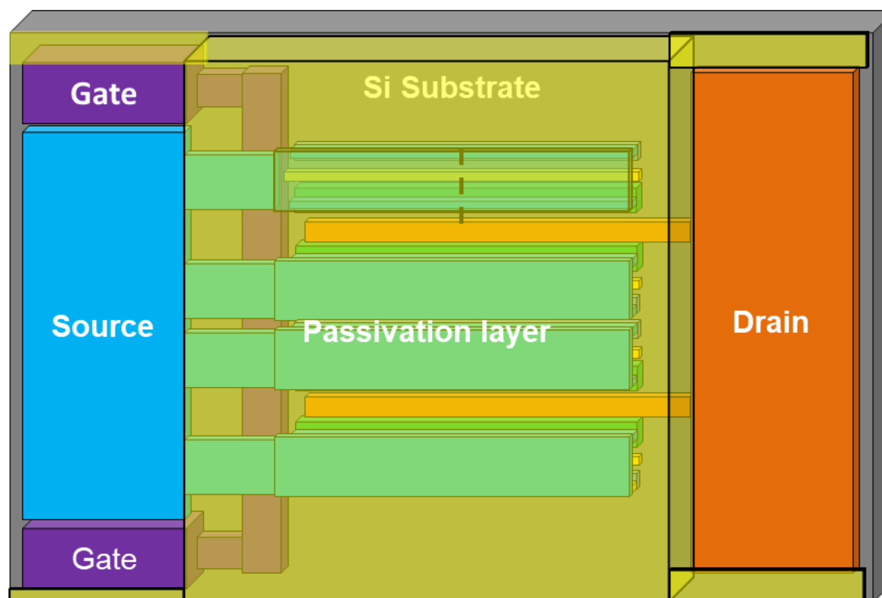
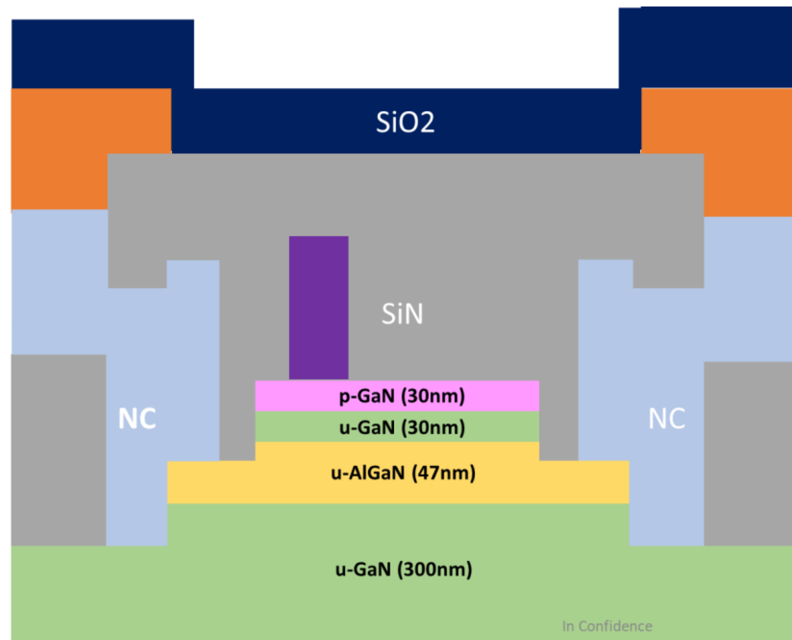


Figure 0.11 The schematic cross-section of devices after M2.

8. Pad and Passivation



(a)



(b)

Figure 0.12 (a) the 3D-schematic cross-section of the large-area devices (b) the schematic cross-section of the active area of the devices after passivation and RIE etching

Fabricated devices/sample

The photograph of the final fabricated PSJ-on-Si sample is displayed in Figure 0.13.

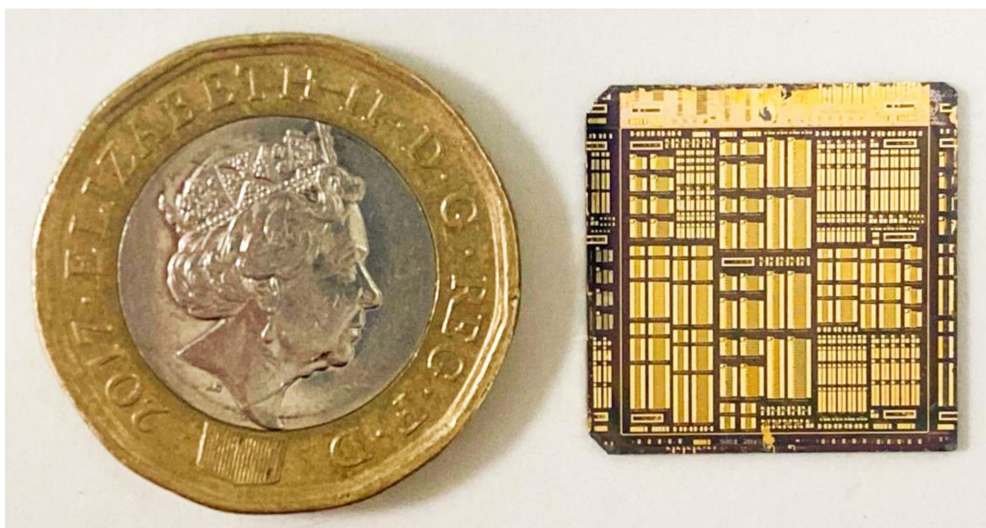


Figure 0.13 The photograph of fabricated PSJ-on-Si sample(18mm×18mm) at Sheffield compared with a one-pound coin.

Appendix-2: References

[1] "POWDEC K.K. | Products | Device." [Online]. Available: https://www.powdec.co.jp/english/products/device/index.php. [Accessed: 11-Oct-2022].

[2] "POWDEC K.K. | Business | ." [Online]. Available: http://powdec.co.jp/english/business/index.php. [Accessed: 11-Oct-2022].

[3] "International Energy Outlook 2021 - U.S. Energy Information Administration (EIA)." [Online]. Available: https://www.eia.gov/outlooks/ieo/. [Accessed: 30-May-2022].

[4] "Status of the Power Electronics Industry 2021 - i-Micronews." [Online]. Available: https://www.i-micronews.com/products/status-of-the-power-electronics-industry-2021/?utm_source=PR&utm_medium=email&utm_campaign=PR_POWER_ELECTRONICS_INDUSTRY_DISCRETE_DEVICES_YOLEGROUP_Nov2021&cn-reloaded=1. [Accessed: 30-May-2022].

[5] "GaN Power 2021: Epitaxy, Devices, Applications and Technology Trends - i-Micronews." [Online]. Available: https://www.i-micronews.com/products/gan-power-2021-epitaxy-devices-applications-and-technology-trends/?utm_source=PR&utm_medium=email&utm_campaign=PR_PO

WER_GAN_EPITAXY_DEVICES_APPLICATIONS_TECHNOLOGY_TRENDS_YOLE_May2021. [Accessed: 30-May-2022].

[6] X. Ding, Y. Zhou, and J. Cheng, "A review of gallium nitride power device and its applications in motor drive," *CES Trans. Electr. Mach. Syst.*, vol. 3, no. 1, pp. 54–64, 2019.

[7] M. Meneghini, G. Meneghesso, and E. Zanoni, *Power GaN Devices: Materials, Applications and Reliability*. 2017.

[8] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907–914, 2003.

[9] O. Ambacher and V. Cimalla, "Polarization Induced Effects in GaN-based Heterostructures and Novel Sensors," in *Polarization Effects in Semiconductors: From Ab InitioTheory to Device Applications*, 2008, pp. 27–109.

[10] F. Bernardini, "Spontaneous and Piezoelectric Polarization: Basic Theory vs. Practical Recipes," in *Nitride Semiconductor Devices: Principles and Simulation*, 2007, pp. 49–68.

[11] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, 1989.

[12] B. J. Baliga, "Semiconductors for high-voltage, vertical channel field-effect transistors," *J. Appl. Phys.*, vol. 53, no. 3, pp. 1759–1764, Mar. 1982.

[13] A. Q. Huang, "New unipolar switching power device figures of merit," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 298–301, 2004.

[14] W. S. Tan, M. J. Uren, P. W. Fry, P. A. Houston, R. S. Balmer, and T. Martin, "High temperature performance of AlGaN/GaN HEMTs on Si substrates," *Solid. State. Electron.*, vol. 50, no. 3, pp. 511–513, 2006.

[15] R. Cuerdo *et al.*, "High temperature behaviour of GaN HEMT devices on Si(111) and sapphire substrates," *Phys. status solidi c*, vol. 5, no. 6, pp. 1971–1973, May 2008.

[16] D. Maier *et al.*, "Testing the Temperature Limits of GaN-Based HEMT Devices," *IEEE Trans. Device Mater. Reliab.*, vol. 10, no. 4, pp. 427–436, 2010.

[17] M. Meneghini *et al.*, "GaN-based power devices: Physics, reliability, and perspectives," *Journal of Applied Physics*, vol. 130, no. 18. American Institute of Physics Inc., 14-Nov-2021.

[18] L. Liu and J. H. Edgar, "Substrates for gallium nitride epitaxy," *Mater. Sci. Eng. R Reports*, vol. 37, no. 3, pp. 61–127, 2002.

[19] N.-. Zhang, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Effects of surface traps on breakdown voltage and switching

speed of GaN power switching HEMTs," in *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, 2001, pp. 25.5.1-25.5.4.

[20] S. Q. Zhou, A. Vantomme, B. S. Zhang, H. Yang, and M. F. Wu, "Comparison of the properties of GaN grown on complex Si-based structures," *Appl. Phys. Lett.*, vol. 86, no. 8, p. 81912, Feb. 2005.

[21] A. Dadgar *et al.*, "Epitaxy of GaN on silicon—impact of symmetry and surface reconstruction," *New J. Phys.*, vol. 9, no. 10, p. 389, 2007.

[22] D. Zhao and D. Zhao, "Analysis of the growth of GaN epitaxy on silicon," *J. Semicond.*, vol. 39, no. 3, p. 33006, 2018.

[23] "Market Research Reports - Research and Markets - Page gone." [Online]. Available: https://www.researchandmarkets.com/reports/4831765/gan-on-sapphire-hemt-power-ic-by-power?utm_source=dynamic&utm_medium=GNOM&utm_code=jf9t84&utm_campaign=1320574+-+GaN-on-Sapphire+HEMT+Power+IC+by+Power+Integrations+-+2019+Production+Cost%2C+Selling+Price+%26+Comparison+Report&utm_exec=joca220gnomd#. [Accessed: 24-Sep-2022].

[24] "Transphorm to Demonstrate 99% Efficiency Power Switching with a 1200 Volt GaN Power Transistor at ISPSD 2022 - Transphorm." [Online]. Available:

https://www.transphormchina.com/en/news/1200v_gan_ispsd/. [Accessed: 24-Sep-2022].

[25] D. Bisi *et al.*, "Commercially Available N-polar GaN HEMT Epitaxy for RF Applications," in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2021, pp. 250–254.

[26] S. Keller *et al.*, "Recent progress in metal-organic chemical vapor deposition of N-polar group-III nitrides," *Semicond. Sci. Technol.*, vol. 29, no. 11, p. 113001, 2014.

[27] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B*, vol. 56, no. 16, pp. R10024–R10027, Oct. 1997.

[28] J. F. Nye and P. P. L. J. F. Nye, *Physical Properties of Crystals: Their Representation by Tensors and Matrices*. Clarendon Press, 1985.

[29] M. Posternak, A. Baldereschi, A. Catellani, and R. Resta, "Ab initio study of the spontaneous polarization of pyroelectric BeO," *Phys. Rev. Lett.*, vol. 64, no. 15, pp. 1777–1780, Apr. 1990.

[30] U. Mishra and J. Singh, *Semiconductor Device Physics and Design*. Springer Netherlands, 2007.

[31] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face

AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999.

[32] O. Ambacher *et al.*, "Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures," *J. Phys. Condens. Matter*, vol. 14, no. 13, pp. 3399–3434, 2002.

[33] I. Vurgaftman and J. R. Meyer, "Band parameters for nitrogen-containing semiconductors," *J. Appl. Phys.*, vol. 94, no. 6, pp. 3675–3696, Aug. 2003.

[34] H. Morkoç and J. Leach, "Polarization in GaN Based Heterostructures and Heterojunction Field Effect Transistors (HFETs)," in *Polarization Effects in Semiconductors: From Ab InitioTheory to Device Applications*, 2008, pp. 373–466.

[35] O. Ambacher *et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 87, no. 1, pp. 334–344, Dec. 1999.

[36] E. T. Yu, G. J. Sullivan, P. M. Asbeck, C. D. Wang, D. Qiao, and S. S. Lau, "Measurement of piezoelectrically induced charge in GaN/AlGaN heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 71, no. 19, pp. 2794–2796, Nov. 1997.

[37] M. A. Khan, J. N. Kuznia, J. M. Van Hove, N. Pan, and J. Carter, "Observation of a two-dimensional electron gas in low pressure

metalorganic chemical vapor deposited GaN-AlxGa1−xN heterojunctions," *Appl. Phys. Lett.*, vol. 60, no. 24, pp. 3027–3029, Jun. 1992.

[38] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 77, no. 2, pp. 250–252, Jun. 2000.

[39] S. Heikman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars, and U. K. Mishra, "Polarization effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 93, no. 12, pp. 10114–10118, May 2003.

[40] I. P. Smorchkova *et al.*, "Polarization-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy," *J. Appl. Phys.*, vol. 86, no. 8, pp. 4520–4526, Sep. 1999.

[41] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs/n-$Al_xGa_{1-x}As$ Heterojunctions," *Jpn. J. Appl. Phys.*, vol. 19, no. 5, pp. L225–L227, 1980.

[42] N. H. Sheng, C. P. Lee, R. T. Chen, and D. L. Miller, "GaAs/AlGaAs double heterostructure high electron mobility transistors," in *1984 International Electron Devices Meeting*, 1984, pp. 352–355.

[43] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, “High electron mobility transistor based on a GaN-AlxGa1−xN heterojunction,” *Appl. Phys. Lett.*, vol. 63, no. 9, pp. 1214–1215, Aug. 1993.

[44] M. Asif Khan, J. N. Kuznia, A. R. Bhattarai, and D. T. Olson, “Metal semiconductor field effect transistor based on single crystal GaN,” *Appl. Phys. Lett.*, vol. 62, no. 15, pp. 1786–1787, Apr. 1993.

[45] V. Unni, *Next-generation GaN Power Semiconductor Devices*. University of Sheffield, 2015.

[46] D. Balaz, *Current Collapse and Device Degradation in AlGaN/GaN Heterostructure Field Effect Transistors*. University of Glasgow, 2010.

[47] A. Nakajima, M. H. Dhyani, E. M. S. Narayanan, Y. Sumida, and H. Kawai, “GaN based Super HFETs over 700V using the polarization junction concept,” in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, 2011, pp. 280–283.

[48] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and T. Ogura, “Design and Demonstration of High Breakdown Voltage GaN High Electron Mobility Transistor (HEMT) Using Field Plate Structure for Power Electronics Applications,” *Jpn. J. Appl. Phys.*, vol. 43, no. 4B, pp. 2239–2242, 2004.

[49] R. Coffie, “Analytical Field Plate Model for Field Effect Transistors,” *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 878–883, 2014.

[50] S. Karmalkar, M. S. Shur, G. Simin, and M. A. Khan, “Field-plate engineering for HFETs,” *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2534–2540, 2005.

[51] S. Karmalkar and U. K. Mishra, “Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate,” *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515–1521, 2001.

[52] Y. Dora, A. Chakraborty, L. Mccarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, “High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates,” *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 713–715, 2006.

[53] I. Rossetto *et al.*, “Field-Related Failure of GaN-on-Si HEMTs: Dependence on Device Geometry and Passivation,” *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 73–77, 2017.

[54] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, “Design optimization of high breakdown voltage AlGaN-GaN power HEMT on an insulating substrate for R/sub ON/A-V/sub B/ tradeoff characteristics,” *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 106–111, 2005.

[55] V. Kumar, G. Chen, S. Guo, and I. Adesida, “Field-plated 0.25-/spl mu/m gate-length AlGaN/GaN HEMTs with varying field-plate length,” *IEEE Trans. Electron Devices*, vol. 53, no. 6, pp. 1477–1480, 2006.

[56] R. Chu *et al.*, “1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic on -Resistance,” *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 632–634, 2011.

[57] J. A. Appels and H. M. J. Vaes, “High voltage thin layer devices (RESURF devices),” in *1979 International Electron Devices Meeting*, 1979, pp. 238–241.

[58] H. M. J. Vaes and J. A. Appels, “High voltage, high current lateral devices,” in *1980 International Electron Devices Meeting*, 1980, pp. 87–90.

[59] J. S. Ajit, D. Kinzer, and N. Ranjan, “1200 V high-side lateral MOSFET in junction-isolated power IC technology using two field-reduction layers,” in *[1993] Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs*, 1993, pp. 230–235.

[60] A. W. Ludikhuize, *A review of RESURF technology*. 2000.

[61] F. Udrea, A. Popescu, and W. Milne, “3D RESURF double-gate MOSFET: a revolutionary power device concept,” *Electron. Lett.*, vol. 34, pp. 808–809, May 1998.

[62] T. Fujihira, “Theory of Semiconductor Superjunction Devices,” *Jpn. J. Appl. Phys.*, vol. 36, no. Part 1, No. 10, pp. 6254–6262, 1997.

[63] P. M. Shenoy, A. Bhalla, and G. M. Dolny, “Analysis of the effect of charge imbalance on the static and dynamic characteristics of the super junction MOSFET,” in *11th International Symposium on Power*

Semiconductor Devices and ICs. ISPSD'99 Proceedings (Cat. No.99CH36312), 1999, pp. 99–102.

[64] A. Nakajima, K. Adachi, M. Shimizu, and H. Okumura, *Improvement of Unipolar Power Device Performance Using a Polarization Junction*, vol. 89. 2006.

[65] G. Deboy, N. Marz, J. .-P. Stengl, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in *International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, 1998, pp. 683–685.

[66] S. Kunori, M. Kitada, T. Shimizu, K. Oshima, and A. Sugai, *120 V multi RESURF junction barrier Schottky rectifier (MR-JBS)*. 2002.

[67] F. Udrea, G. Deboy, and T. Fujihira, "Superjunction Power Devices, History, Development, and Future Prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 713–727, 2017.

[68] A. Nakajima, Y. Sumida, M. Dhyani, H. Kawai, and S. Ekkanath Madathil, *High Density Two-Dimensional Hole Gas Induced by Negative Polarization at GaN/AlGaN Heterointerface*, vol. 3. 2010.

[69] H. Kawai *et al.*, "Low cost high voltage GaN polarization superjunction field effect transistors," *Phys. status solidi*, vol. 214, no. 8, p. 1600834, Aug. 2017.

[70] H. Yan, Y. Du, P. Luo, X. Tan, and E. M. S. Narayanan, “Analytical Modeling of Sheet Carrier Density and on-Resistance in Polarization Super-Junction HFETs,” *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5714–5719, 2021.

[71] V. Unni *et al.*, *2.4kV GaN Polarization Superjunction Schottky Barrier Diodes on semi-insulating 6H-SiC substrate*. 2014.

[72] A. Nakajima *et al.*, “GaN-based bidirectional super HFETs using polarization junction concept on insulator substrate,” in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2012.

[73] B. Song, M. Zhu, Z. Hu, K. Nomoto, D. Jena, and H. G. Xing, “Design and optimization of GaN lateral polarization-doped super-junction (LPSJ): An analytical study,” in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC’s (ISPSD)*, 2015, pp. 273–276.

[74] S. Han, S. Yang, and K. Sheng, “Conductivity Modulation in Vertical GaN PiN Diode: Evidence and Impact,” *IEEE Electron Device Lett.*, vol. 42, no. 3, pp. 300–303, 2021.

[75] S.-W. Han, J. Song, and R. Chu, “Design of GaN/AlGaN/GaN Super-Heterojunction Schottky Diode,” *IEEE Trans. Electron Devices*, vol. 67, no. 1, pp. 69–74, 2020.

[76] S. Yang, S. Han, K. Sheng, and K. J. Chen, “Dynamic On-Resistance in GaN Power Devices: Mechanisms, Characterizations, and Modeling,” *IEEE J. Emerg. Sel. Top. Power Electron.*, 2019.

[77] B. Luo *et al.*, “Comparison of surface passivation on films for reduction of current collapse in AlGaN/GaN high electron mobility transistors,” in *Proceedings. IEEE Lester Eastman Conference on High Performance Devices*, 2002, pp. 477–486.

[78] W. Saito *et al.*, “Field-Plate Structure Dependence of Current Collapse Phenomena in High-Voltage GaN-HEMTs,” *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 659–661, 2010.

[79] M. J. Uren *et al.*, “Intentionally Carbon-Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths,” *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 327–329, 2014.

[80] S. Yang, S. Liu, Y. Lu, and K. J. Chen, “Trapping mechanisms in insulated-gate GaN power devices: Understanding and characterization techniques,” *Phys. status solidi*, vol. 214, no. 3, p. 1600607, Mar. 2017.

[81] T. R. Prunty, J. A. Smart, E. N. Chumbes, B. K. Ridley, L. F. Eastman, and J. R. Shealy, “Passivation of AlGaN/GaN heterostructures with silicon nitride for insulated gate transistors,” in *Proceedings 2000 IEEE/ Cornell Conference on High Performance Devices (Cat. No.00CH37122)*, 2000, pp. 208–214.

[82] H. Hahn, M. Uren, and A. Vescan, "Threshold Voltage Engineering of GaN-based n-Channel and p-Channel Heterostructure Field Effect Transistors," 2015.

[83] H. Hahn *et al.*, "Charge balancing in GaN-based 2-D electron gas devices employing an additional 2-D hole gas and its influence on dynamic behaviour of GaN-based heterostructure field effect transistors," *J. Appl. Phys.*, 2015.

[84] A. Kumar and M. M. De Souza, "Modelling the threshold voltage of p-channel enhancement-mode GaN heterostructure field-effect transistors," *IET Power Electron.*, vol. 11, no. 4, pp. 675–680, Apr. 2018.

[85] A. Nakajima *et al.*, "Generation and transportation mechanisms for two-dimensional hole gases in GaN/AlGaN/GaN double heterostructures," *J. Appl. Phys.*, 2014.

[86] W. Zhang, E. Simoen, M. Zhao, and J. Zhang, "Analysis of Leakage Mechanisms in AlN Nucleation Layers on p-Si and p-SOI Substrates," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 1849–1855, 2019.

[87] P. Waltereit *et al.*, "Influence of AlN nucleation layers on growth mode and strain relief of GaN grown on 6H-SiC(0001)," *Appl. Phys. Lett.*, 1999.

[88] K. J. Chen *et al.*, *GaN-on-Si Power Technology: Devices and Applications*, vol. 64. 2017.

[89] A. Pérez-Tomás *et al.*, "GaN transistor characteristics at elevated temperatures," *J. Appl. Phys.*, vol. 106, no. 7, p. 74519, Oct. 2009.

[90] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *J. Phys. D. Appl. Phys.*, vol. 51, no. 16, p. 163001, 2018.

[91] Y. C. Choi, M. Pophristic, B. Peres, H.-Y. Cha, M. G. Spencer, and L. F. Eastman, "High breakdown voltage C-doped GaN-on-sapphire HFETs with a low specific on-resistance," *Semicond. Sci. Technol.*, vol. 22, no. 5, pp. 517–521, 2007.

[92] Y. C. Choi, L. F. Eastman, and M. Pophristic, "Effects of an Fe-doped GaN Buffer in AlGaN/GaN Power HEMTs on Si Substrate," in *2006 European Solid-State Device Research Conference*, 2006, pp. 282–285.

[93] F. Medjdoub, M. Zegaoui, B. Grimbert, N. Rolland, and P.-A. Rolland, "Effects of AlGaN Back Barrier on AlN/GaN-on-Silicon High-Electron-Mobility Transistors," *Appl. Phys. Express*, vol. 4, no. 12, p. 124101, 2011.

[94] S. Kato, Y. Satoh, H. Sasaki, I. Masayuki, and S. Yoshida, "C-doped GaN buffer layers with high breakdown voltages for high-power operation AlGaN/GaN HFETs on 4-in Si substrates by MOVPE," *J. Cryst. Growth*, vol. 298, pp. 831–834, 2007.

[95] M. Meneghini, O. Hilt, J. Wuerfl, and G. Meneghesso, "Technology and Reliability of Normally-Off GaN HEMTs with p-Type Gate," *Energies* , vol. 10, no. 2. 2017.

[96] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Mechanism of Threshold Voltage Shift in p-GaN Gate AlGaN/GaN Transistors," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1145–1148, 2018.

[97] A. Stockman, E. Canato, M. Meneghini, G. Meneghesso, P. Moens, and B. Bakeroot, "Threshold Voltage Instability Mechanisms in p-GaN Gate AlGaN/GaN HEMTs," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, pp. 287–290.

[98] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold Voltage Instability in p-GaN Gate AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, 2018.

[99] D. Bisi *et al.*, "Deep-Level Characterization in GaN HEMTs-Part I: Advantages and Limitations of Drain Current Transient Measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, 2013.

[100] M. Kuzuhara, J. T. Asubar, and H. Tokuda, "AlGaN/GaN high-electron-mobility transistor technology for high-voltage and low-on-resistance operation," *Jpn. J. Appl. Phys.*, vol. 55, no. 7, p. 70101, 2016.

[101] A. M. Angelotti, G. P. Gibiino, C. Florian, and A. Santarelli, "Trapping Dynamics in GaN HEMTs for Millimeter-Wave Applications: Measurement-Based Characterization and Technology Comparison," *Electronics* , vol. 10, no. 2. 2021.

[102] G. Meneghesso *et al.*, "Trapping phenomena in AlGaN/GaN HEMTs: a study based on pulsed and transient measurements," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 74021, 2013.

[103] A. Nigam, T. Bhat, S. Rajamani, D. Surani, S. Tripathy, and M. Kumar, *Effect of self-heating on electrical characteristics of AlGaN/ GaN HEMT on Si (111) substrate*, vol. 7. 2017.

[104] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. Springer Publishing Company, Incorporated, 2008.

[105] D. Disney, H. Nie, A. Edwards, D. Bour, H. Shah, and I. C. Kizilyalli, "Vertical power diodes in bulk GaN," in *2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2013, pp. 59–62.

[106] T. Oeder and M. Pfost, "Gate-Induced Threshold Voltage Instabilities in p-Gate GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4322–4328, 2021.

[107] W. Shockley and W. T. Read, "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, 1952.

[108] T. Sugahara *et al.*, "Direct Evidence that Dislocations are Non-Radiative Recombination Centers in GaN," *Jpn. J. Appl. Phys.*, vol. 37, no. Part 2, No. 4A, pp. L398–L400, 1998.

[109] T. Naka and W. Saito, "Relation between UIS withstanding capability and gate leakage currents for high voltage GaN-HEMTs," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, 2017, pp. 199–202.

[110] N. Xu *et al.*, "Gate leakage mechanisms in normally off p-GaN/AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 113, no. 15, p. 152104, Oct. 2018.

[111] S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. DasGupta, and N. DasGupta, "Gate Leakage Mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and Modeling," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3157–3165, 2013.

[112] S. Ghosh, A. Dasgupta, A. Dutta, S. Khandelwal, and Y. Chauhan, *Physics based Modeling of Gate Current including Fowler-Nordheim Tunneling in GaN HEMT*. 2016.

[113] H. R. Mojaver and P. Valizadeh, "Reverse Gate-Current of AlGaN/GaN HFETs: Evidence of Leakage at Mesa Sidewalls," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1444–1449, 2016.

[114] E. J. Miller, X. Z. Dang, and E. T. Yu, "Gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors," *J. Appl. Phys.*, vol. 88, no. 10, pp. 5951–5958, Nov. 2000.

[115] A. Hassan, Y. Savaria, and M. Sawan, "GaN Integration Technology, an Ideal Candidate for High-Temperature Applications: A Review," *IEEE Access*, vol. PP, p. 1, Dec. 2018.

[116] J. Kotani, M. Tajima, S. Kasai, and T. Hashizume, "Mechanism of surface conduction in the vicinity of Schottky gates on AlGaN / GaN heterostructures," *Appl. Phys. Lett.*, vol. 91, no. 9, p. 93501, Aug. 2007.

[117] A. Stockman *et al.*, "On the origin of the leakage current in p-gate AlGaN/GaN HEMTs," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, 2018, pp. 4B.5-1-4B.5-4.

Appendix-3: List of Figures

Figure 1.1 World energy consumption: history and projection from 2010-2050 [3]. 1

Figure 1.2 Share primary energy consumption by source in 2020 and the prediction in 2050[3]. 2

Figure 1.3 Power electronics applications[4]........ 3

Figure 1.4 Power device technology positioning in 2021[5]. 4

Figure 2.1 Wurtzite-type Hexagonal GaN crystal structure with Ga- or N-face at the surface of the crystal[7]. 17

Figure 2.2 Spontaneous polarisation (Psp) coefficient in $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ as a function of Al mole fraction(x) [32]. 18

Figure 2.3 Theoretical calculation results of the piezoelectric polarisation charge density as a function mole fraction of Al or In in $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $Al_xIn_{1-x}N$[7]. 19

Figure 2.4 The polarisation field exists in the ionic bonds of the GaN tetrahedron structure with (right) and without (left) the mechanical stress[7]. 20

Figure 2.5 the theoretical and experimental lattice constant of $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ at T=0K and 300K, respectively[9]. 22

Figure 2.6 Spontaneous and piezoelectric polarisation with Ga-face and N-face induced sheet charge density under different conditions [35]. 23

Figure 2.7 (a)The spontaneous, piezoelectric and total polarisation sheet charge density as a function of Al-content in the N-face GaN/ AlxGa1-xN/GaN heterostructures(b)the polarisation induced sheet charge density[31]. 26

Figure 2.8 Theoretical calculation results of the polarisation induced sheet charge density as a function of Al or In molar fraction(x) in $Al_xGa_{1-x}N$/GaN, $In_xGa_{1-x}N$/GaN and $Al_xIn_{1-x}N$/GaN heterostructures[36]. 27

Figure 2.9 conduction band diagram of AlGaN/GaN HFET with different space charge components [38]. 28

Figure 2.10 schematic band diagram of the surface-donor model under different AlGaN thicknesses:(a)less than(b)more than the critical thickness. (C)The theoretical relationship between 2DEG density and AlGaN barrier thickness is based on the surface donor model[38]..29

Figure 2.11 shows the measured and calculated 2DEG sheet density as a function of $Al_{0.34}Ga_{0.64}N$ barrier thickness at room temperature [39]................30

Figure 2.12 The relationship between 2DEG and 2DHG sheet density and carrier mobility as a function of GaN cap layer thickness in GaN/AlGaN/GaN double heterostructures [33]..31

Figure 2.13 schematic band diagram of (a) AlGaN/GaN heterostructures; GaN/AlGaN/GaN double heterostructures with a(b) thin GaN cap layer(C) thick GaN cap layer [39]...32

Figure 2.14 2DEG sheet density as a function of Al composition of AlGaN in AlGaN/GaN heterostructures [40]. 33

Figure 2.15 The schematic cross-section of conventional AlGaN/GaN HEMTs [45]. 35

Figure 2.16 conduction band diagram under different gate voltage(a)V_g is positive (b)$0<Vg<V_{Th}$ (C) $Vg>V_{Th}$ [46]. 37

Figure 2.17 Schematic of a conventional HFET in (a) the ON-state and (b) the off-state[47]. 38

Figure 2.18 Cross-sectional structures of fabricated AlGaN/GaN HEMT with field plate structure (FP-HEMT) and electric field distribution along with the AlGaN/GaN interface layer with field plate (solid line) and without field plate (broken line)[54]. 39

Figure 2.19 Comparison of electric field profile between single and double FP technology during off-state[54]. 40

Figure 2.20 The breakdown voltage of AlGaN/GaN HEMTs with single and double FP technology as a function of field plate length[54]. 41

Figure 2.21 The schematic cross-section of the PN diode with RESURF technology [57] 43

Figure 2.22 Th electric field distribution and potential lines in bulk and at the surface under various t_{epi}:(A) 50um at BV=370-470V;(B)for 15um at BV=1150V [57]. 44

Figure 2.23 Schematic cross-section and electric field profile of (a) Conventional diode (b) SJ diode [64] 46
Figure 2.24 The trade-off relationship between specific on-state resistance and breakdown voltage for conventional Si, SiC, GaN and super junction for Si, SiC and GaN[65]. 48
Figure 2.25 Schematics of (a) layer structure and (b) band diagram[68]. 49
Figure 2.26 The cross-section and electric field distribution under the ideal condition of PSJ HFETs during off-state[69]. 50
Figure 2.27 Typical (a)transfer characteristics and (b) Id-Vd characteristics of PSJ HFETs[69] 51
Figure 2.28 (a)Typical gate leakage(Ig) and drain leakage(Id) characteristics of Lpsj=40um (b) the breakdown characteristics as a function of PSJ Length during the off state of the PSJ HFETs with Wg=90mm. Furthermore, they are all measured at Vgs=-10V[69]. 52
Figure 2.29 The switching waveform and circuit diagram for evaluating current collapse (left); Id-Vds characteristics of conventional HFETs(right) [45]. 54
Figure 2.30 Schematic cross-section of conventional GaN-on-Si power HEMTsand the main factors for the current collapse[76]. 55
Figure 2.31 Gate-instability-induced dynamic R increase in the MIS-HEMTs (a) schematic of energy band diagram with the interface/border trapping

mechanism under positive gate bias(b)positive V_{th} shift(ΔVth)(c)degradation of R_{on} after ΔVth. 56

Figure 3.1 Schematic diagram of PSJ heterostructures (U-GaN/AlGaN/U-GaN). 62

Figure 3.2 Schematic band diagram of PSJ heterostructures (U-GaN/AlGaN/U-GaN) with the free surface above the top U-GaN layer. 63

Figure 3.3 (a) Schematic cross-section of U-GaN/AlGaN/U-GaN and (b) the relationship between top u-GaN thickness and 2DHG sheet density with the free surface and Schottky barrier ($\boldsymbol{\phi B, P}$) of the surface on top U-GaN layer.66

Figure 3.4 Schematic diagram of PSJ heterostructures with P-GaN layer(P-GaN/U-GaN/AlGaN/U-GaN) 68

Figure 3.5 Schematic diagram of PSJ heterostructures (P-GaN/U-GaN/AlGaN/U-GaN) with the free surface above the top U-GaN layer. 69

Figure 3.6 The calculated and simulated results of the relationship between top U-GaN thickness and sheet density of 2DHG are extracted from the numerical model of P-GaN/u-GaN/AlGaN/U-GaN heterostructures. 72

Figure 3.7 Measured sheet density of 2DHG with different top u-GaN thicknesses under different temperatures by Nakajima. [85] 74

Figure 3.8 The band diagram of PSJ heterostructures with AlN nucleation layer 77

Figure 4.1 (a)The schematic cross-section of the PSJ hybrid diode (b) the mask photograph of the test structure of the PSJ hybrid diode. 83

Figure 4.2 Typical PSJ hybrid diode I-V characteristics with different widths (finger length):(a)200 um and (b)800 um. 84

Figure 4.3 The multi-finger layout for PSJ large hybrid diode with five fingers and L_{psj} =10 um, but different finger widths (200um and 500um, respectively). 85

Figure 4.4 the specific R_{on}·A of PSJ hybrid diode as function L_{PSJ} (5um to 25 um) with different widths (finger length):200 um,500 um,800 um and 1000 um. ...86

Figure 4.5 Typical I-V characteristics of PSJ hybrid diode with different finger quantities (5,10, and 20)(a)PSJ hybrid diode with L_{PSJ}=10um(b) with L_{PSJ}=20um and width=200um. 88

Figure 4.6 Typical I-V characteristics of PSJ hybrid diode with different finger quantities (5,10, and 20)(a)PSJ hybrid diode with LPSJ=10um(b) with LPSJ=20um and width=500um. 89

Figure 4.7 The specific R as a function L(10,15,20,25 um) for PSJ large hybrid diode. 90

Figure 4.8 Typical PSJ hybrid diode I-V characteristics at elevated temperature from 25 °C to 125 °C with 25 °C step. 91

Figure 4.9 Specific R_{on}·A as a function of L_{PSJ} with the rise of temperature from 25°C to 125 °C with 25 °C step. 92

Figure 4.10 (a)Typical reverse blocking characteristics (b) breakdown voltage of PSJ diode as a function of L_{PSJ}, measured at 25°C. 93

Figure 4.11 Typical reverse blocking characteristics of PSJ hybrid diodes-on-Si substrate provided by POWDEC.K.K as a function of L_{PSJ}, measured at 25°C. 94

Figure 4.12 The BV of PSJ fabricated hybrid diodes are compared with the hybrid diodes-on-Si from POWDEC.K.K and diodes-on-Sapphire as a function of L_{PSJ}, which are measured at 25°C. 95

Figure 4.13 The schematic cross-section and device dimensions of the fabricated PSJ HFETs...98

Figure 4.14 Typical transfer characteristics of the fabricated PSJ HFETs at 25°C. 99

Figure 4.15 Typical I_d –V_d characteristics of the fabricated PSJ HFETs at 25°C. 99

Figure 4.16 (a) The mask layout of the PSJ HFETs (b) the specific R_{on}·A as a function of L_{PSJ} of PSJ HFETs with different gate widths (50,200,500,800 and 1000 um). 100

Figure 4.17 (a) Typical I-V characteristics of PSJ HFETs with L_{PSJ} =5um as function of elevated temperature(25°C to 125°C) (b) the measured specific R_{on}·A as a function of L_{PSJ} (5um to 25 um)and elevated temperature(25°C to 125°C). 101

Figure 4.18 (a) the off-state breakdown characteristics of PSJ HFETs with different L_{PSJ} ranging from 5 um to 20 um(b)the relationship between BV and L_{PSJ} of PSJ HFETs from Sheffield PSJ HFETs on Si and sapphire substrate and POWDEC PSJ HFETs-on-Si substrate. 103

Figure 4.19 The relationship between the breakdown voltage and Specific Ron·A of the Sheffield PSJ-on-Si substrate, POWDEC PSJ-on-Si and PSJ-on-sapphire power devices from Kawaii et al. [69]. 105

Figure 5.1 The Cross-section schematics of P-GaN ohmic gate PSJ HFETs. .. 110

Figure 5.2 The measurement conditions and setup for (a) pulsed-transfer measurements; and (b) pulsed Ids-Vds characteristics for analysing the Vth shifts in PSJ HFETs. 112

Figure 5.3 Typical Gate Current characteristics (Igs-Vgs) of the PSJ HFETs measured at Vds=1V. 113

Figure 5.4 (a)Typical pulsed transfer characteristics of PSJ HFETs measured at V_{ds}=1V and quiescent V_{dsq}=0V, under different stress gate bias V_{gsq}, ranging from 0V to 3.4V.(b) the trapping mechanisms under positive gate stress 114

Figure 5.5 Vth shift value (ΔVth) with different L_{PSJ} =15um,20um,40um,50um and 70um. 115

Figure 5.6 Typical pulsed transfer characteristics of PSJ HFETs were measured at V_{ds}=1V and quiescent V_{dsq}=0V. The measuring time ranges from 0.5ms to

100ms, and the stressing time is fixed at 500ms under gate stress voltages (a) V_{gsq} =+1V and (b) V_{gsq} =+3V 116

Figure 5.7 Typical pulsed Id-Vds characteristics of PSJ HFETs were measured at Vgs=3V with different stress gate voltages (Vgsq), ranging from 0V to 3V. 118

Figure 5.8. (a) Typical pulsed transfer characteristics of PSJ HFETs were measured at V_{ds}=1V and quiescent V_{dsq}=0V under negative stress gate bias V_{gsq}, ranging from 0V to -7V. (b) the V_{th} shifts as a function of varying gate stress voltages in PSJ HFETs(C)The trapping mechanisms under negative gate stress. 120

Figure 5.9 Typical pulsed transfer characteristics of PSJ HFETs measured at V_{ds}=1V and quiescent V_{dsq}=0V. The measuring time ranges from 0.5ms to 100ms, and the stressing time is fixed at 500ms under gate stress voltages V_{gsq}=-7V. 121

Figure 5.10 Typical pulsed Id-Vds characteristics of PSJ HFETs were measured at Vgs=3V with different stress gate voltages (Vgsq), ranging from 0V to -4V. 122

Figure 5.11 the Vth shifts as a function of different temperatures in PSJ HFETs, the gate stress voltage is +3V, and the steady Vds is 1V (Vdsq is 0V). The Vth is extracted at 10mA/mm. 124

Figure 5.12 (a) The schematics cross-section and （b） the photograph of Schottky-gate PSJ HFETs. 125

Figure 5.13 The pulsed transfer characteristics of PSJ HFETs measured at Vds=1V and quiescent V_{dsq}=0V, under different stress gate bias $V_{gstress}$, ranging from 0V to 4V.(b) the Vth shift as a function of varying gate stress voltage in PSJ HFETs, V_{th} is extracted at 1mA/mm. 126

Figure 5.14 The pulsed transfer characteristics of PSJ HFETs measured at Vds=1V and quiescent Vdq=0V under different negative stress gate bias Vgstress, ranging from 0V to -4V. 127

Figure 6.1 The schematic cross-section of conventional AlGaN/GaN diode. 130

Figure 6.2 The typical forward I-V characteristics of conventional AlGaN/GaN diode with(a)L_{AC}=5 μm and (b) L_{AC}=10 μm 131

Figure 6.3 The simulated forward I-V characteristics of conventional AlGaN/GaN diode 133

Figure 6.4 (a) the schematic cross-section of conventional AlGaN/GaN diodes with a cutline at the 2DEG channel. (b)the electron concentration distribution along the 2DEG channel...134

Figure 6.5 The electric field distribution along the 2DEG channel at different V_{AC} (from 0V to 10V). 135

Figure 6.6 The schematic cross-section of PSJ hybrid diode............................136

Figure 6.7 The typical forward I-V characteristics of three identical PSJ hybrid diode 137

Figure 6.8 The typical forward I-V characteristics of PSJ (a)small (b) large-area hybrid diode as a function of temperature (from 25°C to 175°C)..................... 138

Figure 6.9 The simulated current flow-lines distribution at V_{AC}=10V in PSJ hybrid diode. 139

Figure 6.10 The typical I-V characteristics of the PSJ hybrid diode obtained from the simulation and experiment. 140

Figure 6.11(a) the cutline is located along the 2DEG channel, (b)the electric field distribution, and (C) the electron distribution with the rise of the V_{AC}(from 5V to 20V). 142

Figure 6.12 The on-state characteristics of Si PiN rectifier[104]. 144

Figure 6.13 The schematic cross-section of PSJ PiN diode. The AlGaN thickness is 25nm, and the Al mole fraction is 0.3. A and C represented Anode and Cathode.. 146

Figure 6.14 Typical DC-mode I-V characteristics of the GaN PSJ PiN diode. 146

Figure 6.15 Typical DC-mode I-V characteristics of the GaN PSJ PiN diode with L_{PSJ}=5,10,15, and 20 μm. 147

Figure 6.16 Forward pulsed I-V characteristics under different on-state periods varying from 0.5ms to 2ms with the step of 0.5ms, and the pulse period is fixed at 500ms.(a)V_{AC} from 0v to 20V (b) V_{AC} from 4V to 5V..................................... 148

Figure 6.17 Simulation: forward I-V characteristics with different trap concentration 151

Figure 6.18 (a) The distribution of the diffusion current density of the PiN junction and (b) Zoom-in the AlGaN layer under different biases (from 5V to 25V, the step is 5V) at the trap states concentration equal to 6.7e18. 152

Figure 6.19 (a)The hole and (b) electron velocity distribution in the PiN junction under different biases (from 5V to 25V, the step is 5V) at the trap states concentration equal to 6.7e18 cm^{-3}. 153

Figure 6.20 The operation principles of the trap-assisted mechanism for the PSJ PiN diode current saturation behaviour under the forward bias. 154

Figure 6.21 The distribution of the (a) hole saturation velocity of the PiN junction and (b) electron saturation velocity with different trap concentrations. 155

Figure 7.2 Typical transfer characteristics (Ids-Vgs) of the PSJ HFETs were measured at Vds=1V. 161

Figure 7.1 The schematic cross-section of the PSJ P-GaN ohmic gate HFETs. 161

Figure 7.3 Typical pulsed Id-Vd characteristics of the PSJ HFETs were measured at V_{gs}=-5V to 2V with the step of 1V. The pulse width is 1ms, and the duty cycle is 1% at room temperature. 162

Figure 7.4 (a)Typical gate leakage characteristics (Ig-Vg) of the PSJ HFETs with different lengths of PSJ(LPSJ):5,10,15,20,40,50,70 um at room temperature under dark conditions. (b) gate leakage current of PSJ HFETs with different LPSJ is extracted at Vg=-10V. 163

Figure 7.5 The electron and hole concentration distribution along the PSJ PiN junction under different gate biases (V_g=-3V and -5V). The blue line is for -5V and the red line is for -3V. The solid line represents the electron Concentration, and the dashed line is the hole concentration...165

Figure 7.6 The gate leakage characteristics (Ig-Vg) of the PSJ HFETs with the length of PSJ (LPSJ) =15 um with the temperature rising from 25 ^{o}C to 150°C in steps of 25 ^{o}C. 167

Figure 7.7 lnJg of PSJ HFETs with LPSJ=15 um as a function of the (2/T). 168

Figure 7.8 (a)The lnσ of the PSJ HFETs as the function of $(1/T)^{1/3}$ (b) the mechanism of 2D-VRH hopping effects in PSJ HFETs.....................................170

Figure A.0.1 Mask alignment sequence and alignment tolerance rules. 178

Figure A.0.2 The unit cell dimensions of PSJ HFET are based on the mask alignment tolerance rules..179

Figure A.0.3 The photograph of the mask design..180

Figure A.0.4 The final photograph of the mask layout. 180

Figure 0.5 The schematic cross-section of devices after device Isolation etching. 182

Figure 0.6 The schematic cross-section of devices after mesa etching. 183

Figure 0.7 The schematic cross-section of devices (a)after depositing the 150 nm-SiN dielectric layers (b) after etching the 150 nm-SiN dielectric layers on the active area. 183

Figure 0.8 The schematic cross-section of devices of P-ohmic deposition. 184

Figure 0.9 The schematic cross-section of the device after N-contact metallisation.. 184

Figure 0.10 The schematic cross-section of devices(a) PECVD 150nm-SiN (b)SiN via etching through RIE. 185

Figure 0.11 The schematic cross-section of devices after M2........................... 186

Figure 0.12 (a) the 3D-schematic cross-section of the large-area devices (b) the schematic cross-section of the active area of the devices after passivation and RIE etching 187

Figure 0.12 The photograph of fabricated PSJ-on-Si sample(18mm×18mm) at Sheffield compared with a one-pound coin. 187

Appendix-4: List of Tables

Table 2-1 intrinsic Si and major wide bandgap semiconductor properties[7] 10

Table 2-2 Main figures of merit for WBG semiconductors compared with Si[9], [10] 10

Table 2-3 properties of different Substrates for GaN power devices[7] 14

Table 4-1 The design information of PSJ-on-Si power devices 82

Table A-0-1 Mask layer information. 178

Appendix-5: List of Publications

1. Yangming Du , Hongyang Yan , Peng Luo , Xiao Tan , Shankar N Ekkanath Madathil , Hiroji Kawai , Shuichi Yagi , Hironobu Narui "**Investigation on Shift in Threshold Voltages of 1.2kV GaN Polarization Superjunction (PSJ) HFETs**" *IEEE Transactions on Electron Devices*, DOI:10.1109/TED.2022.3225695
2. H. Yan, Y. Du, P. Luo, X. Tan, and E. M. S. Narayanan, "**Analytical Modeling of Sheet Carrier Density and on-Resistance in Polarization Super-Junction HFETs,**" *IEEE Transactions on Electron Devices,* DOI: 10.1109/TED.2021.3115091.