

Fabrication of High Speed GaN-based Transistors and DC-to-DC Converters

By Joseph Pinchbeck

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Abstract

GaN power devices are an area of research with growing interest due to the material's superior intrinsic properties making it a good choice for high frequency high power applications. This study looks at using a dual metal gate (DMG) structure to improve the transconductance and reduce short channel effects. The study presents research into how GaN HEMTs can improve monolithically integrated buck converters and different topologies have been fabricated and compared.

Several dual gate devices with different gate lengths were fabricated and tested as well as comparisons with simulations made. Transconductance improvements stemming from the dual gate structure were demonstrated down to gate lengths of 200nm. Improvements from 216mS/mm to 229mS/mm for a total gate length of 200nm are demonstrated. In addition, short channel effect reductions, specifically drain induced barrier lowering (DIBL) has been shown to be greatly reduced with the dual gate metal implementation. Reductions up to 49% are shown down to total gate lengths of 200nm.

Monolithically integrated buck converters have been demonstrated with both standard and multilevel topologies compared. High efficiencies of 80% have been demonstrated with the standard topology shown for 10V, 1MHz operations. Experimental testing has also been performed at higher voltage, 25V 1MHz and higher frequency 10V 50MHz. Standard, three level and five level converters have been tested experimentally and the results verified with simulations. Comparisons show that the five-level topology may be the most suitable for the highest voltage tested in this study, 25V, and show the highest efficiency at 77.3%.

A study into the effect of the field plate have on the electrical performance of the power transistors was performed. The source field plate configuration in the GaN power transistors has been demonstrated to be best option for dynamic Ron suppression and intrinsic gate capacitance. A increase in device on state resistance by 210% is shown to be reduced to a 20% increase by the addition of the field plate.

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List of Publications

Journal papers

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Chapter 1 - Introduction

1.1 Overview of GaN

Gallium Nitride (GaN) is a III-V semiconductor looked at recently for its large bandgap and ability to sustain a high breakdown field¹⁻³. These factors have led to the development of semiconductor devices created from GaN that can take advantage of these intrinsic properties. The properties of GaN mean that the creation of high electron mobility transistors (HEMT) are possible and lead to the potential to be able to create transistors that can sustain larger breakdown voltages and provide low channel resistance⁴.

A comparison between GaN's properties and a number of other materials intrinsic properties can be seen in table 1.1.

	Bandgap (eV)	Breakdown Field (MV/cm)	Electron Mobility (cm ² /Vs)
Silicon	1.1	0.3	1500
GaAs	1.4	0.4	8500
4H-SiC	3.3	3	1000
GaN	3.4	3.3	2000
Diamond	5.5	10	1800

Table 1.1 - A comparison between the intrinsic properties of the most commonly used semiconductor materials^{5,6}.

The advantages are clear when directly comparing to similar materials, with high electron mobility and a high breakdown field present in GaN. As such, much research is being done into implementing GaN devices in high frequency and high-power applications. RF communications are the most common area of use and are used in broadband and 5G communication technologies.

By creating an alloy of Aluminium and GaN the intrinsic band gap can be increased even further which can be used in conjunction with GaN to create a 2 dimensional electron gas (2DEG). By growing the AlGaN on the surface of GaN the interaction between the two leads to spontaneous generation of a 2DEG which in turn allows the creation of high electron mobility transistors (HEMTs)⁷.

1.2 Two Dimensional Electron Gas (2DEG) Physics

One of the key advantages that comes from GaN and more specifically AlGaN/GaN HEMTs comes from the presence of the naturally occurring 2DEG leading to a very high electron mobility within the device. Typically for an AlGaN/GaN HEMT the 2DEG concentration is higher than other 2DEG forming materials such as AlGaAs/GaAs. Sheet carrier concentrations of 10^{13}cm^{-2} are achieved in GaN compared to 10^{12} for GaAs⁸. Unlike AlGaAs/GaAs HEMT devices, doping is not required in GaN and forms intrinsically between undoped AlGaN and GaN. The formation of this 2DEG originates from the net polarisation charge between AlGaN and GaN, this is contributed to from the fact that AlN has a band gap of 6.2eV and GaN 3.4eV⁹. The percentage of AlN within the AlGaN determines its band gap with a higher percentage increasing the band gap. Typical values are between a 20-30% AlN composition with the gallium in the crystal structure being replaced by aluminium.

This difference in work function leads to a bending of the conduction and valence bands at the interface between the two materials such that the fermi level lies above the conduction band of the GaN. This leads to the creation of a quantum well which all the free electrons lie within⁹. The size of this quantum well determines the number of carriers trapped in this energy state. While in this energy state the carriers are subject to fewer collisions with defects in the structure which leads to higher electron mobility. This can be seen below in figure 1.1 and shows how the amount of band bending, i.e. the percentage of AlN within the AlGaN, can lead to a larger quantum well and therefore more carriers with a higher electron mobility.

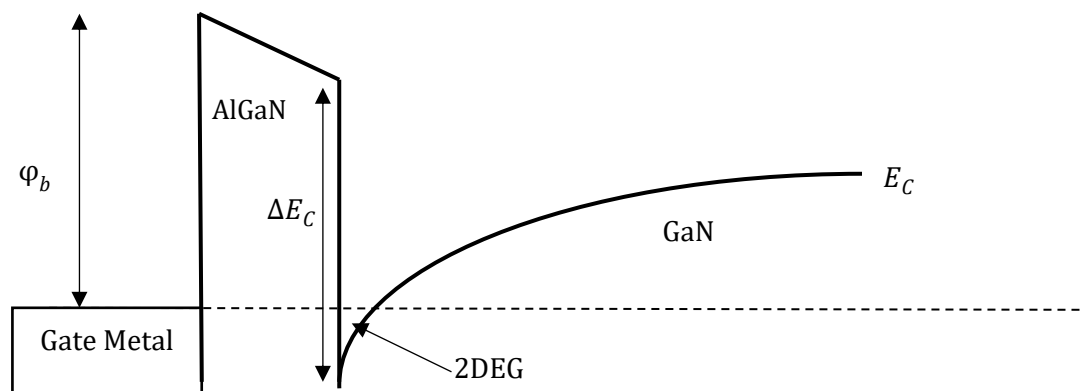


Figure 1.1 – An energy diagram showing conduction band bending at the AlGaN/GaN interface

The density of this 2DEG channel can be shown from the following equation 1.1¹⁰

$$n_s = \frac{\sigma_{pol}}{q} - \frac{\epsilon}{q^2 d} (q\phi_b + E_f - \Delta E_c) \quad 1.1$$

ϕ_b being the surface barrier height, σ_{pol} the net charge density at the surface given between the difference between the AlGaIn and GaN. ϵ being the dielectric constant of AlGaIn, E_f is the fermi level at the GaN conduction band edge standard value and ΔE_c the conduction band difference between AlGaIn and GaN.

There are two main types of polarisations that contribute to the 2DEG density. Piezoelectric polarisation and spontaneous polarization¹¹⁻¹³. The piezoelectric polarisation is primarily due to the lattice constant difference between the AlGaIn and GaN. The strain on the AlGaIn layer is a tensile force on the crystal structure which leads to the 2DEG formation. Increasing this strain present at this intersection increases the 2DEG density but care must be taken to prevent cracks forming at the interface if the difference is too large.

Spontaneous polarisation occurs naturally in Ga-face GaN due to the wurtzite crystal structure which has inherent asymmetry within the crystal lattice. This asymmetry leads to a shift in the free electron cloud within the GaN which moves the total charge to one end of the crystal, in this case towards the 2DEG channel leading to an increase in polarization. Typical values for 2DEG density are between 10^{12} - 10^{13} cm⁻² which is a factor in the low conduction losses seen within GaN HEMT devices¹⁴.

1.3 Basic Device Structure

The two important considerations to make when creating an efficient AlGaIn/GaN HEMT are the wafer epitaxy and the device structure.

A typical wafer structure can be seen below in figure 2 and consists of an independently grown substrate such as silicon (Si), silicon carbide (SiC) or sapphire (Al₂O₂), as GaN cannot be grown natively it requires a base substrate to be grown upon. Typically, silicon carbide substrates have much better thermal characteristics than silicon substrates and as such will perform better at high frequency operation¹⁵ silicon substrates are typically cheaper. For the devices fabricated in this study all the GaN wafers were grown on a Silicon substrate. Following this is a buffer layer consisting of a number of layers closely lattice matched to the substrate to prevent the strain becoming too large. This layer consists of an AlN layer is grown directly on the substrate then a graded AlGaIn that gradually relieves the strain and prevents cracking from occurring^{16,17}.

Following the graded AlGa_N, a buffer layer is grown that either is iron doped or carbon doped. Carbon doped tends to produce more resistive buffer regions but the current collapse effects in the buffer tend to be worse than with iron doped regions^{18,19}. The iron doped buffer fermi level sits closer to the conduction band, effectively lowering the resistance but in turn allowing trapped carriers to deplete more easily lowering the potential for trapping. The carbon doped fermi level lies closer to the valence band meaning a higher resistance and also a worse trapping effect within the buffer. As such all the wafers looked at in this report have buffer regions which are carbon doped. Following this a thin undoped Ga_N region provides the region for the 2DEG channel to be formed.

Above this is usually a very thin AlN layer to help reduce the alloy scattering that is present between AlGa_N and Ga_N. The uniformity of the aluminium distribution within the AlGa_N is non uniform which can cause alloy scattering. By introducing a constant distribution of aluminium with the AlN layer it helps to reduce this. The AlN layer is extremely thin, <3nm, as it has a large lattice mismatch with Ga_N so making this layer too thick will introduce cracking in the wafer structure.

Above this is the AlGa_N layer, typically 20-30% AlN doped with a typical thickness between 9-25nm. A Ga_N cap around 3nm is placed as the top layer and helps increase the 2DEG present in the channel layer.

The device is then fabricated on top of this wafer, utilising the layer structure to create the working transistor. The basic structure can be seen in figure 1.2. Two ohmic contacts are needed for the source and drain contacts. These are created such that the specific metal composition allows diffusion into the wafer down into the 2DEG channel region to create a low contact resistance. The barrier between this contact and the 2DEG is a key resistance that must be minimised to help optimise the performance of these devices. As well as this there is the Schottky gate contact used to control and deplete the 2DEG in the device to switch the device between on state and off state. By applying a bias to this gate contact, the 2DEG present underneath can be depleted to turn the device off or if the bias is removed the device is normally on. This means unlike conventional silicon transistors Ga_N HEMT devices are normally on devices with a gate bias of 0V. This presents a new set of challenges particularly with power circuits that may have safety concerns involved with normally on transistors. In the event of the failure of the gate driver circuitries which leads to the loss of gate voltage, the use of the normally on transistors means that the power electronic system remains on and may lead to

unexpected consequences. On the other hand, the normally off transistors will ensure the power electronic system remains off in the event of the gate driver failure.

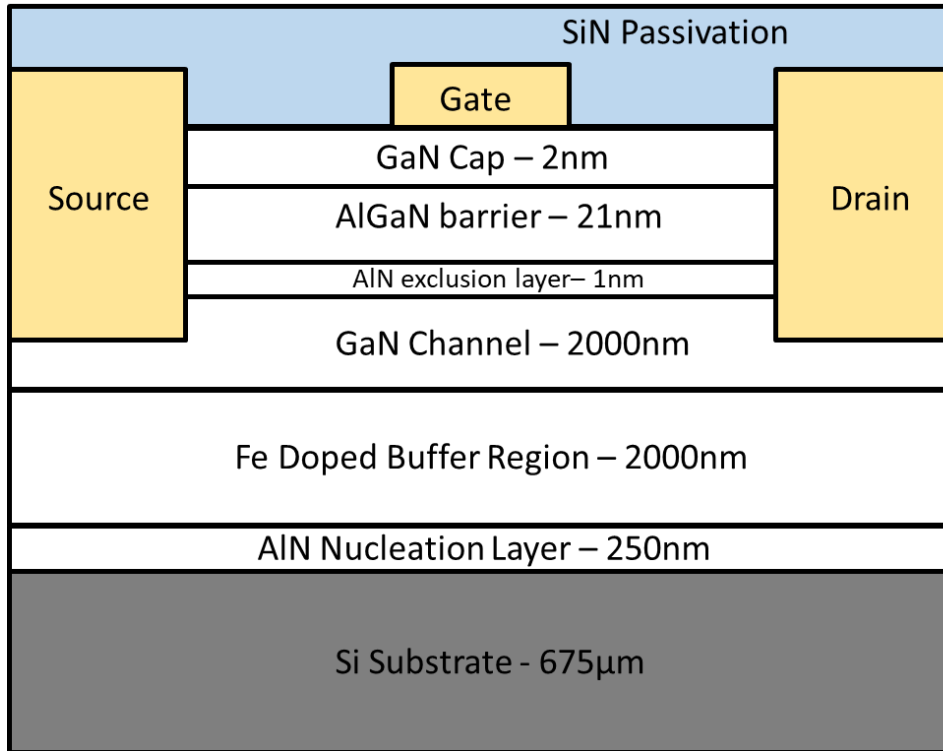


Figure 1.2 – A cross section of the typical device layout and wafer structure seen in an AlGaN/GaN HEMT fabricated on the NTT 1197 Wafer.

Epitaxial Layer	NTT Wafer - 1196 + 1197	Nexperia Wafer – NM170557-1	Nexperia Wafer – NM170558-1
GaN Cap	2nm	2nm	2nm
AlGaN barrier	21nm	25nm	9nm
AlN exclusion	1nm	1nm	1nm
GaN Channel	200nm	250nm	250nm
Buffer	2000nm	1750nm	1750nm
AlN Nucleation	250nm	250nm	250nm
Si Substrate	675µm	675µm	675µm

Table 1.2 – The wafer epitaxy and layer thicknesses of the wafers used for the fabrications outlined in this work.

The wafers used throughout this work are listed in table 1.2. The NTT wafers, 1196 and 1197, were used for all the buck converter fabrications outlined in chapters 4 and 5 and should both have the same wafer epitaxy. The dual gate fabrications outlined in chapter 3 were performed on the Nexperia wafer NM170557-1. Some initial further work outline in chapter 6 was performed using the Nexperia wafer NM170558-1

1.3.1 An overview of Device usage in high frequency, high power applications

As the intrinsic properties of GaN make it a suitable choice for high frequency high power applications further improvements made utilising novel architectures and applications can lead to even greater device performance.

An overview of how implementing a Dual Metal Gate (DMG) device structure can lead to performance improvements. As well as a detailed investigation into GaN implementation within a 5G envelope tracking application and the improvements this can bring will be presented in this research.

1.3.2 Dual Gate Devices

As the main usage of GaN devices is in high frequency high power applications, the use of device architectures that facilitate this is key. A primary device characteristic that controls the ability to perform at high frequency is the gate length and more specifically decreasing the gate length allows faster operation. However, decreasing the gate length of the device can bring about negative short channel effects such as drain induced barrier lowering (DIBL)²⁰. DIBL is an effect where with increasing drain source bias the pinch off region under the gate is shifted towards the drain end. This leads to an increasing in both leakage current and a change in the device threshold voltage. An example of how the surface potential can be altered by the drain bias can be seen in Figure 1.3.

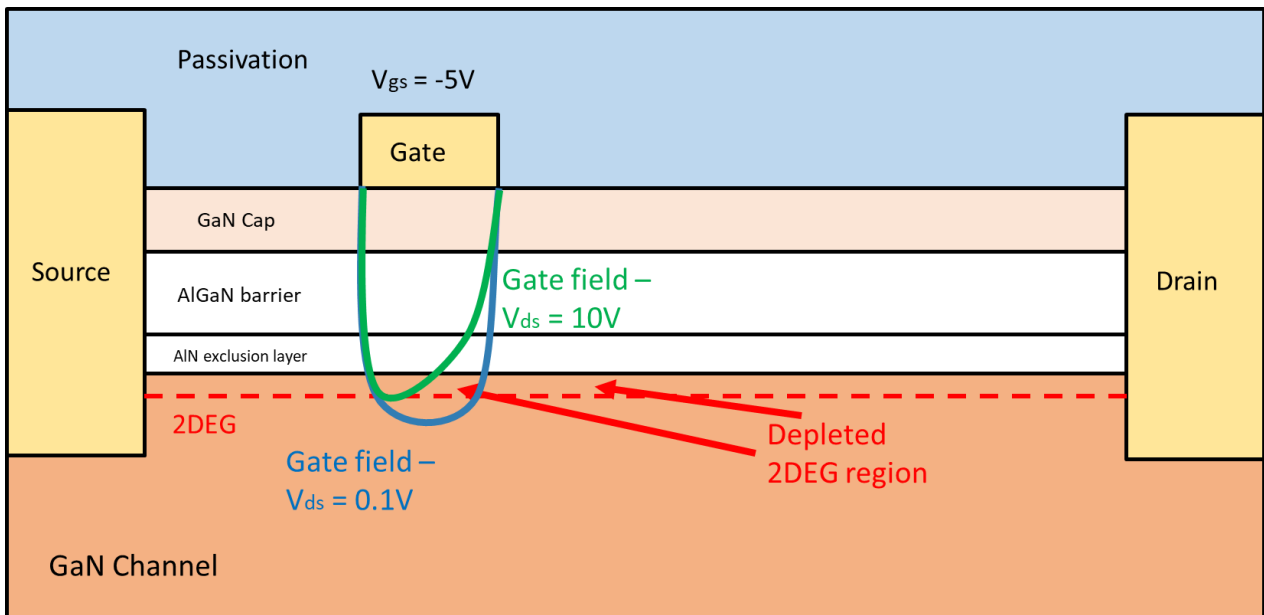


Figure 1.3 – An illustration of DIBL or how the drain bias can affect the gate electric field.

This shows that the surface potential becomes distorted towards the drain end of the gate region and as such can lead to difficulty pinching off the 2DEG channel. This in turn leads to the shift in threshold voltage and increase in leakage currents seen in devices experiencing drain induced barrier lowering.

One way of suppressing this effect and also providing the advantage of increasing device transconductance is by implementing a dual metal gate (DMG) structure. This involves using two metals with differing work functions, typically one high work function metal and one low work function metal.

The two metals are created such that the overlap between them creates one continuous region that acts as a single gate. The work function of the metal defines the device threshold voltage and the higher the work function the less negative the V_{th} . The lower work function is placed on the drain side of the channel and works to effectively spread out the peak field under the device and shield the lower work function metal from the typically high drain bias. This shielding effect prevents the higher work function metal from being affected by the high drain bias.

Previous work has been done on dual metal gate devices originally by Long et al²¹ demonstrating the performance improvements possible using GaAs DMGFET devices. This was the first work to investigate the functionality and improvements that could be introduced into devices by implementing a DMG structure. Investigations into short channel effects as

well as the improvements in transconductance were investigated in this study. Prabhat et al²² has created and analysed a model for the potential and drain current in DMG devices.

This has been translated over to GaN HEMT devices primarily as simulation work, which again show an improvement over conventional SMG devices.

Lee et al²³ have demonstrated the first simulations of the DMGFET structure applied to GaN HEMTs. This study examines both the transconductance improvements and the DIBL improvements the structure can bring. The study also examines the device physics that occur due to the structure that give rise to these improvements using Sentaurus TCAD simulations.

Kumar et al²⁴ have demonstrated simulations on the DMG effects that can be observed in an AlGaIn/GaN HEMT device. They have also quantified the device for use in RF applications with improvements in transconductance and higher cut-off frequency. Although investigations into the short channel effect improvements that can come from this device layout have not been performed.

Initial work fabricating DMG devices has been done by Jung et al²⁵ with gate lengths of 2 μ m. Investigations and improvements in the device transconductance have been demonstrated in fabricated devices, showing a 9% improvement in transconductance. They also investigate the potential for the DMG device to provide an improvement in device current collapse, or dynamic Ron. This investigation does not consider improvements in short channel defects that the DMG device can provide. This is likely due to the larger gate length investigate in this study as the short channel effects tend to present and become an issue in device performance typically with a sub μ m gate length.

As such there are still areas of DMG devices to investigate with regards to AlGaIn/GaN HEMTs particularly in the gate length range below 1 μ m. Investigating whether transconductance improvements continue to smaller gate lengths as well as the short channel effects that can be improved are areas of research this work will cover, with both simulations and experimental data.

1.3.3 Trapping and Field Plate Design

AlGaIn/GaN HEMTs are vulnerable to the negative effects brought about due to an effect known as dynamic Ron, this is an effect that leads to the increasing Ron of the device due to high drain stress voltages^{26,27}. This is due to trapping effect caused by defects in the surface of the device and/or in the GaN buffer of the wafer.

These defects act as traps for the carriers present in the 2DEG and effectively deplete the 2DEG increasing the channel resistance of the device and hence the Ron. There are two main mechanisms that traps can become occupied via, tunnelling, hopping and the Poole Frenkel effect.

Tunnelling occurs due to the electric field induced in the device seen when a high drain source bias is applied at off-state. This field acts to provide the electrons with a reduced barrier that it becomes possible for them to tunnel through. In the GaN devices, the tunnelling is typically trap-assisted²⁸. Once the electrons are trapped in these states, it takes a finite amount of time for them to de-trap. Hopping is a trapping mechanism which involves electrons to hop from a trap site to another. This mechanism relies on the thermal energy of the electrons as well as the energy barrier of the traps.

The final mechanism that can give rise to the occupation of traps is the Poole-Frenkel effect. Poole-Frenkel mechanism are dependent on temperature as well as the applied electric field. The presence of the field reduces the trap energy barrier, which allows the electrons to hop from one trap site to another. A visualisation of all three of these effects can be seen in Figure 1.4.

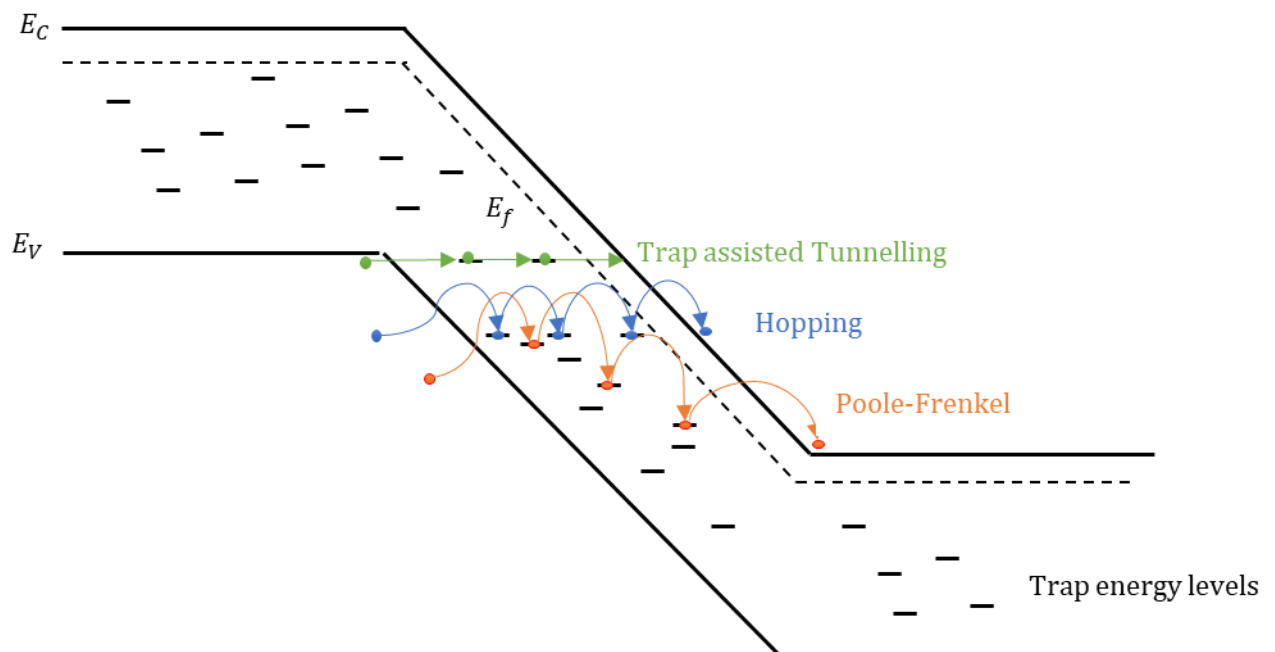


Figure 1.4 - A figure showing a visualisation of the three types of trapping that can occur in defects present in GaN crystals and how the carriers travel using each method.

The trapping in the buffer region can be mitigated by the GaN wafer epitaxial optimisation and carefully controlling the dopants present in this region is key to reducing the trapping effect. The study of the buffer trapping effect is beyond the scope of this study. On the other hand, the GaN surface trapping can be mitigated by device design. Several factors can be used to help reduce traps such as surface passivation using silicon nitride and by implementing field plates. Silicon nitride is effective in passivating the surface traps in GaN and preventing the electrons from accessing those traps²⁹.

In addition to the surface passivation, field plates are implemented to reduce the peak electric field at the edge of the gate. Field plates are an extension of a metal plate over the channel region between the gate and drain as shown. The field plate is raised above the surface of the sample usually by sitting on top of the SiN passivation layer. The field plate splits the gate-edge electric field into two separate peaks in order to achieve an electric field moderation effect³⁰. There are two main types of field plate, a source field plate and a gate field plate. An illustration of a device with both a source and a gate field plate can be seen below in figure 1.5.

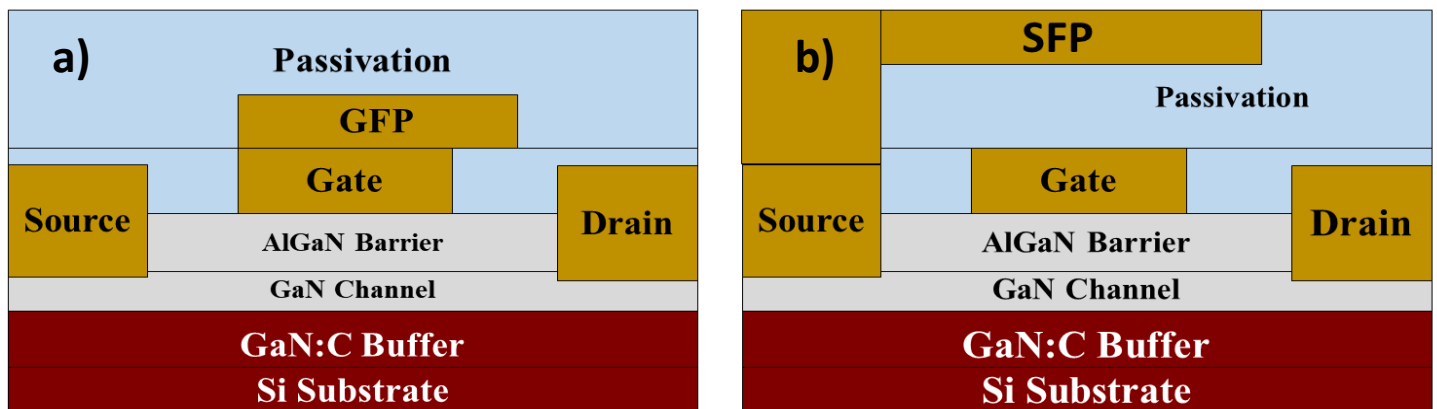


Figure 1.5 – A simple device structure used to illustrate the two types of field plate and their connections to contacts. a) A gate field plate (GFP) and b) A source field plate (SFP).

Although the field plates have been reported to suppress the field-induced trapping³¹, it also affects the capacitance of the devices, and this study aims to investigate how well they suppress dynamic Ron and the effect they have on intrinsic capacitances.

1.4 Envelope Tracking

Envelope tracking is a power delivery system that can provide the required instantaneous power needed to a system at a given moment to help reduce losses^{32,33}. Rather than providing a fixed input power to

the system an envelope tracking system matches the input power to the output power. This can be seen in Figure 1.6. An important requirement for these systems is that they have the required speed to match the transitioning output power. Typically used in systems that will spend a majority of time in lower power operations with only the need for a spike in power requirements in irregular intervals. This spike of output power in a standard power delivery system will determine the power needed to be delivered across the whole operation in mode in case the system has a spike in power requirements.

Primarily used in RF systems that have largely variable power demands the system aims to only provide the instantaneous power needed at a given point in time. Envelope tracking systems see the most use in mobile signal transmission systems, 4G and 5G systems that use LTE signals³⁴. They typically operate at power and frequency levels that make envelope tracking an ideal choice. Particularly the LTE signals that typically operate at low power outputs for the majority of the time.

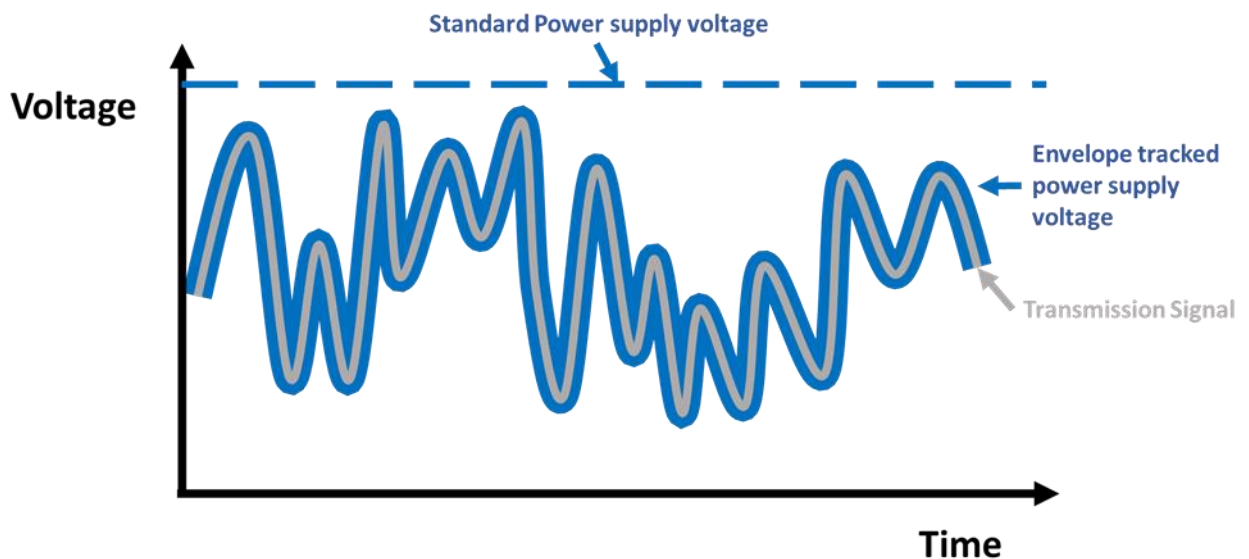


Figure 1.6 - An example of the power needed and transmission signals in a fixed power supply vs an envelope tracking system. Highlighting how envelope tracking provides power closer to the demand at any given point.

The envelope tracking system itself is made up of two main parts and can be seen in figure 1.7.

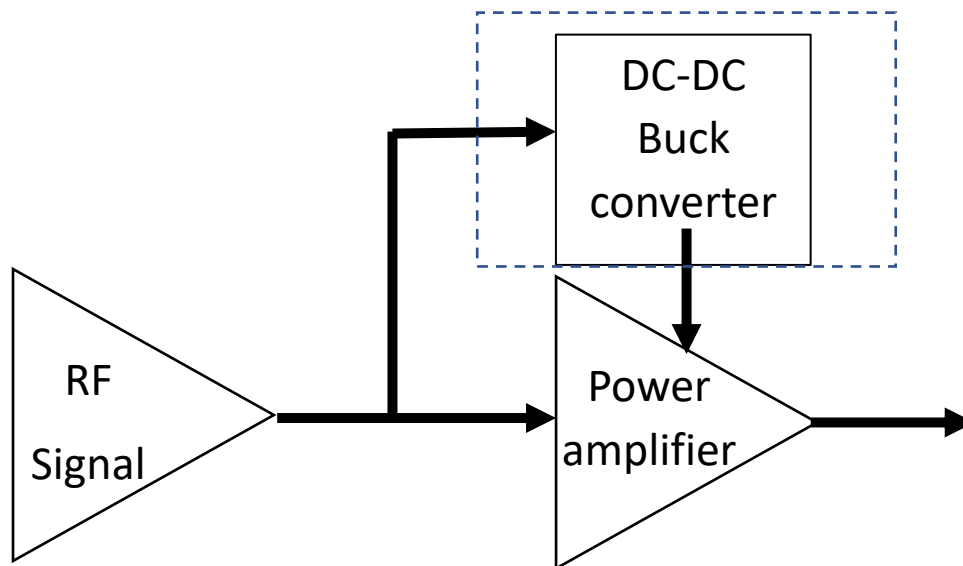


Figure 1.7 - A system diagram showing the stages that are required to produce an envelope tracking system used in RF applications.

The RF signal being transmitted is fed into both an RF power amplifier (RFPA) and a DC-DC voltage converter that in turn provides the power needed for the RFPA. The DC-DC converter in this system is usually a step-down buck converter. The buck converter is the main focus of this research.

To be able to accurately track the waveform a high switching speed is required, typically around 10x the frequency of the waveform. We will be investigating a range of frequencies up to 50MHz and the effect this has on the efficiency.

1.5 Buck Converters

DC-DC converters are a key element in envelope tracking systems and having them maintain a high efficiency is extremely important to prevent power wastage. There are a number of types of DC-DC converters but the main focus of this research was investigating and improving a buck converter as they can take advantage of the power switching capabilities of GaN devices.

The buck converter is a step down converter that reduces the voltage and increases the current. It utilises a varying duty cycle along with an inductor and capacitor filter to modulate the voltage seen at the output. The basic layout of the circuit can be seen in figure 1.8.

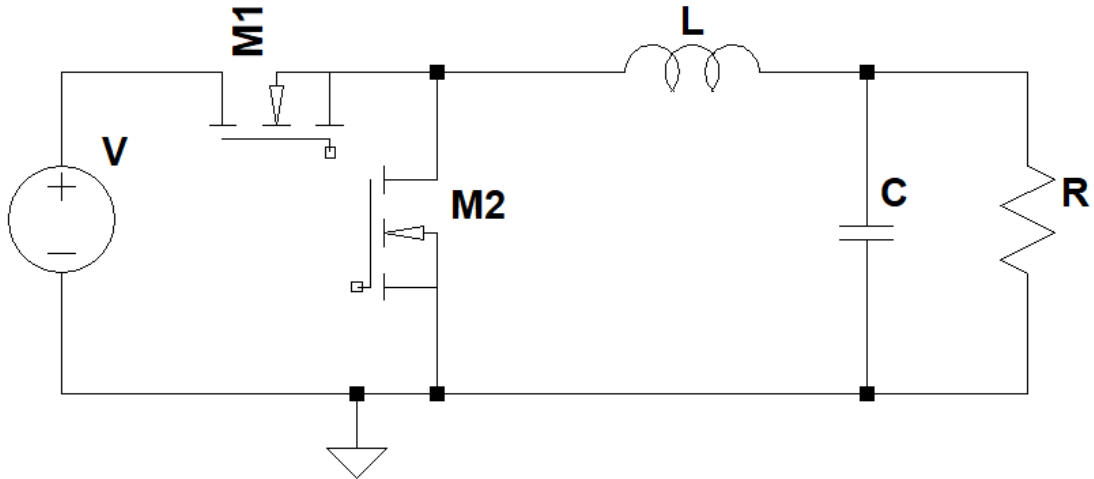


Figure 1.8 – The basic layout of the power stage of a synchronous buck converter without any gate control system in place.

The control of this duty cycle is done via either a power transistor and a diode or a pair of power transistors in the case of a synchronous buck converter. The voltage control in the circuit can be described by the equation. The duty cycle is the proportion of the input to output ratio shown in equation 1.2.

$$Duty\ Cycle = \frac{V_{out}}{V_{in}}. \quad 1.2$$

This study focuses mainly on synchronous rectification as the second transistor can provide a more efficient system than the conventional buck converter as tighter switching control can be achieved. The main losses in the circuit are made up from transistor, inductor and capacitor losses with the majority coming from the transistor. As such minimising both the conduction and switching losses due to the transistor is key to achieving high efficiency. The switching losses can be described by equation 1.3

$$P_{switch} = \frac{1}{2} V_{in} I_{out} (T_{rise} + T_{fall}) f_{sw} \quad 1.3$$

Where V_{in} is the input voltage, I_{out} is the output current, T_{rise} and T_{fall} and the rise and fall times during the transistor switching and f_{sw} is the switching frequency. As can be seen a higher switching frequency is directly correlated with higher losses but due to the needs of the envelope tracking system a minimum threshold for this must be hit.

The conduction losses in the devices are given by equation 1.4

$$P_{conduction} = I_{out}^2 R_{on} \frac{V_{out}}{V_{in}} \quad 1.4$$

Where R_{on} is the on-state resistance in the device, V_{out} is the output voltage, I_{out} is the output current and V_{in} is the input voltage.

Minimising both of these transistor losses is key to providing a solution with very high efficiency.

The ripple current is an important factor to consider and is controlled by the size of both the inductor and capacitor, typical values are chosen dependant on output requirements, usually <1% of the total current. The ripple current size must be closely controlled to ensure the system tracks the power closely and the over and undershoot values do not cause any damage to other parts of the envelope tracking system. The equation that describes this is in equation 1.5.

$$\Delta I_L = \frac{(V_{in} - V_{out})D}{f_s * L} \quad 1.5$$

The target for this system is 0.5% of the total output current, based on the requirements for the envelope tracking system.

1.5.1 Previous Work in Literature

Buck converters have been previously demonstrated in literature for a wide range of applications. Silicon buck converters, GaAs buck converters and GaN buck converters have all been previously shown although targeting different performance characteristics. A brief look into both silicon and GaAs systems shows where the limitations lie and how GaN systems can be used to overcome this.

High frequency, high efficiency buck converters have been previously demonstrated using silicon CMOS systems. While these systems can target frequencies in the MHz range, similar to that of the GaN systems, the voltages and overall power conversions are typically much lower. Wang et al³⁵ have demonstrated a silicon FET design that will allow efficiencies up to 93%. The operation of this circuit is however 3.6V which when compared to the operation targets of GaN devices highlights the limitations of other materials.

Similarly, GaAs systems can be efficient at similar frequencies but again with much lower voltage and power requirements. Buring et al³⁶ have demonstrated operational speeds of 1 GHz with efficiencies close to 60% although the output power in this circuit is a maximum of 0.86W.

They have demonstrated a fully integrated buck converter system including a gate driver as well as wire bonding used to provide an on chip inductor. This is a more integrated level than will be demonstrated in this work which will not include an integrated inductor. They also mention testing at lower frequencies down to 100MHz but say the peak performance of their system lies at 1GHz. This means there is a gap in other semiconductor fabrications that GaN devices can fill with their ability to target high powers as well as relatively high frequencies.

A number of buck converter systems have been developed targeting similar requirements to this research. Shinjo et al³⁷ have demonstrated an integrated buck converter with gate driver at various frequencies from 100MHz to 300MHz achieving an overall efficiency of 64%. A final stage efficiency not including gate drivers was measured at 90%. They included an inbuilt gate driver in their circuit and only considered a standard synchronous buck converter topology. They examined the converter under a standard power sweep across a range of duty cycles as well as considered the operation when fed with an example LTE signal that might be used in high frequency RF communications. This is an interesting paper to compare results to as their system is very similar to the ones that are produced in this work.

Sakata et al³⁸ have also demonstrated an integrated buck converter operating at 80MHz for envelope tracking but with only some of the circuit being fully integrated. An overall efficiency of 78% was achieved for the buck converter operated at 20MHz with a 50Ω load. In this work they developed an entire system that would be used for an envelope tracking system integrating also the radio frequency power amplifier (RFPA) to create a mostly on chip envelope tracking solution. They also investigated results using an example LTE signal but only produced lower total system efficiencies of around 35%.

Zhang et al³⁹ have also demonstrated a 100MHz GaN buck converter with integrated gate driver achieving 90% efficiency for the power stage of the system. This setup involved using an external inductor and capacitor connected on a CB to the integrated IC. They operated the circuit at 20V and tested 100MHz, 40MHz and 10MHz. They observed peak efficiencies of 91% for 100MHz, 94.5% at 40MHz and 96% at 10MHz. The output power range is from 0W up to 8W and typically observed peak efficiencies at output powers above 50% duty cycle. They also followed this with some testing of the system as part of an envelope tracking system using an LTE signal and predictions of power stage efficiencies of 83%.

These previous results set high efficiency targets for the research and achieving a fully integrated system with these targets will require new ideas and schematics.

1.5.1 Multi-Level Converters

As well as the standard single level buck converter there are a number of other more complex buck converter circuits that can provide certain advantages. The two main different schematics of buck converters are the three and five level buck converters.

Multi level buck converters provide an increased efficiency across all duty cycles and output powers. This is done by utilising a setup in which more than one high side transistor is used to provide a smaller switching voltage at the switching node. A schematic for a multi level converter can be seen in figure 1.9.

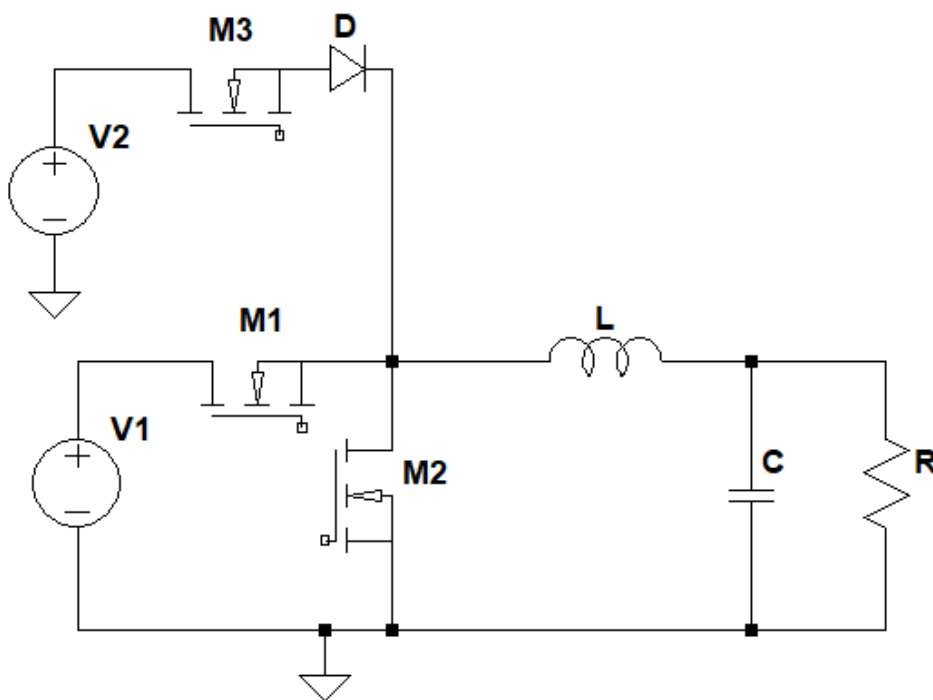


Figure 1.9 - The basic layout of the power stage of a three level buck converter without any gate control system in place.

This smaller switching voltage means the total losses in each transistor will be greatly reduced particularly for smaller output voltages meaning lower switching and conduction losses and in turn higher efficiency.

Previous work on multilevel converters has been performed. Villarruel et al⁴⁰ have produced simulations and predictions of the multi-level converter and how adding additional levels can improve efficiency. These models were done using a 75MHz switching frequency and an output voltage of 30V and output power of 15W. They model the losses from a standard

converter up to a nine level converter and show how the improvement in efficiency becomes smaller with the addition of each extra level. They then created two prototypes with a standard and a five level converter using commercial GaN devices. They show that the five level converter demonstrated efficiencies up to 85% compared to 77% for the standard converter.

Wang et al⁴¹ have also demonstrated a multi-level converter using GaN commercial devices. They target operating parameters of 15V output at 1MHz with a peak output power of 500W. This system provides very high efficiencies up to 97% when operating close to 300W. They also demonstrate the system working with an envelope tracking signal operating at 400kHz bandwidth.

Sepahvand et al⁴² have demonstrated a multi-level converter targeting 8MHz operation at 3.5W. The system includes integrated gate drivers for each stage of the converter as well as integrated power transistors. They demonstrate the converter providing four different output voltage levels and demonstrate a power stage efficiency of 97.3% with a total efficiency of 87.5% when tracking a 10MHz LTE envelope tracking signal.

These previous works have shown the advantages that using a multilevel schematic can bring as well as the high efficiency targets that monolithically integrated systems can provide. This work aims to provide direct comparison between the converters when monolithically integrated, between the multi-level and standard converters.

1.6 Overview of thesis

The main objective of this thesis is to show the advantages that can be achieved by using GaN HEMTs within traditional power circuit architecture. Demonstrations of various buck converter topologies for use within an envelope tracking system are presented and the efficiencies are presented and compared. As well as this investigation into the dual metal gate configuration for GaN HEMTs will be comprehensively investigated. The advantages this layout can bring as well as it's integration into the buck converter system are presented and comparisons made to traditional device layouts. The field plate configurations used within power systems are also investigated to ensure the highest efficiencies are achieved when implementing this technology into the buck converter.

Chapter 2 in the thesis present both the fabrication and characterisation steps needed to create and test integrated GaN devices. Single device testing as well as fully integrated system testing is outlined.

Chapter 3 will outline the dual metal gate device structure, both simulation results as well as experimental results will be presented. Devices with varied gate lengths between 1 μ m to 200nm are compared, as well as devices fabricated on thinner AlGa_N barrier thicknesses. Comparisons are also made to standard single gate devices and the improvements in both DIBL and transconductance are presented.

Chapter 4 will outline the synchronous buck converter. The key fabrication steps and challenges that needed to be overcome followed by simulation results. The experimental results will be gathered from single converters and compared for at various power levels and frequencies. As well as this field plate analysis will be performed to compare the trade offs made with each configuration of field plate.

Chapter 5 will outline the results gathered from the three and five level converters and compare the experimental results with the single level buck converters gathered in chapter 4.

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Chapter 2 - Device Fabrication, characterisation, and simulations

2.1 Introduction

Device fabrication involves construction techniques that allow the development of monolithically integrated circuits built directly onto GaN wafers. This chapter will cover three key areas needed to successfully design create and test GaN devices. The device fabrication will be outlined including techniques used for standard HEMT design, dual gate HEMT design and the fabrication of a monolithically integrated buck converter. The testing methods needed to fully characterise these fabricated devices are also covered in this chapter and cover single device characterisation and full circuit testing. Finally, simulation methods are briefly covered involving both Sentaurus device level TCAD simulations and LTSpice circuit level simulations.

2.2 Wafer Epitaxy

Wafer epitaxies used in this research were supplied by a commercial supplier, NTT Advanced Technologies, and the University of Cambridge using metal-organic chemical vapour deposition (MOCVD). A typical wafer structure can be seen in figure 2.1 and consists of a Si substrate. A 250nm AlN layer as a nucleation layer was first grown on the Si substrate. This nucleation layer allows further AlGaIn/GaN layers to be grown easily as growing these materials directly on Si is extremely difficult. This is primarily due to the thermal mismatch between GaN and Silicon which can lead to cracks forming in the wafer structure. As well as this the AlN nucleation layer is needed to prevent a Ga-Si alloy forming^{1,2}. Following this, a 2 μ m graded AlGaIn strain relief layer is grown to gradually reduce the strain present in the wafer structure as growing GaN directly on AlN leads to too large of a lattice mismatch which can cause the wafer to crack and introduce large amounts of impurities. The differing thermal expansion coefficients can also contribute to the lattice mismatch. Then, a 1 μ m carbon-doped GaN buffer layer is grown as a back barrier for the 2DEG channel to ensure a good channel pinch-off at off-state and to achieve a high breakdown voltage. The channel region which will contain the 2DEG is then grown as a 250nm unintentionally doped GaN layer. This is followed by an AlN spacer layer used to enhance channel mobility. Then the 25nm AlGaIn barrier layer was grown, with an aluminium percentage of 25%. The final layer of the epitaxy structure is then a 2nm GaN cap layer used to improve the surface of the structure and reduce the gate leakage current.

GaN Cap – 2nm
AlGaN barrier – 21nm
AlN exclusion layer– 1nm
GaN Channel – 2000nm
Fe Doped Buffer Region – 2000nm
AlN Nucleation Layer – 250nm
Si Substrate - 675 μ m

Figure 2.1 - A cross section of the wafer structure seen in the NTT 1197 Wafer used in the buck converter fabrications.

2.3 Fabrication of a standard GaN High Electron Mobility Transistor (HEMT)

All the fabrication was performed in the Nanoscience and Technology device fabrication cleanroom at the University of Sheffield. The following steps outline the basic fabrication process of a standard GaN HEMT device. They provide the processes needed to be able to create custom devices and structures such as the buck converter and dual gate metal device which will be outlined after. The basic process flow can be seen in figure 2.2

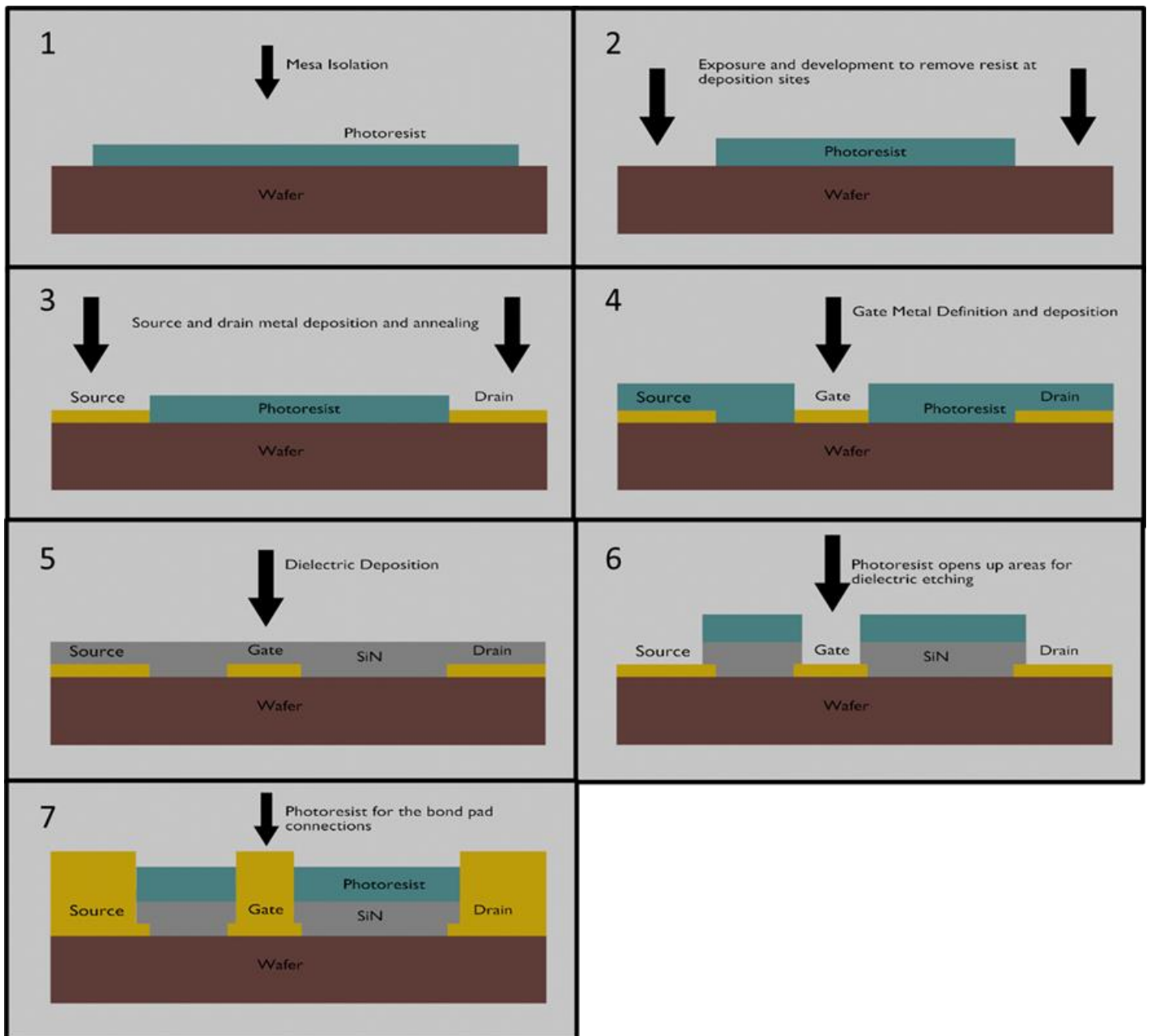


Figure 2.2 – The basic process flow of a basic GaN HEMT fabrication from top left to bottom right. Highlighting 1) Mesa isolation where photoresist is exposed and then 2) developed to remove the exposed areas. 3) Source and drain ohmic contacts are exposed and the metal deposited. 4) Gate contact region is exposed and the metal deposited. 5) Dielectric deposition is performed to act as passivation. 6) Openings to the contacts made through the passivation. 7) Contact pads deposited to allow easy testing of devices.

2.3.1 Sample Cleaving

Sample cleaving is the first step needed in device development. Small samples used to characterise singular devices are hand scribed using a diamond tipped scribe from a 6 inch GaN Wafer. For larger samples needed for the buck converter fabrications, wafers are cut into

35x35mm squares by Loadpoint as hand scribing is not a viable option due to the inaccuracy of sample size and leaving damage at the edge of the samples. These can be used without the need for scribing in buck converter fabrications as the mask size is designed to occupy all the space.

A diamond tipped scribe is used to score the material on the back. Repeatedly scribing straight lines to cut into the sample is done until the wafer is able to be broken. Breaking of the sample is usually done using two glass slides to apply equal pressure to either side of the scribe, breaking it along this joint.

2.3.2 Sample Cleaning

Sample cleaning is an important step to ensure no dust or debris is present on the surface that will prevent correct operation. As such, after almost all fabrication steps a three step cleaning process will be performed to remove oils, dust, debris or marks left on the sample surface.

The first step is to rinse the sample in boiling n-butyl acetate for one minute. The n-butyl acetate is good at removing any grease or oils on the sample.

The sample is then submerged in acetone for one minute to remove any other organic material that may have deposited on the surface. This is followed by a final rinse in boiling Isopropyl alcohol to remove any residue left on the sample from the other chemicals used for rinsing. A nitrogen air gun is then used to blow dry the sample which is then checked under an optical microscope to ensure the sample is clean. The process is repeated if the sample is not cleaned to a level of one particle per area magnified 100x.

2.3.3 1st stage photolithography – Mesa Isolation

The first stage of the device fabrication is to isolate the mesa area on the device. This is done using an Inductively coupled plasma (ICP) etch. Before this patterning of the mesa area is needed and is done using a photoresist and UV exposure. Mask plates made of glass with chrome patterning act to block the UV in the areas needed to remove the photoresist. The step by step process followed is below.

First prebake the sample for one minute at 100C to evaporate and moisture that may be left.

Mount the sample on a spinner and deposit SPR350 photoresist onto the sample. The sample is then spun at 4000RPM for 30 seconds, this ensures an even layer is formed on the surface. The sample is then baked at 100C for 1 minute to harden the resist.

A Karl suss mask aligner is then used to align the sample with the chrome mask plate. There are two mask aligners available UV300 and UV400 providing different wavelengths of UV (365nm and 405nm), leading to different exposure times. For this stage with no pattern on the sample it is important to ensure the whole mask design is included in the sample.

Once exposed the areas of activated photoresist must be removed, this is done using a developing agent called MF26A, this is done for 1 minute before a rinse in de ionised water and blown dry with nitrogen.

This is followed by etching using the ICP. An ICP etcher functions by creating a plasma using a high power RF frequency on the wafer platter. This plasma field strips the gasses pumped into the chamber of electrons creating a plasma that can react and etch away at the surface of the wafer. It etches the surface either by the force of the plasma colliding with the sample or by chemically reacting with the surface. The gasses used for GaN etching are typically chlorine and argon, with chlorine being the primary etchant³. The chlorine reacts with the GaN surface and produces volatile chlorides, GaCl₂ and GaCl₃ which are then etched away by the argon. A two-step etching power is used with a 15s high RF power (450W) to help strike the plasma followed by a lower power etch (350W). The lower power etch helps create less damage induced by the etching process and produces smoother mesa side walls. This second etch step typically lasts between 15 and 20 minutes and is monitored using a laser refraction monitor to ensure an etch depth of at least 600nm (etched down to C-doped GaN layer) is achieved. This ensures the mesa etch is well below the 2DEG and GaN channel region present to allow good electrical insulation between devices. Typically for this etch depth we have measured the mesa to mesa leakage through the buffer region to be around 10⁻⁶ mA/mm up to 100V. Any residual resist is the stripped away using EKC830 resist stripper, and this is followed by the three-step cleaning process as described above.

2.3.4 Second Stage Photolithography – Ohmic Contacts

The next stage is the definition of the ohmic contacts. Good quality ohmic contacts are key to allowing the GaN HEMT to have a low Ron as the contact resistance can make up a substantial proportion of the total Ron. A dual resist layer is spun on the sample to ensure that any excess metal is easily lifted off and is not left on the sample. This consists of PMGI spun first at 4000RPM for 30 seconds, followed by a post bake of 180C for 5 minutes to ensure the resist is fully hardened. Then the same SPR350 photoresist deposition procedure as before is

followed. PMGI acts as a thin under layer the develops faster than SPR350 allowed an undercut to form as seen in figure 2.3.

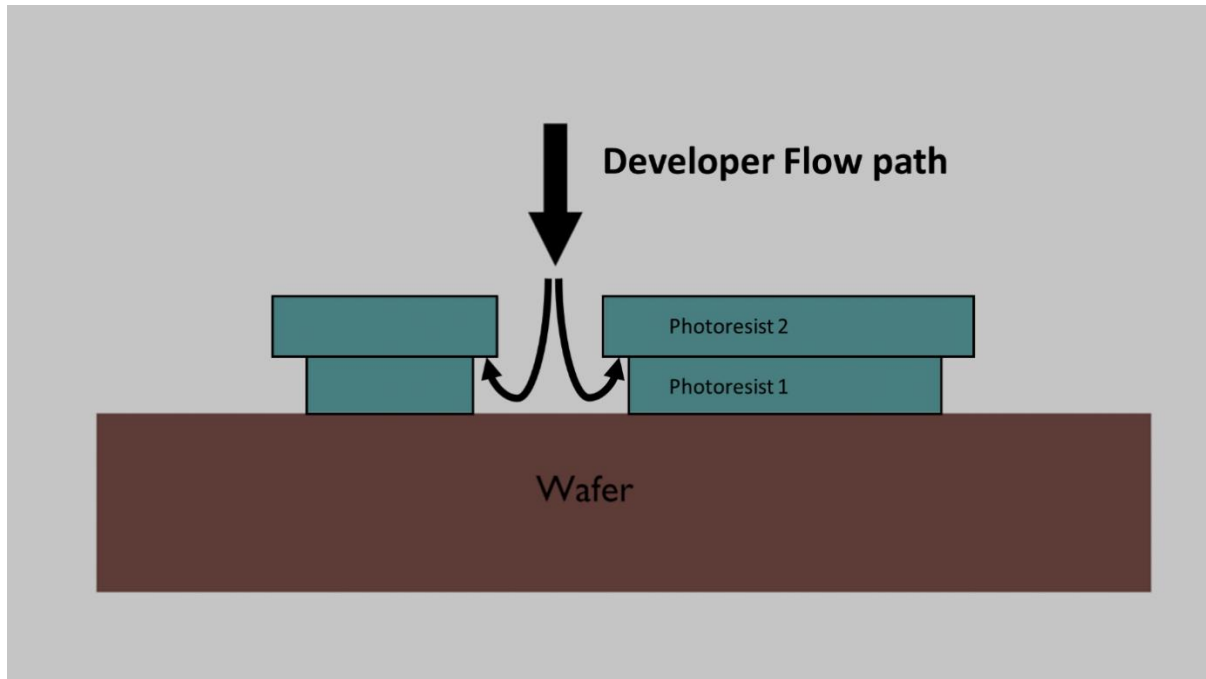


Figure 2.3 - A visualisation of how an undercut is produced using a dual layer photoresist and how this can aid lift off.

Alignment with the next chrome mask layer is then done using the same mask aligning process. Alignment marks are present to ensure that the ohmic contact falls correctly within the mesa defined areas. Developing is then done using the same process.

Following this an acid pre-treatment is performed using diluted HCl. GaN naturally forms an oxide on the surface when exposed to air and this can prevent metal diffusion into the epitaxial stack, so removal of this layer using acid is important. A one minute submersion in 1:1 HCl:DI water is done, followed by a rinse in DI water and then placed into the evaporator.

2.3.5 Ohmic Metal Contact Evaporation and Lift off

Metal contacts are then deposited onto the sample using a thermal evaporator. This consists of a pressured chamber, tungsten evaporation coils and a crystal monitor. The chamber is pumped down to a pressure around $4E-6$ mbar and high current is passed through the metal coils containing the evaporation metals that are to be deposited on the sample. Due to the pressure and current applied to the metals they evaporate and deposit evenly across the chamber, the total thickness evaporated is then monitored using a crystal thickness monitor.

Ohmic contacts require a metal composition that allows diffusion through the GaN surface layers down into the 2DEG layer. To do this typically a metal stack of Ti/Al/Ni/Au^{4,5} with thicknesses of 20/120/25/40 nm, respectively is deposited.

Lift off of the unwanted metal is then done by leaving the samples in EKC830 to remove the photoresist and any metal on top of this. This is necessary to allow the resist stripper to diffuse into the undercut created by the dual layer resist and removing the metal while leaving clean edges at metal deposition sites.

Annealing is needed to promote metal diffusion into the wafer structure to form an ohmic contact. Typically, 775 °C for 60 seconds is used to allow diffusion of the ohmic contacts into the wafer. Variations in ohmic contact quality can be caused by several process variations that may occur during fabrication. The amount of time between the HCl treatment and placing the sample in the evaporator can affect the surface oxide regrowth and hence contact quality. As well as this during evaporation if coils are not directly over the monitoring system slightly different thicknesses of each metal may be deposited, affecting the ohmic contact quality.

Typically following this process for the ohmic contacts a resistance of 1Ω.mm is achieved when extracted from TLM measurements.

2.3.6 Third stage of lithography – Defining the Gate region

Gate lengths used in this work are targeted at sub-μm, which is difficult to achieve with the photolithography setup available. As such an electron beam lithography (EBL) is used to define the gate contact region.

An EBL uses a focused beam of electrons to ionise an electron sensitive resist, similarly to using UV light to activate a photolithography resist. As a focused beam of electrons is used, it is much easier to achieve sub-μm feature sizes. The electron wavelength is usually much smaller than that of photons and depends on the acceleration voltage⁶. This smaller wavelength means in turn that smaller features can be patterned using this system. This beam is then controlled by the E-Beam system to pattern features without the need to use a physical mask as with photolithography. A dual layer resist is used to ensure that lift off is possible with a slightly thicker metal stack deposition is possible. PMGI spun at 8000rpm and PMMA diluted 1:1 spun at 4000RPM are used to give around 1μm total thickness of resist. A virtual mask is loaded into a program designating the areas that need to be exposed to the electron beam. Alignment is done similarly using crosses defined by the ohmic metal and aligning them to the

virtual mask. After exposure development is then performed using Xylene for 1 minute followed by a rinse off in IPA.

2.3.7 Schottky Gate Contact Deposition

Gate contacts are then deposited using metal evaporation. As these metal contacts form Schottky contacts with the GaN surface, only the metal directly in contact with the surface defines the Schottky barrier. A 20-30nm thick of the Schottky metal, such as nickel, palladium or titanium, is deposited followed by 100-200nm of gold. The thicker gold layer to help reduce the contact resistance. To achieve a good lift off, the aspect ratio of the resist to the metal thickness must be considered. The resist must be at least twice as thick as the metal thickness deposited. This ensures that the lift off completes correctly as if the resist is too thin it will not be able to remove the metal during the lift off process. The CSAR62 used for the EBL step is around 400nm so usually no more than 150nm of total for the metal stack is deposited.

2.3.8 Dielectric Deposition

Dielectric deposition is a key step for GaN devices and is required to passivate the surface of the GaN device. This is to reduce surface trapping effects and reduce the device leakage as well as dynamic Ron effects. It is done using Plasma Enhanced Chemical Vapour Deposition (PECVD), similar to the ICP it uses a high power RF plasma and gas flow rate to deposit the passivation.

Both silicon dioxide and silicon nitride (SiN) are the commonly used as passivation materials^{7,8} for GaN devices although the primary passivation used in this study will be SiN. Silane, nitrous oxide and ammonia are used as the reactant gasses to produce these. When depositing the dielectric an RF frequency at 13.56MHz with a power of 25W is used to deposit the passivation onto the sample which is heated to 300 °C at the base of the chamber. Typically thicknesses between 70 and 120nm of SiN are deposited to passivate the surface.

2.3.9 Reactive Ion Etching for Silicon Nitride (SiN) via opening

Reactive ion etching (RIE) is used to etch through the SiN layer to access the metal contacts. RIE works similarly to ICP etching in that a high RF power is used to generate a plasma that, along with gasses in the chamber, will attack the passivation and etch away. Typically CHF₃ and O₂⁹ with a flow rate of 35sccm and 5sccm are used to an etch rate of ~40nm per minute.

2.3.10 Bond-pad metal deposition

The final stage in a standard device fabrication process is the deposition of the bond-pads to allow for probing of the device. The same process steps are followed as with a typical Schottky

pad deposition. Photolithography followed by Schottky metal deposition, Ni/Au although typically thicker metals are used at 40/400nm.

2.4 Device Characterisation

Device measurements are performed using multiple source-measurement units (SMUs) connected together and controlled using LABVIEW programs. These programs allow control of each terminal of the devices to allow current measurements to be made at the same time as voltages are applied to various device terminals. The SMUs are (add SMUs). The main programs used for the measurements are Transmission line measurements (TLM), Gate transfer (GT) measurements, IV measurements and breakdown voltage measurements. As well as this a number of circuits have been produced to test each of the monolithically integrated buck converters. These utilise fixed power supplies and a (brand) oscilloscope to calculate the efficiency of the devices.

2.4.1 Two Terminal Measurements

TLM measurements are the first set of two terminal measurements usually performed to test the device has good ohmic contacts . A two terminal measurement is performed by probing the source and drain ohmic contacts on the device to ensure they have correctly formed and diffused into the 2DEG. The TLM structure used can be seen below in figure 2.4 and features ohmic contact pads at various separations between 2um to 20um.

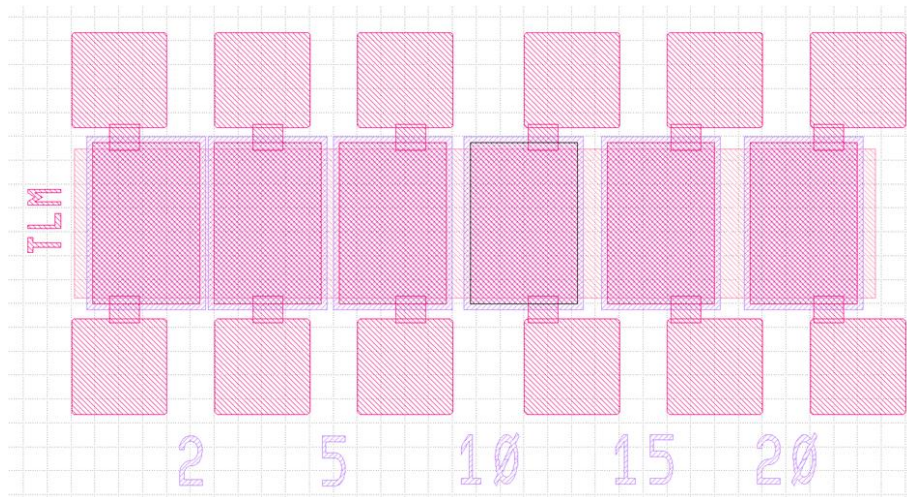


Figure 2.4 – The mask outline used to define the TLM structure showing the increasing separation between probe points

A plot is produced showing the resistance for each separation and the contact and sheet resistance can be extracted from this plot.

The contact resistance is given by half of the y intercept over the voltage measurement. The sheet resistance is given by the slope multiplied by the device width. The total device resistance can then be shown by the equation 2.1.

$$R_{total} = 2R_{contact} + R_{sheet} \frac{L}{W} \quad 2.1$$

Where R_{total} is the total device resistance, $R_{contact}$ is the contact resistance of the device, R_{sheet} is the sheet resistance, L is the device length and W the Width.

2.4.2 Three Terminal Device Measurements

The gate transfer of the device is a three terminal measurement where the gate source and drain of a transistor are probed. A fixed drain source (V_{ds}) bias is applied, usually around 10V and the gate source (V_{gs}) voltage is swept from the device off state up to on state, the plot is shown as the normalised current in the device against the gate voltage. As GaN HEMTs are normally off devices the device is usually swept up to 0V. The main device parameters that can be extracted from this measurement are the transconductance of the device and the threshold voltage (V_{th}). Figure 2.5 shows a typical gate transfer and transconductance plot.

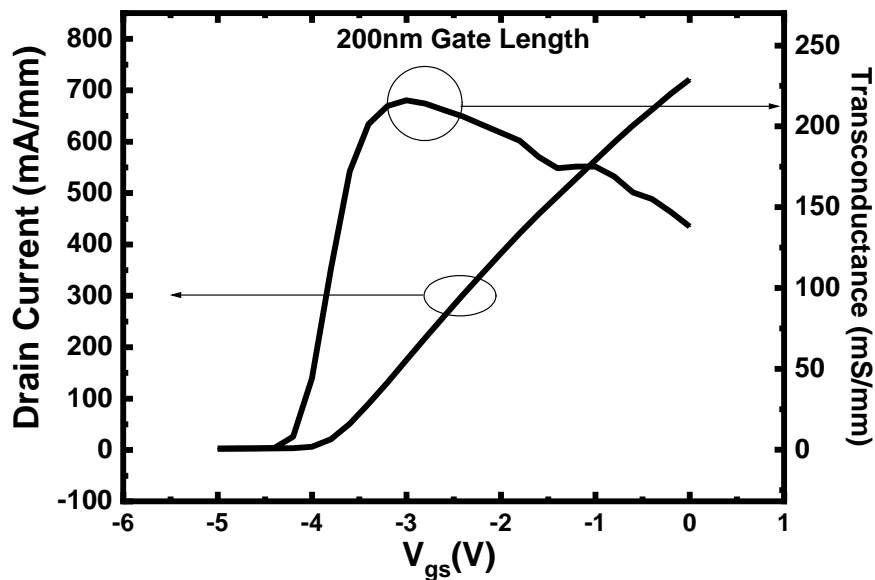


Figure 2.5: A typical gate transfer plot of a 200nm device with a gate length of 200nm. The device is a single gate device with a gate width of 125um. V_{gs} is varied between -5 and 0V is used with a V_{ds} of 10V and the current between source and drain measured. The transconductance is then calculated from the IV plot.

The transconductance of the device is extracted by plotting the differentiated version as it is given by the rate of change of the slope of the gate transfer plot. Typically, peak transconductance values for the GaN devices are between 200 and 300mS/mm.

The threshold voltage of the device can be extracted by first finding the voltage at which the maximum transconductance of the device occurs. Then by making a tangent to this point and extracting where this crosses zero current this new voltage can be taken as the threshold voltage.

The IV is another key three terminal measurement and allows the calculation of the device R_{on} . For this measurement again the source is grounded and the V_{ds} is swept from 0V to usually 10-20V. A plot of the device current against the drain voltage can then be used to calculate the R_{on} of the device by extracting the resistance between 0 to 1V V_{ds} . This can be seen in figure 2.6.

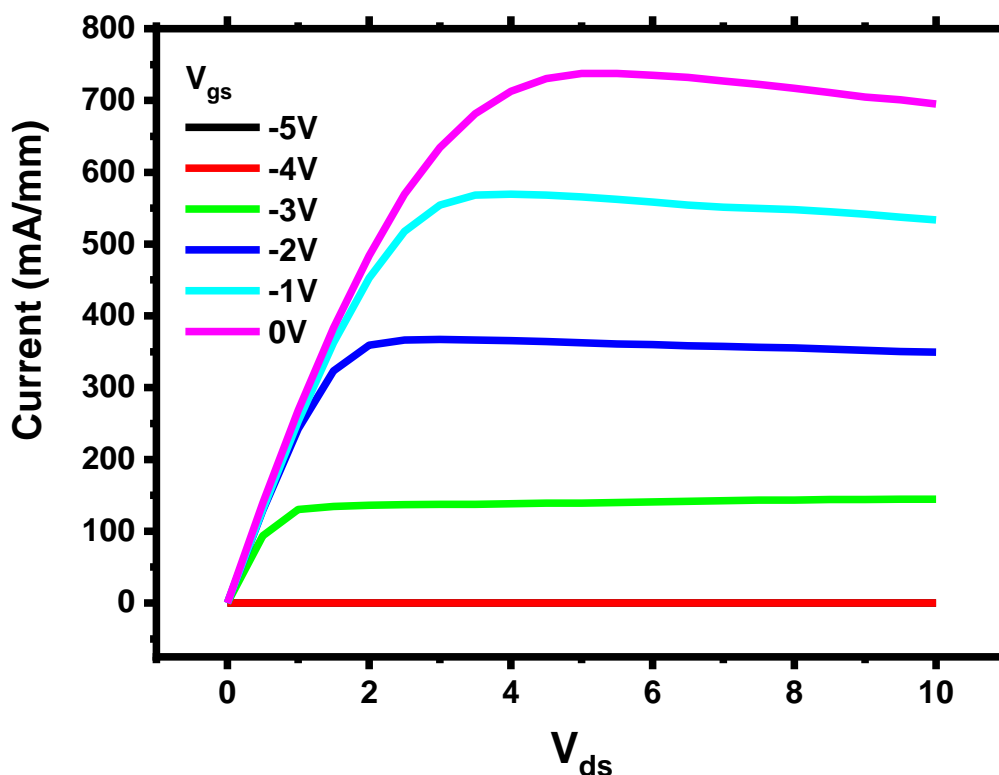


Figure 2.6 – A typical IV plot of a device with a 125 μ m gate width and 200nm gate length. V_{gs} is varied between 5V and 0V in 1V increments and a sweep of V_{ds} from 0V to 10V is made.

2.4.3 Pulsed Measurements

Dynamic Ron characterisation is very important to ensure the success of field plate integration into devices. Comparisons between identical devices both with and without field plates can be compared to ensure that they effectively suppress current collapse in the device.

An external circuit was created and used to measure the dynamic Ron. The circuit is designed to deliver a high drain voltage to the device for a longer time frame, over 500uS, then remove the drain stress and quickly, 10us, pulse the gate of the device from off state to on state. The circuit operation is as follows, Q1 is a high voltage silicon carbide JFET which is normally on. When a high voltage stress voltage is applied to the circuit at P9 this ensures the voltage bypasses the device under test (DUT). Once the DUT is connected this JFET is turned off causing the stress voltage to be applied across the drain and source of the DUT. This stress voltage causes the carriers to become occupied in traps, reducing the device carrier concentration and increasing the Ron. After the stress voltage is applied for 500us, Q1 is switched back on to remove the stress voltage and the DUT is turned on to allow current to flow through and the dynamic Ron value to be calculated. By varying the drain stress in the device and measuring the current through the device a profile of dynamic Ron can be built up across a range of voltages.

2.4.4 Capacitance Voltage (CV) Measurements

CV measurements are an important set of measurements that can extract a number of device parameters to aid with characterisation. The devices capacitance, AlGa_N thickness and 2DEG density can be extracted which in turn allows calculation of the mobility and Schottky barrier height. A Keithley LCR meter is used to extract the capacitance values and care must be taken to ensure the phase angle of the measurement is close to 90 degrees to ensure the measurement is accurate. Figure 2.7 shows an example CV measurement.

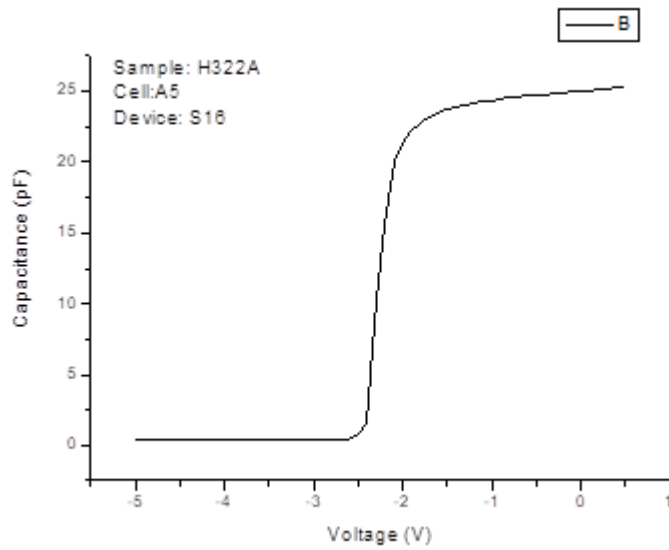


Figure 2.7 - A standard CV measurement plot for a circular CV measurement device with diameter 200um and Nickel Schottky contacts.

2DEG density is calculated from equation 2.2

$$n_s = \frac{CV}{qA} \quad 2.2$$

Where n_s is the 2DEG carrier density, C is the capacitance, V is the voltage, q is the electron charge, and A is the area of the device.

AlGaIn thickness can be calculated from CV measurements using equation 2.3.

$$C = \frac{\epsilon A}{d} \quad 2.3$$

Where ϵ is the dielectric constant, A is the area of the device, and d is the distance from the surface the 2DEG channel in the device is located.

2.5 FPGA Testing

The Field Programmable Gate Array (FPGA) is an intel Stratix V with the capability to provide a number of control signals that can be fed into the buck converter. There are a number of high speed clock signals within the FPGA that can be used to generate digital pulse signals used to switch the system. Due to the nature of the FPGA these high speed signals cannot provide a large enough voltage to fully switch the gate driver fully from off state to on state so a digital isolator that can increase this voltage is required, that can provide a swing of 5V.

The programs have been created in the Quartus software using the block diagram program creation feature. This makes use of an inbuilt PLL controller that can be assigned to the appropriate clocks to generate the signal required. The system has a number of high speed clocks that can be addressed, a 625MHz, 644MHz, 270MHz and a 282MHz one that are all fast enough to generate a 50MHz signal. These clocks are connected to the PLL and the PLL settings are adjusted for each to ensure the input is correct and the output timings are correct.

There are two main programs created, one for the multi-level setups and one for the single level setups. The single level program has two signals generated at 50MHz switching inversely to each other with a 10% dead time between the signals. This is to ensure no overlap between the two signals by accommodating for a slow slew rate. The duty cycle of each is altered to correspond to the required output power. The other setup for the multi-level circuits has one switched on signal and one switching signal to accommodate for the higher level switching operation modes.

2.6 Bonded buck converter testing

The monolithic buck converters are bonded into a package using gold wire and these packages are then soldered into testing circuits. A testing circuit has been created for each buck converter schematic and these all follow the same basic schematic. The circuits utilise a digital isolator to make sure the FPGA signal is separate from the power signal used in the switching. ISO7760-DBQ is the chosen isolator as it has six channels, enough to isolate all the signals needed for every configuration of buck converter. Its operation speed has a theoretical maximum of 100Mbps. The circuits also have external capacitors to aid with testing should the internal ones fail as well as an external inductor.

2.7 Simulations

Two main types of simulations have been performed and matched to experimental results to allow the prediction and verification of data. LTSpice is used for level circuit modelling of the buck converter and Sentaurus TCAD is used for device level simulations. Sentaurus TCAD is primarily used for simulations involving the DMG devices and the field plate designs. It allows for the extraction of device level parameters such as transconductance and the on-state resistance of devices.

2.7.1 Sentaurus

Sentaurus is simulation software that allows device physics level simulations. It has built in models and parameters that can be used to simulate GaN accurately. This allows the simulation of not only different device topologies but also simulations of different wafer epitaxies to allow an insight into how this affects various device parameters. This software was primarily used for both the dual gate device structures as well as the field plate simulations. Dual gate devices were simulated using this software and once experimental results were matched to the results, simulations were produced to investigate the internal physics at play that gave rise to the advantages brought about using this topology. For the field plate simulations, capacitance changes in the device were extracted and used in conjunction with SPICE to produce quick estimates on device efficiencies.

Sentaurus is a commercial device TCAD simulator which allows an in-depth view at the physical properties within the device in order to achieve a greater understanding of device function. The two main programs within the software used to produce the device simulations are Structure Editor, used to create the device structure, and Sentaurus Device, used to simulate the electrical characteristics of the structures. The software has a number of in-built materials and AlN, GaN and AlGaIn are part of this set allowing easy addition of the materials into the simulations.

Sentaurus Device then again uses code to define the voltage and current values as well as the physics parameters to use within the simulations. An example of the physics section of the code is shown below and explanations of the sections within it are broken down.

Physics {

AreaFactor= 1000

The AreaFactor refers to the theoretical width of the device, the simulations are performed in 2D so this is simply a scaling factor.

Mobility (

DopingDependence

Highfieldsaturation

)

This section defines which physical factors affect the mobility of the carriers, the doping in the device as well as the velocity saturation.

Piezoelectric_Polarization (strain(GateDependent))

```

Aniso(Poisson direction=(0, 0, 1))
EffectiveIntrinsicDensity (Nobandgapnarrowing)
Fermi
Recombination(
    SRH
)
Thermionic
eBarrierTunneling "SourceNLM"
eBarrierTunneling "DrainNLM"
}

```

Piezoelectric polarization is defined and specified to be dependent on the gate work functions. Aniso is the anisotropic property of the GaN material and the direction the GaN is simulated in. Effectiveintrinsicdensity no band gap narrowing keeps the band gap stable for the simulation. Fermi defines the dopant diffusion model used. The recombination is defined as a Shockley-read-hall recombination and is based on that model. Thermionic adds thermal effects into the device, which as they are a key factor in device performance are needed to build an accurate model. eBarrierTunnelingg defines the tunnelling present at the contacts for the source and drain.

```

Physics (MaterialInterface="GaN/Nitride") {
    Traps(
        (Donor Level Conc= 5e13 EnergyMid= 0.3 FromCondBand)
    )
}

```

Donor doping is defined between material interfaces, both in the GaN and carbon doping. The concentration and donor level is defined in the above example defined at a concentration to allow the formation of the 2DEG. This is defined at levels close to measured results from the real devices although slight alterations are made to make the devices more closely match them results wise.

The simulated device has been created in Sentaurus to emulate the real device wafer epitaxy and fabricated structure. The wafer structure consists of a bottom silicon substrate of thickness 1mm. This is followed by a GaN:C buffer region carbon doped to a similar level as the real epitaxy, around $1e18 \text{ cm}^{-3}$. The GaN channel region is then defined at a thickness of 250nm, followed by a 1nm AlN spacer layer. Then a 25nm AlGaIn barrier layer with an aluminium

percentage of 25% is simulated. Finally, a GaN cap of thickness 2nm and Si_xN layer with a thickness 50nm is added. The simulated structure in Sentaurus can be seen in figure 2.8.

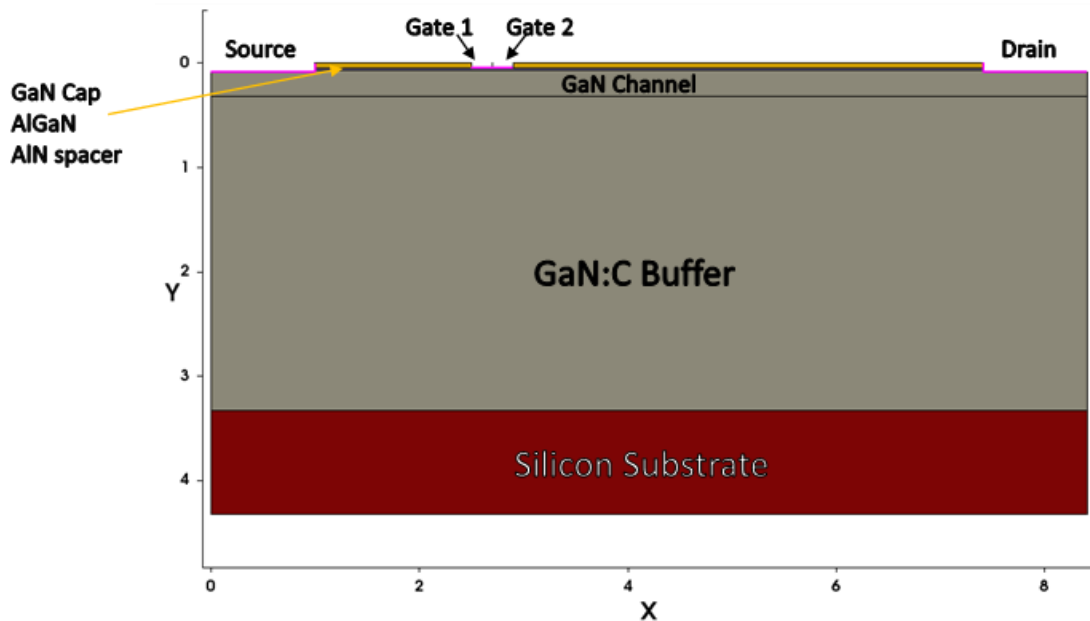


Figure 2.8 – The typical DMG device structure used in the Sentaurus simulations.

There are a number of other parameters used in the Sentaurus simulations such as electron mobility in the GaN and the physics simulations used when calculating the results. These have been configured to give a close match to the experimental results ensuring that the physics simulations used to explain the device parameters are accurate to real results. A simulated gate transfer compared with an experimental device is shown below in figure 2.9, the maximum difference in current is around 5%.

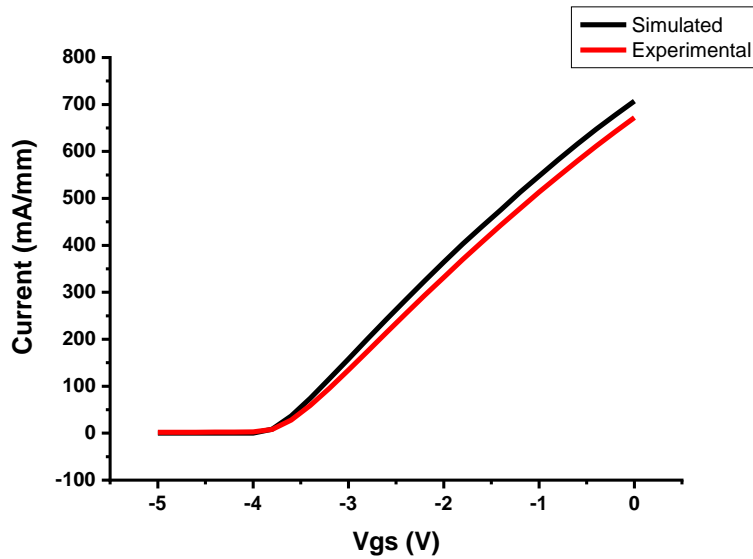


Figure 2.9 – A comparison between a simulated and experimental gate transfer plot for a 125 μ m width device with a gate length of 400nm. A V_{ds} of 10V was used with the V_{gs} swept between -5V and 0V.

2.7.2 SPICE

LTSpice has been used to simulate device performance for the various buck converters and also to help verify the field plate study. These circuit level simulations allow fast prototyping and changes to be made to the circuits without the need for recreating a physical circuit. The circuits also allow a greater understanding of the circuits by allowing instantaneous voltage and current values to be seen at various points within the circuit.

All the SPICE circuits consist of a basic JFET model that has been modified to behave closer to the devices we fabricate. The JFET is used in conjunction with parasitic capacitances that match our fabricated GaN HEMT devices. This allows us to simulate the impact changing device parameters will have on whole integrated buck converter circuits in terms of frequency and efficiency.

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Chapter 3 - Dual Gate Metal (DMG) AlGaIn/GaN HEMTs

3.1 Introduction

The suitability and motivation behind pursuing dual metal gate (DMG) transistors has been outlined in chapter 1 Section 1.3.2. There has already been work providing evidence of their advantages in improving transconductance over the conventional single metal gate (SMG) devices.¹⁻⁵ We further this work by going into detailed analysis of the drain-induced barrier lowering effect (DIBL) improvements this layout achieves and the physical reasons behind this. This chapter outlines the key reasons behind all of these advantages and analyses some key challenges and drawbacks brought about by this approach. The most obvious of these challenges is the increased device complexity brought about by the need to fabricate multiple gates and ensure a very accurate alignment is achieved. This becomes a more difficult challenge as gate length decreases further which is where the DIBL improvement becomes more apparent.

The chapter begins with the device fabrication of the SMG and DMG AlGaIn/GaN HEMTs. Experimental result comparisons between the SMG and DMG HEMTs including transconductance, output current density, off-state leakage current and DIBL will be presented. Technology Computer Aided Design (TCAD) device simulations are employed which allow an insight into the key differences in the device physics between these devices. Electron mobility, electric field plots and saturation velocity plots will be presented from the simulations and used to explain the differences between the SMG and DMG.

3.2 Single Metal Gate (SMG) and Dual Metal Gate (DMG) HEMT Device Fabrications

The AlGaIn/GaN epi-wafers used in this study are as described in Chapter 2, Section 2.2. The device fabrication steps for the SMG and DMG HEMTs are as previously outlined in chapter 2 section 2.2. Devices with gate lengths of, 1 μ m, 600nm, 400nm and 200nm were fabricated with a source-gate separation (L_{sg}) of 1 μ m, gate-drain separation (L_{gd}) of 5 μ m and gate width of 125 μ m. During metal deposition, 30nm of the Schottky, either titanium or palladium, metal followed by 100nm of gold is deposited for each gate. For the DGM devices, two separate EBL steps are performed with each of the different Schottky metal depositions performed in between. This allows two gates with different metal stack compositions to be made. An overlap has been created in the mask that ensures the second gate pattern slightly overlaps the first gate to ensure that there is no gap between the metal stacks. Palladium (Pd) with a work function

(WF) of 5.1 eV and titanium (Ti) with a work function (WF) of 4.3 eV⁶⁻⁸ are used for the gate metals in this study. Secondary electron microscopy (SEM) was used to check the gate length and alignment between 2 gate metals in the DGM devices. Figure 3.1 shows a visualisation of the DMG HEMT device. Figure 3.2 shows the SEM picture of a 500nm/500nm DMG.

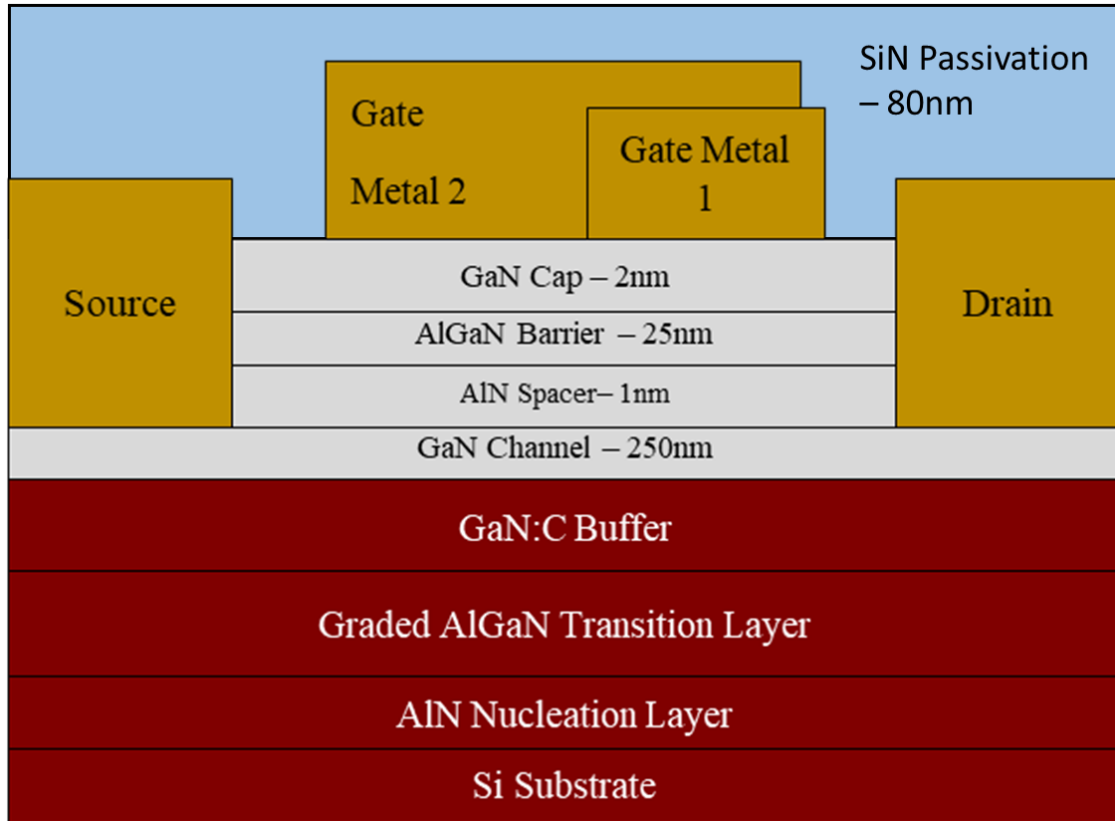


Figure 3.1: A visualisation of the DMG HEMT device structure showing the gate overlap

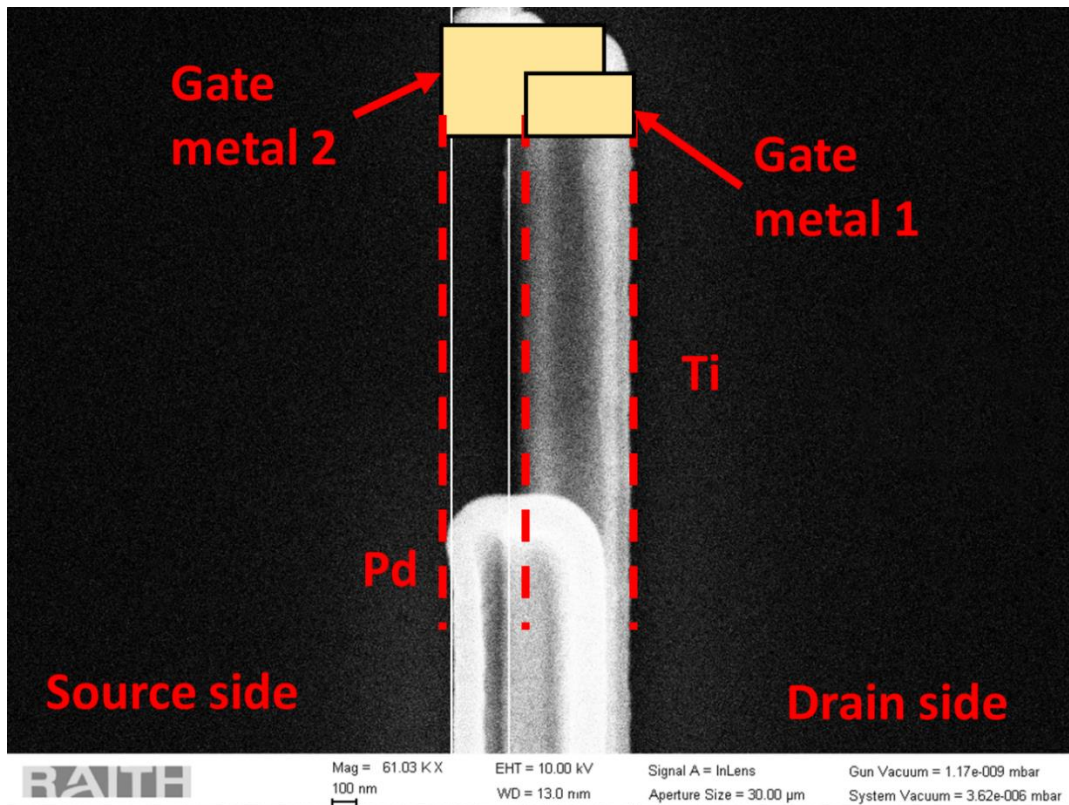


Figure 3.2 – An SEM image showing the gate alignment in a 200/200nm DMG device

3.3 Results

3.3.1 Threshold Voltage Schottky Extraction

Due to the fact the improvements presented through the DMG structure are dependent on the metal work function gap between the two metals, the extraction of the Schottky work function of the metals is important.

The method of Schottky barrier height extraction used was by depositing a large Schottky contact on the wafer at the same time as each of the metal gate depositions⁹⁻¹¹. The device structure used to take these measurements can be seen in figure 3.3.

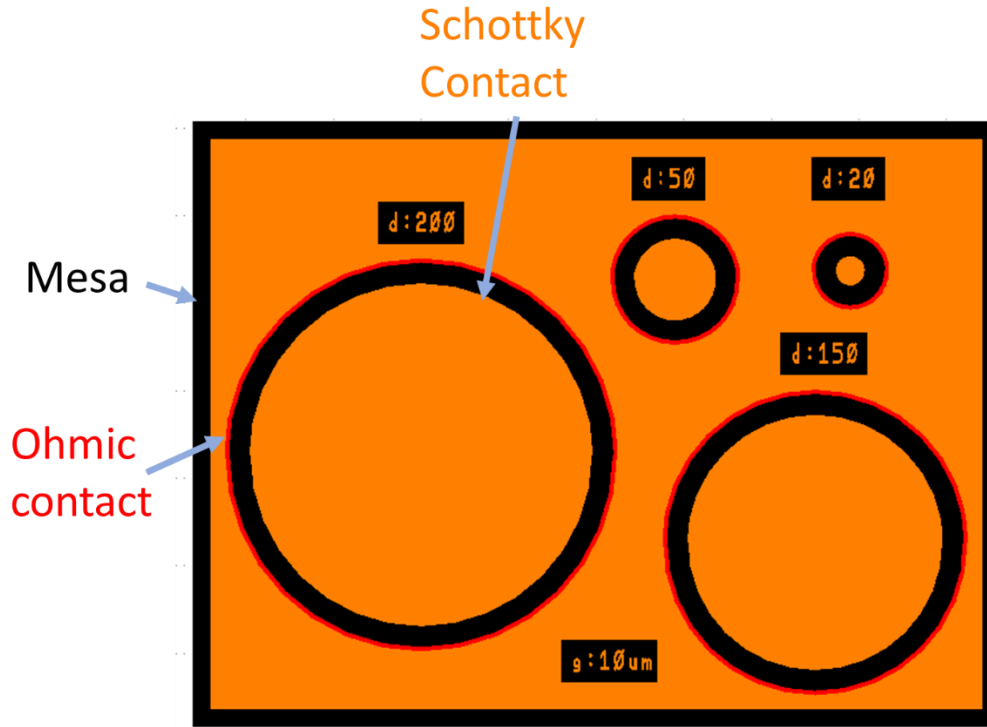


Figure 3.3 – The circular Schottky diode used to measure the Schottky barrier height of the two metals used in the DMG device.

This was performed for each metal on two separate diode devices which allows an IV measurement to provide the values needed to calculate the Schottky barrier height.

The threshold voltage of the devices can be extracted using the equation^{12,13} seen in equation 3.1:

$$V_{th} = \frac{\phi_B - \Delta E_c}{q} - q \frac{d_B}{\epsilon_B} \sigma_{pol} + \frac{E_F}{q} \quad 3.1$$

Where ϕ_B is the Schottky barrier height, ΔE_c is the conduction band discontinuity, q is the charge of an electron, d_B is the thickness of the barrier layer, ϵ_B is the permittivity of the barrier layer, σ_{pol} is the polarisation charge density present at the AlGaN/GaN 2DEG interface and E_F is the difference between the fermi level and the conduction band at the GaN channel. As the data shown is for devices all fabricated on the same wafer composition, the only factor in determining the V_{th} of the devices is the Schottky barrier height. To extract the barrier height from an IV plot the equations 3.2 and 3.3 are used.

$$I = I_0 \left(\exp \left(\frac{qV - IR_S}{nkT} \right) - 1 \right) \quad 3.2$$

$$I_0 = AA^{**}T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \quad 3.3$$

Where I_0 is the saturation current, Φ_B is the Schottky barrier height, R_S is the series resistance, n is the ideality factor, k is the Boltzmann constant and T is the temperature. A is the Schottky diode area, A^{**} is the Richardson constant taken to be $35A \text{ cm}^{-2}K^{-2}$ 14,15.

The two IV plots seen in figure 3.4a and b were extracted from circular Schottky pads with a 150um diameter. Using a least squares fit on the graphs allows the values extracted from the graph to be used in equations 2 and 3 to extract the Schottky barrier height and in turn the threshold voltage shift that will be seen from the different metals used. For the fabricated devices the two metals used were Ti and Pd with Schottky barrier heights in literature reported to be around 0.6eV and 1.2eV respectively. The extracted values calculated from the measured devices were 0.57eV and 1.18eV, close to the expected values, giving a barrier difference between the two of 0.61eV. This then directly translates to a threshold voltage shift of 0.6V as the only difference between the two fabricated devices is the Schottky barrier height of the two metals.

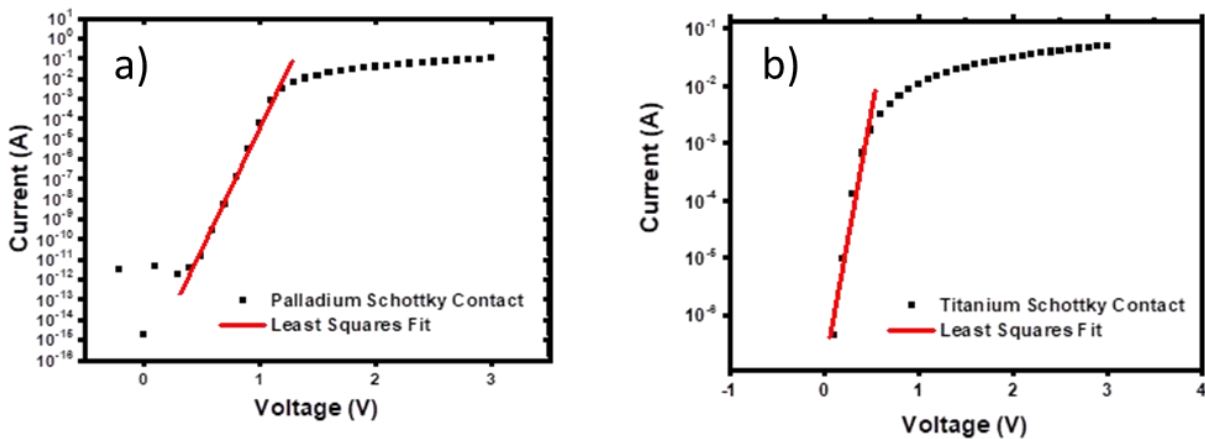


Figure 3.4: The IV plots used to extract the Schottky value for the different Schottky contacts. The current is shown in a log scale to allow for extraction of I_0 using a least squares fit shown in red. a) palladium and b) titanium

This again is consistent with the measure threshold voltage shift in the SMG devices and also the shift between the DMG device and the titanium SMG device. This leads to the conclusion

that as the higher metal work function pinches off first, it is that barrier height that determines the devices threshold voltage. This is primarily due to the fact the higher Schottky barrier height a lower gate voltage is needed to deplete the 2DEG channel and therefore pinch off the device.

The primary reason for the simulations is to verify the physical concepts that give rise to the DMG device structure advantages. Electrical field manipulation can be visualised using these results to verify that the transconductance and DIBL improvement are due to the interface between the two metal work functions. Verification of the experimental results will also be done by the simulation results to ensure that the improvements seen are explainable by the structure changes and to help provide ideal targets to aim for.

In this section the results for the transconductance will be shown and peak field, saturation velocity and 2DEG density will be shown. The shielding effect that gives rise to the DIBL improvement will be shown. Finally, the results will be compared to the experimental results.

3.3.2 Transconductance improvement

3.3.2.1 Experimental Results

As well as the simulation results we can present some experimental results showing the improvement in transconductance scaling down to 200nm. Figure 3.6 shows the four possible metal orientations that could be used to create gate lengths with a total length of 1 μ m. This demonstrates the Pd/Ti configuration does in fact provide the highest gm consistent with the hypothesis and simulation results. As well as 1 μ m devices, 600nm, 400nm and 200nm gate length devices were fabricated and as can be seen in table 3.1 below all the DMG devices show a higher transconductance than the SMG devices. This improvement varies between 9-6% and was measured from an average of 10 devices with each gate configuration.

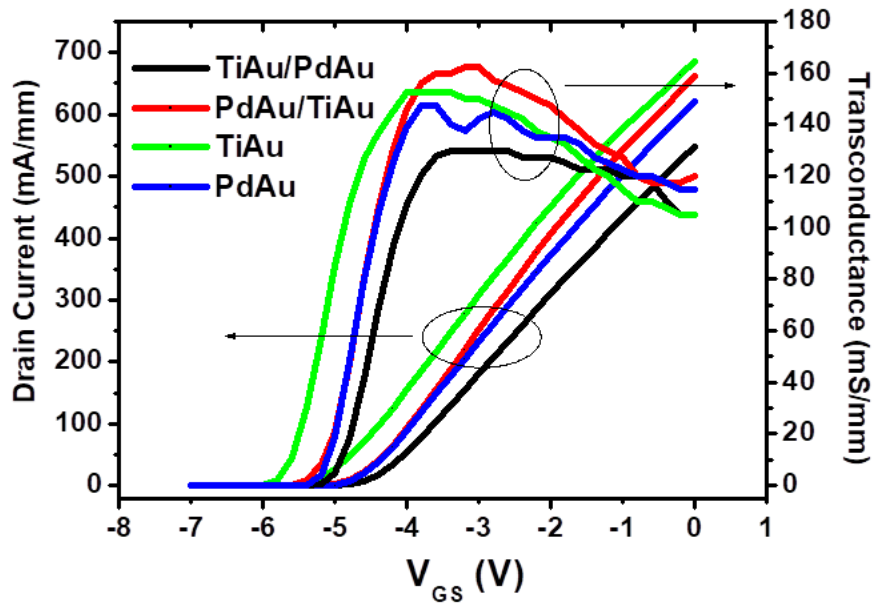


Figure 3.5 - A gate transfer showing both drain current and transconductance for a range of DMG devices. The devices all have total gate lengths of 1 μ m and gate widths of 125 μ m. A V_{ds} of 10V is used and V_{gs} is swept from -7V to 0V.

Gate Configuration	gm (mS/mm)	Percentage improvement in gm
500nm/500nm – DMG (Ti/Pd)	162	8.7%
1 μ m – SMG (Pd)	149	
300nm/300nm – DMG (Ti/Pd)	204	7.9%
600nm – SMG (Pd)	189	
200nm/200nm – DMG (Ti/Pd)	211	5.5%
400nm – SMG (Pd)	200	
100nm/100nm – DMG (Ti/Pd)	229	6%
200nm – SMG (Pd)	216	

Table 3.1 - The transconductance improvement present in the devices with a gate width of 125 μ m and gate lengths with a range between 1 μ m and 200nm. The results are an average of 10 devices with IV characteristics extracted from a test setup of V_{ds} 10V, and V_{gs} swept

between $-7V$ and $0V$. The percentage improvement shows the difference between the DMG and SMG with same total gate length.

A visualisation off this for a more clear comparison is shown below in figure 3.6 below.

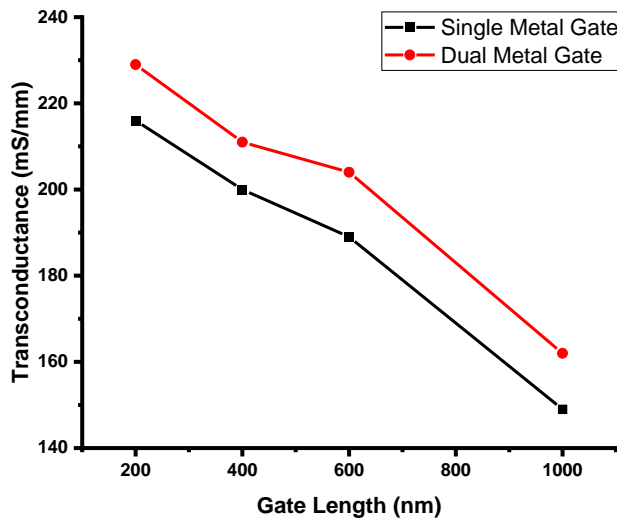


Figure 3.6 - A plot of the g_m against gate length for a range of SMG and DMG devices shown in table 3.1. The results are an average of 10 devices with IV characteristics extracted from a test setup of V_{ds} 10V, and V_{gs} swept between $-7V$ and $0V$.

Unsurprisingly, the improvement in transconductance leads to an improvement in the output current in the saturation region of the device. In figure 3.7 a plot showing the output characteristics in the 400nm gate length device and the higher current at saturation is presented.

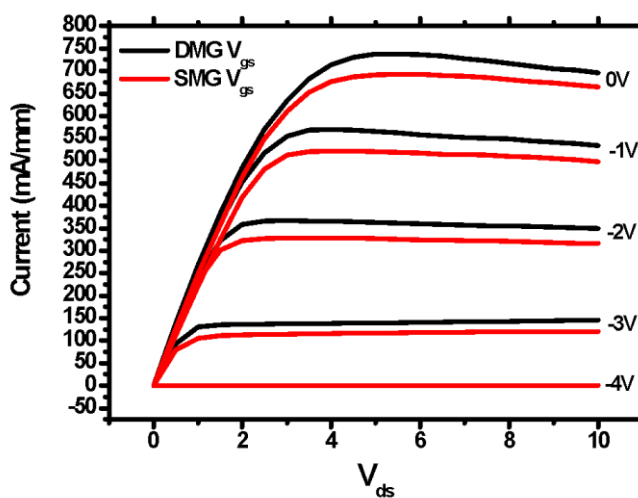


Figure 3.7 – A comparison of output characteristics of the DMG and SMG HEMTs with 400nm gate length and gate width 125 μ m. IV characteristics are extracted from a test setup with V_{gs} from -4V to 0V at 1V intervals, and V_{ds} swept between 0V and 10V.

Another interesting comparison to make is between a DMG device with double the gate length of the SMG device, for example 200nm Pd SMG and 200nm/200nm Pd/Ti DMG devices. This comparison is interesting as both devices will have the same Pd metal gate length (i.e. 200nm) which in the DMG device should primarily control the threshold voltage and peak gm seen in the gate transfer characteristics as seen in figure 6. Comparing between these two allows it to be seen if the Ti has a negative effect on overall gm as it will double the gate length. This is necessary to see as the fabrication technology is the same for fabricating a DMG as fabricating a SMG with half the gate length. This means if no advantage in the device transconductance is seen in this device or even a large enough disadvantage in gm it will not be worth fabricating. Figure 3.8 shows a comparison between the 400nm DMG device and the 200nm SMG device.

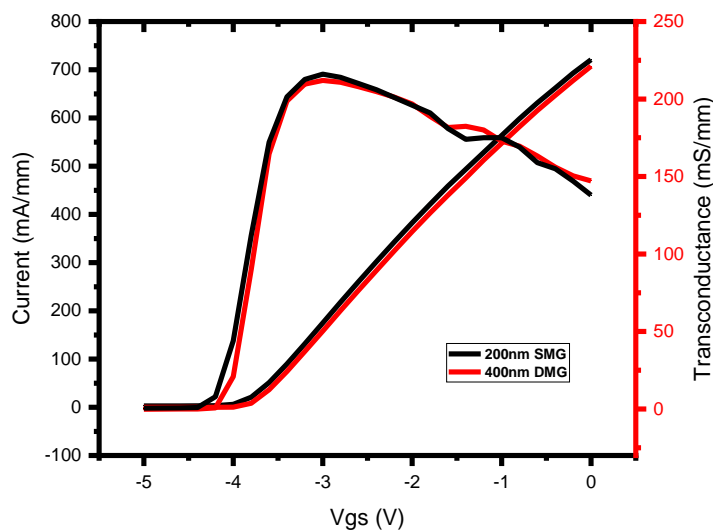


Figure 3.8: Gate transfer characteristics of devices with a gate width of 125 μ m and gate lengths of 200nm Pd SMG and 200nm/200nm Pd/Ti DMG devices. With a V_{ds} of 10V and V_{gs} swept from -5V to 0V.

It is shown the DMG device has a very similar overall gm when compared to the SMG device. This is good as it means even with a gate length double that of the SMG device the second spike in the electric field and increased electron velocity present under the gate mitigates the larger gate length.

As the percentage increase in the table 3.1 remains consistent across decreasing gate lengths if it is assumed the trend continues this will provide larger benefits at smaller gate lengths. This is due to the worse DIBL that is seen at lower gate lengths which again is mitigated by the DMG structure.

3.3.2.2 Simulation Results

The transconductance improvement is primarily due to the work function difference between the two metal gates giving rise to a spike in the electric field at the interface between the metals in the 2DEG channel. This is only present in the DMG device as the SMG has a gradual increase in the electric field up to the drain edge of the gate as shown in figure 3.9.

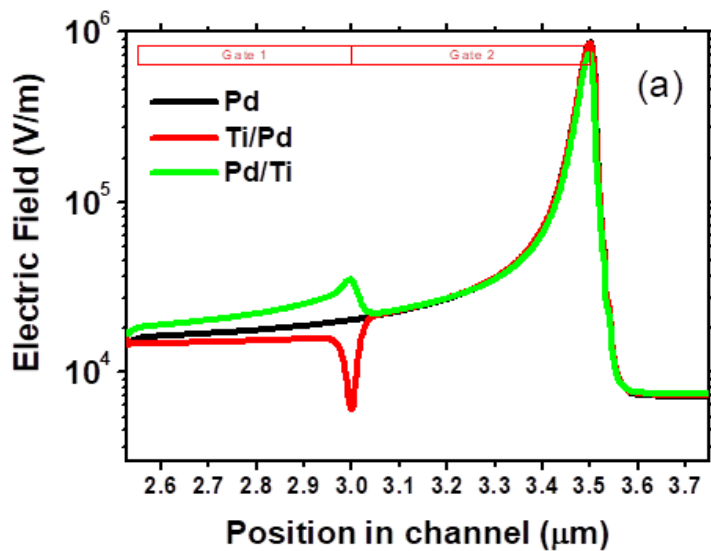


Figure 3.9 - Electrical field simulation showing the electrical field at $V_{GS}:0V$, $V_{DS}:-8V$ showing the interface spike present from a Pd/Ti metal gate device.

The Schottky barrier height of the metals is directly linked to the work function of the metals used. The metals with a larger work function leading to a larger barrier height between the two. This affects the barrier height and a simulation of the change the Gate WF can have on the conduction band energy can be seen below in figure 3.10.

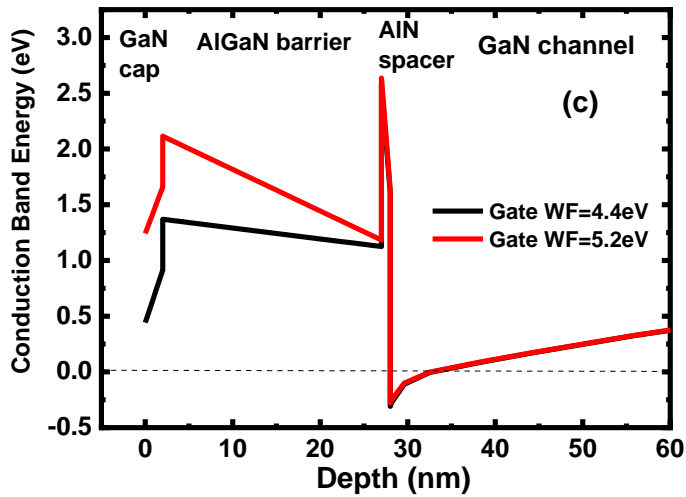


Figure 3.10: The Conduction band energy change shows between two metals with different work functions, 4.4 eV and 5.2 eV against the depth in the wafer stack.

This higher Schottky barrier height observed with Pd gate stack translates to the 2DEG channel under the gate region being depleted at a smaller V_{gs} voltage. Conversely the Ti gate stack will pinch off at a higher V_{gs} proportional to the difference in WF when compared to the Pd gate. This means that in a DMG device the Pd gate is the dominant factor in defining the devices total pinch off voltage. This work function change between the two gates explains why the peak in the interface is observed in the DMG device as the difference in effective channel ‘pinch offs’ in the two gate metals acts to spread out the total field present in under the gate region. This spreading out of the field acts in a similar manner to the function of field plates. As this spreading of the field is directly proportional to the threshold of the metals it is proportional to the Schottky barrier height of the device. This means that increasing the Schottky barrier height difference between the two metals leads to an increase in the field profile, which in turn means an increase in electron velocity and therefore transconductance. This is shown in figure 3.11.

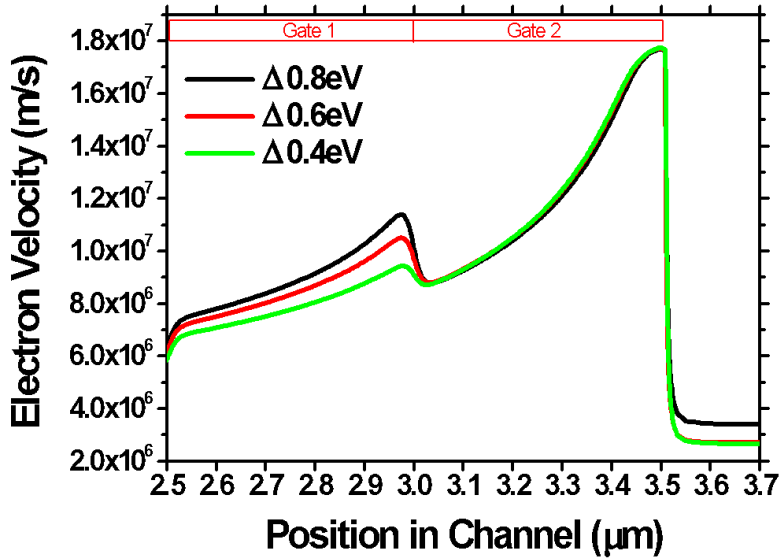


Figure 3.11 - A plot of the electron velocity profile for three differences in Work function, 0.4eV, 0.6eV and 0.8eV against the position in the channel under the gate region of the device.

Conversely swapping the order of the two metals, having the Ti with a lower EF on the source side and the Pd with a higher WF on the drain side acts to produce an ‘inverted’ peak in the electric field at the interface as shown in Figure 3.12. This leads to a decrease in the electron velocity across the gate region as shown in Figure 3.12 and hence lower transconductance in the device compared to that of the SGM devices.

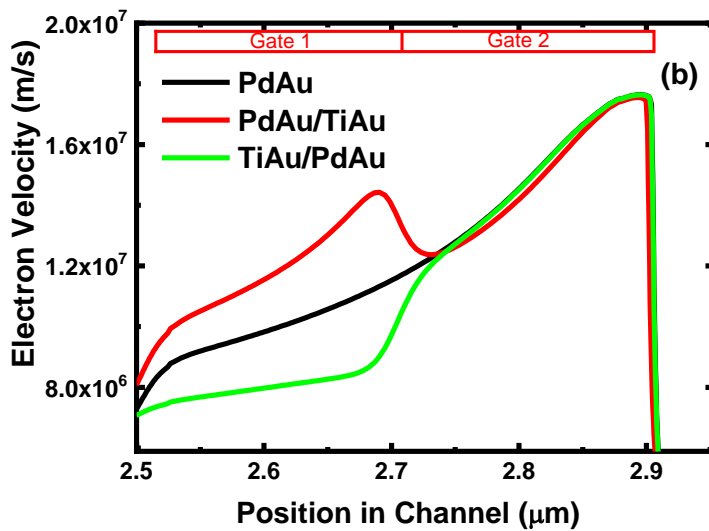


Figure 3.12 – An electron velocity plot showing DMG (PdAu/TiAu), DMG(TiAu/PdAu), and SMG (Pd), for a $V_{ds}=10V$ and $V_{gs}=0V$.

As this increase in transconductance is only directly related to the barrier thickness and Schottky barrier height, changing the gate lengths in the device should produce the same increase in transconductance that is scalable down to sub μm gate lengths. To verify this, simulations from $1\mu m$ down to $200nm$ have been performed and the results for the increase in transconductance can be seen in figure 3.8, showing a $200nm$ device and table 3.1, comparing the gate lengths.

3.3.3 Shielding effect and Drain Induced Barrier Lowering (DIBL) improvement

3.3.3.1 Experimental Results

As well as the improvement in transconductance that can be achieved with the DMG device structure a reduction in DIBL can be achieved by placing the lower WF metal on the drain side of the gate stack. The different Schottky barrier heights and therefore threshold voltages mean that each gate depletes the 2DEG in the channel at a different V_{ds} . This depletion of the 2DEG under the gate region is from the creation of a vertical E-field generated by applying a gate bias. With an increasing V_{ds} this vertical E-Field is changed in the lateral direction causing the field as a whole to move towards the drain side of the device. This lateral movement of the field causes a worse pinching off of the channel region which leads to increase threshold voltage required and an increased leakage current.

Drain induced barrier lowering is defined as the change in threshold voltage for a given change in drain source voltage¹⁶⁻¹⁸. The extraction of the DIBL is done using the following equation 3.5.

$$DIBL = \frac{V_{TH(LIN)} - V_{TH(SAT)}}{V_{DS(SAT)} - V_{DS(LIN)}} \quad 3.5$$

Where V_{ds} is the drain source voltage and V_{th} is the threshold voltage, V_{ds} is set at, $V_{DS(SAT)} = 10V$ and $V_{DS(LIN)} = 0.1V$ respectively.

Fabricated devices have been created and tested to extract the DIBL across a range of gate lengths from $1\mu m$ to $200nm$.

Gate Configuration	DIBL (mV/V)	Percentage reduction in DIBL
500nm/500nm – DMG (Ti/Pd)	12	50%
1um – SMG (Pd)	24	
300nm/300nm – DMG (Ti/Pd)	19	34%
600nm – SMG (Pd)	29	
200nm/200nm – DMG (Ti/Pd)	19	49%
400nm – SMG (Pd)	37	
100nm/100nm – DMG (Ti/Pd)	27	51%
200nm – SMG (Pd)	55	

Table 3.2 – The DIBL present in the devices with a gate width of 125um and gate lengths with a range between 1um and 200nm. The results are an average of 10 devices with IV characteristics extracted from a test setup of Vds at 0.1V and 10V, and a Vgs of -5V. The percentage reduction shows the difference between the DMG and SMG with same total gate length.

As is shown in table 3.2 the DIBL reduction in the device increases as the total gate length of the devices decreases from 50% to 34%. This is to be expected as DIBL gets worse for decreasing gate lengths and the shielding effect will become more pronounced. This scales well down to 200nm gate lengths, and the trend is expected to continue for even smaller gate lengths although further investigation would be needed.

It can be seen from these results that the reduction of DIBL is roughly 50% and remains consistent across the range of gate lengths tested in this experiment. This is an important finding as the DIBL gets increasingly worse as the gate length shrinks meaning the overall value of DIBL improvement will increase as the gate length decreases

3.3.3.2 Simulation Results

The simulations can help visualise this improvement in the DMG device and a electrostatic potential profile along the channel in Figure 3.13 shows the reduction in lateral field movement.

The DMG device has the lower WF metal on the drain side which then shields the higher work function metal from the varying drain bias.

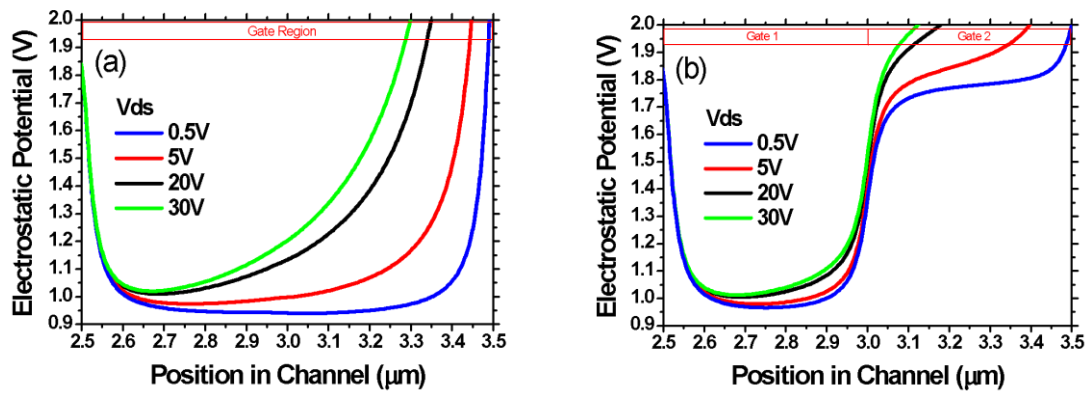


Figure 3.13 – Simulated electrostatic potential profile with varying drain bias between 0.5V to 30V at $V_{gs} = -6V$ for a) PdAu SMG and b) PdAu/TiAu DMG devices.

Figure 3.13 shows the simulated electrostatic potential profile of the SMG and DMG devices with varying drain bias. It is noted that the channel electrostatic potential is sensitive to the drain bias in the SGM devices which leads to a DIBL effect where the threshold voltage changes with drain voltage. The change in the electrostatic potential increases which is consistent with the experimental DIBL. As the gate length reduces, the change in the electrostatic potential with drain bias becomes even more prominent.

On the other hand, a two-step profile in the electrostatic potential along the channel is observed in the DMG device with the Pd gate metal with a higher WF on the source side. The potential in the Pd gate region is shielded from the varying drain bias by the lower WF metal, Ti, on the drain-side for the PdAu/TiAu DMG device. This acts to spread out the depletion region in the channel and the screening effect reduces the sensitivity of DIBL with the drain bias variation when compared to the PdAu SMG device.

3.3.4 Leakage Improvement

As well as the reduction in DIBL leading to a more stable threshold voltage it will also lead to a lower device leakage as the gate is able to better control the channel region^{19,20}. A plot of the off state electric field within the device is shown in figure 3.14 below. The second spike can be seen at the gate interface as well as a lower maximum field at the drain edge of the device. These two features of the modified electric field lead to a device that is able to better control the channel region.

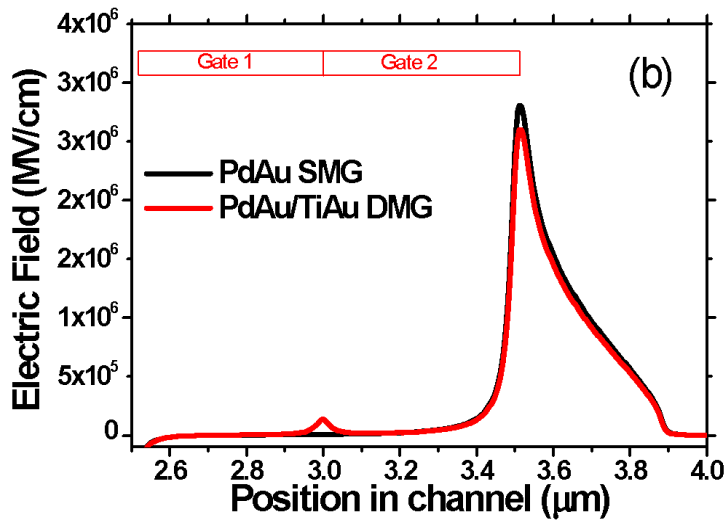


Figure 3.14 – The simulated off state electric field profile within the device. $V_{ds} = 10V$ and $V_{gs} = -6V$

This leads to a lower gate leakage current within the device, shown in figure 3.15. At lower values of drain source voltage, the leakage current is reduced by almost an order of magnitude but this reduces significantly at higher V_{ds} values. Even so, as a typical device is gate leakage dominant any reduction in leakage will contribute to better device performance and reduced losses. This reduction in gate leakage comes from a physical effect in the device which is analogous to having a field plate. With a field plate at the drain edge of the device the peak E-Field is lowered and shared between the region under the edge of the field plate and the edge of the drain. This spreading out of the E-Field helps reduce leakage within the device. The DMG device functions in a similar way with the peak E-Field spreading across both the drain edge of the device and at the intersection between the two metals. This helps reduce leakage through the gate of the device and the overall device leakage current.

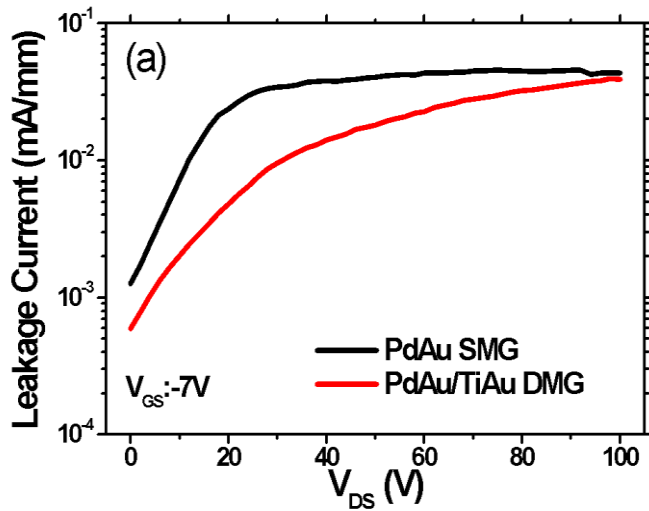


Figure 3.15 - Off-state gate leakage current comparison between SMG and DMG HEMTs. $V_{ds} = 10V$ and $V_{gs} = -6V$

As well as a decrease in gate leakage the device structure provides the potential for very small gate lengths that would otherwise not be able to pinch off the channel once the DIBL becomes too high. Once the gate length becomes too small, the gate cannot pinch off the channel region and leakage currents become too high for the device to operate as a transistor. This reduction in DIBL means the leakage current will become low enough to allow smaller and smaller gate lengths. This manifests itself as drain-source leakage current during the transistor off state. Figure 3.16 a shows the DMG structure and shows how the leakage current is gate leakage dominated as the gate leakage current level is equal to the drain leakage current. The separation between the gate leakage and drain leakage in figure b means the device leakage currents will be source dominated. This is because of the inability of the SMG device to fully deplete the channel due to the DIBL. This additional mechanism of reducing leakage only presents itself in devices with gate lengths sub 500nm and the DMG provides a way to improve the leakage current.

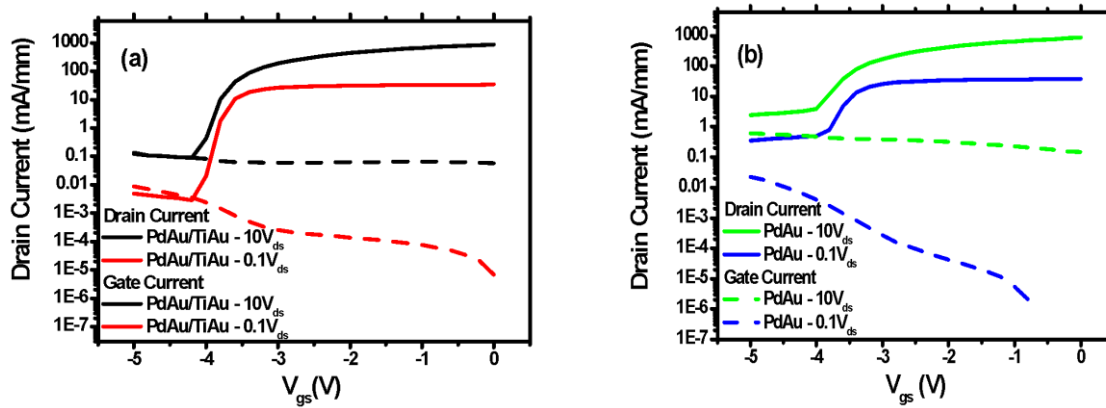


Figure 3.16 a and b - Gate transfer characteristics of the PdAu/TiAu and PdAu, DMG and SMG devices with a gate width of 125 μ m and gate lengths of 200nm. The results are extracted using a test setup of V_{ds} at 0.1V and 10V, and a V_{gs} of -5V.

3.4 Conclusion

In summary, the DMG AlGaIn/GaN HEMTs has been demonstrated provides several advantages over the conventional SMG configuration typically used in AlGaIn/GaN HEMTs. The improvements in transconductance and the improvements in DIBL have been observed at a range of decreasing gate lengths.

The advantage in peak transconductance has been demonstrated to be between 5-8% and output characteristic plots of the devices show a slight improvement in R_{on} and output current. As well as this, the transconductance improvement has been shown to be at a similar level to SMG devices with a total gate length half the value of the DMG total gate length. An explanation of this improvement based on the altered electric field under the gate region has been explained and backed up with simulated results.

The main advantage of this device structure however is the large reductions in device DIBL that are present. Consistent reductions shown across gate lengths from 1 μ m to 200nm up to a 50% reduction down to a gate length of 200nm have been demonstrated. This combined with the improvement in transconductance demonstrates the advantage this device configuration can bring. As well as this, leakage current reductions particularly at small gate lengths where the DIBL effect may prevent a proper pinch off in the devices have been demonstrated. An explanation of how this improvement in DIBL has been given, the shielding effect the second gate metal is presented to be the method that gives rise to the improvement.

This has demonstrated that even for the smallest gate lengths that are able to be fabricated creating a DMG structure instead of a SMG device can provide advantages with an equal transconductance and a largely improved DIBL and in turn leakage current. This means that although the fabrication method does require an increased complexity in the form of aligning the second gate metal to the first, it is advantageous to produce the DMG structure to give a device with double the smallest possible gate length that is able to be fabricated. For example, fabricating a 200nm DMG device instead of a 100nm SMG device will provide the peak transconductance similar to the 100nm device with a largely improved DIBL.

Further research into this device structure could be in the form of investigating how the gate length ratio will affect the gm improvement and the DIBL. Changing the DMG structure to have both a longer and shorter higher work function metal may provide a different range of advantages that could be tailored for specific applications.

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Chapter 4 - AlGaN/GaN Based Monolithically Integrated Buck Converters

4.1 Introduction

Monolithically integrating a buck converter system completely made on a GaN epitaxial will lead to a higher efficiency system that functions at high voltages and frequencies when compared to other semiconductor materials. Shinjo et al have already demonstrated the suitability of this and achieved high efficiencies of 64% at 300MHz¹. Building on this system, and further improving this efficiency will be the main aim of this chapter and also providing the efficiencies of the standard converter for comparison with more complex circuit schematics. No work has directly compared the standard, three and five level integrated buck converters when fabricated simultaneously. By doing this a greater understanding of the system and how further improvements can be achieved reducing power wastage.

This chapter will outline the basic fabrication process followed by experimental results gathered at a range of input voltages and frequencies. Breakdowns of component losses as well as overall efficiencies for the converter are provided. Following this, simulations have been provided to outline the ideal efficiencies that the systems could possibly provide and comparisons of these with the experimental results. Discrepancies between the simulation results and the experimental results have been quantified and explanations for this have been explored.

Following this an investigation into the field plate within the devices has been explored and simulations of different field plate types when integrated into a buck converter have been investigated. A breakdown of the physical mechanism that give rise to the differing effects of each field plate have been examined from a device level through to total efficiency simulations of buck converters.

4.2 Operating Principles

A buck converter is a DC-DC converter that steps down the voltage between the input and output of the circuit². The circuit makes use of a pair of switches, a transistor that switches connecting and disconnecting the input power, at a high speed followed by an inductor and capacitor that act as a filter. This smooths the output waveform to a predetermined level that can be used as a DC signal. There are two main types of single level buck converter, asynchronous and asynchronous buck converter.

The asynchronous buck converter³ uses a diode to free wheel the circuit when the high side transistor is switched off. The basic circuit diagram of an asynchronous buck converter can be seen in figure 4.1.

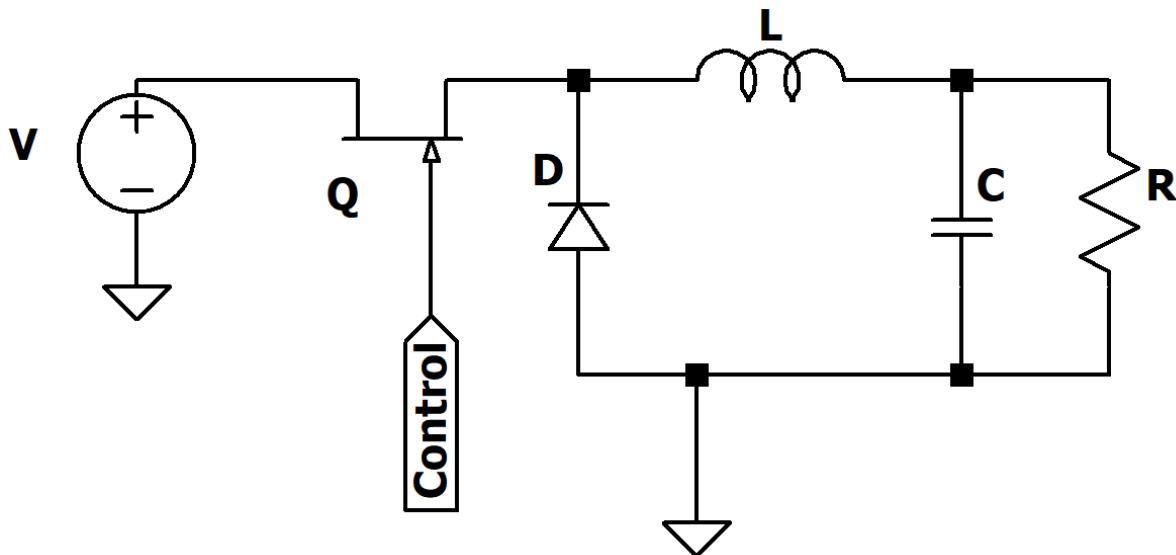


Figure 4.1 - A basic circuit schematic of a standard asynchronous buck converter

As only one transistor in this configuration is switching the control circuitry for this schematic is significantly simpler than a synchronous buck converter. However, as a synchronous buck converter takes advantage of using two transistors for switching, the typically lower on-state resistance between the drain and source (R_{dson}), of the low side transistor is typically more efficient than using a diode. This synchronous buck converter schematic is the configuration that will be used for the envelop tracking system where efficiency is key so the lower on state losses of the low side transistor will provide a more efficient choice than an asynchronous buck converter. The basic schematic for this circuit is shown in figure 4.2.

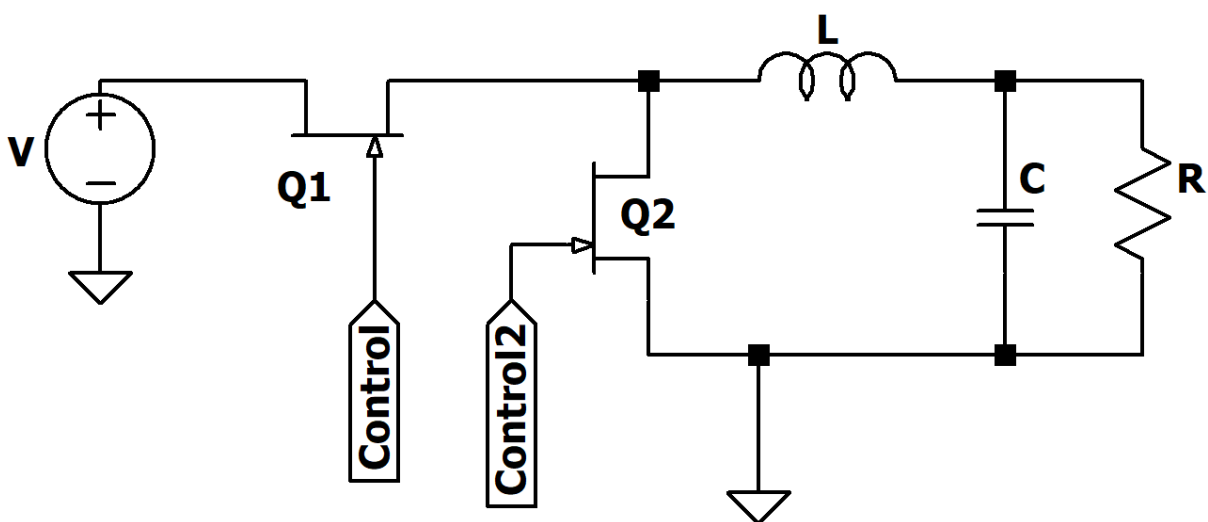


Figure 4.2 – A basic circuit schematic showing a standard synchronous buck converter.

The basic operation of a synchronous converter is as follows and a current breakdown of each component is shown in figure 4.3. When Q1, the high side transistor, is switched on the allows current flow through to the switching node. This allows current flow through the inductor L enabling it to store energy, charge the capacitor C and allow current flow through the load resistor R. This leads to the load seeing a steadily increasing output current as the components charge up. During this time Q2, the low side transistor, will be switched off.

When Q1 is switched off the input current falls close to zero, only leakage current through Q1 flows into the circuit. Q2 is then switched on and the inductor will resist the change in current and adjust the voltage to try to maintain a constant current. The inductor current flows through the load as it steadily decreases and at the same time the capacitor will also discharge through the load. As the stored energy depletes the output current will slowly decrease, this is see in the load ripple current displayed in figure 4.3.

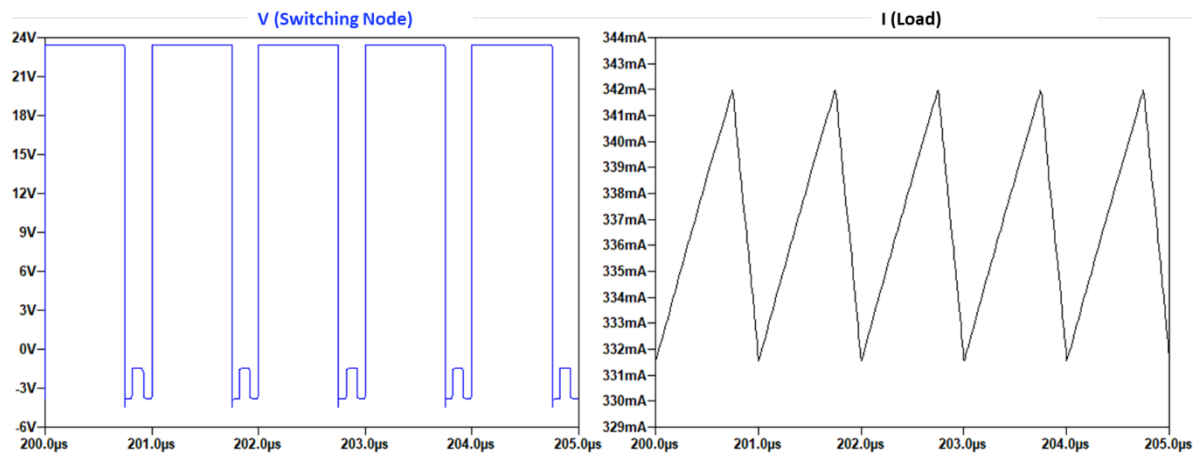


Figure 4.3 - A breakdown of the voltage, or current, in each component in the buck converter.

A key factor to consider when operating the synchronous buck converter is that the two transistors must not be on at the same time. If this occurs, it can lead to effectively as short circuit between the input and ground and cause high power through the devices leading them to breakdown. Due to this the slew rate of the transistors must be considered to ensure that no overlap occurs. The slew rate is given by the rate of voltage change per unit time and will be a key factor to consider when operating at high speed as this system will be.

The output voltage of the buck converter is directly tied to the duty cycle of the high side transistors switching. The equation to summarise this is as follows in equation^{4.5} 4.1.

$$V_{out} = D * V_{in} * \eta \quad 4.1$$

Where V_{out} is the output voltage, V_{in} is the input voltage, D is the duty cycle and η is the efficiency of the converter. Another challenge of the buck converter when designing for a specific output voltage is

to ensure that the system accounts for the efficiency of the converter when operating at a specific duty cycle as the efficiency will change across the range of output powers the converter can output.

Another important consideration when designing the converter for maximum efficiency is the output filter components and values used. The capacitor and inductor determine the output ripple voltage/current the load in the circuit will see. The value of these components is determined by deciding on an absolute maximum size for the ripple value, which gives rise to a minimum component value that will accommodate this. Equation 4.2 to determine the inductor size is as follows:

$$L = \frac{(V_{in}-V_{out})*D}{f_s*\Delta I*V_{in}} \quad 4.2$$

Where ΔI is the ripple current through the inductor, f_s is the switching frequency, D is the duty cycle and L is the inductor value. This give the minimum inductor size that should be chosen to achieve a given ripple voltage although larger values of inductor can be chosen further minimise the ripple size. The capacitor is calculated from the following equation 4.3:

$$C = \frac{\Delta I}{f_s*8*\Delta V_{out}} \quad 4.3$$

Again this is a minimum capacitor value that should be selected.

4.3 Gate Driver Operation

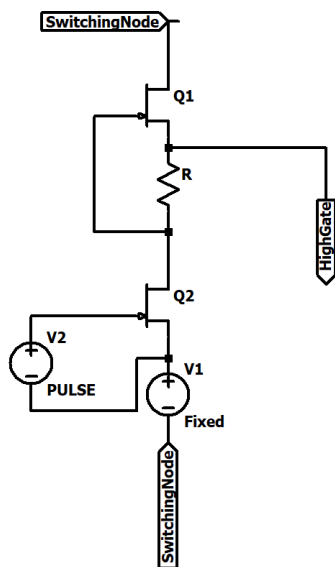


Figure 4.5: The active pull-up gate driver used in the integrated buck converter that feeds into the gate of the power transistors.

The gate driver schematic can be seen in figure 4.5. And consists of two transistors and resistor connected to both a pulsing signal and fixed DC signal which is used to switch the power transistor. The gate driver is a variation on an active pull-up driver and is required to provide enough current to the gate of the power transistors, to ensure high switching frequency⁶. This is required to charge C_{gd} , the miller capacitance, fast enough such that it does not limit the switching frequency. The integrating of two transistors into each pull-up driver provides lower losses when compared to simply using one transistor and a resistor, due mainly to the lower DC losses thanks to lower leakage through the transistor. The low side gate driver is connected to ground and the high side connected to the switching node. This is to ensure that the power transistor is placed under the correct V_{gs} as the switching node, the source of the transistor will operate between 0V and the input voltage. The gate driving transistors are smaller than the power transistors and have a gate width of 25 μ m compared to the power transistors 1mm. This should provide enough current to the gate of the power transistors, around 25mA, to prevent the C_{gs} being the limiting factor in the device charging.

The digitally isolated gate switching signal is fed into the gate of J1 in the bottom section of the gate driver, this is switching between 0 to -5V referenced to the source of the transistor. The source of the transistor is fed with a fixed DC -5V. This provides a total switching voltage to the transistor of -5V, greater than the -3.5 V_{th} given by the design requirements for the device ensuring it is fully switched off minimising the leakage current. This operation means the transistor switches with operating polarity to the voltage seen by the power transistor, then the low side of the gate driver is off the power transistor will be turned on, and vice versa.

The operating principle of the driver is the same for the high side power transistor but with it taking a reference voltage from the switching node, between 0V and the input voltage. The source of the power transistor is connected to this switching node to ensure a V_{gs} swing of 5V is provided, effectively a 5V swing in addition to the switching node voltage. The gate driver can be made with the fabrication considerations that any component within it will only ever see at maximum a 5V swing. Although the reference voltage used within it is the input voltage of the circuit each component only will have to switch the 5V needed for the gate voltage of the power transistor. This means each component can be made much smaller than the power transistors and only be made to withstand a lower current and breakdown voltage, saving space within the circuit.

4.4 Efficiency and Losses

Previously demonstrated work that reports efficiencies up to 74% do not include an integrated gate driver and only report the efficiency of the power switching. Including a gate driver with this circuit schematic will also increase the system power losses compared to the previous work which excludes this from their estimations, although this tends to be much lower than the power transistor losses especially when looking at a high power system. The power losses can be broken down into three main areas, the on-state power transistor losses, off-state losses and gate driver losses.

Typically, buck converters designed for high voltage operation have a lower efficiency at lower voltages due to switching losses within the circuit dominating the total system losses. This is due to switching power losses remaining fairly constant throughout the range of operating output voltages. This means at lower output powers they make up a higher proportion of the total losses. The efficiency tends to increase at higher output powers as the switching loss proportion decreases and the on-state losses increase, although the R_{Dson} of GaN devices is low compared to silicon devices so this tends to be a small value.

The on-state losses in the system and the power lost through the transistors depend on its R_{Dson} and the duty cycle in the system, i.e. the amount of time the transistor remains ‘on’ for. The on-state losses are independent of the switching frequency meaning that these losses will remain constant as the system switches at higher frequencies.

The on-state losses in the system can be calculated as follows in equation 4.4, and this applies to both the high side and low side transistors.

$$P_{onstate} = I_{switch}^2 * R_{Dson} \quad 4.4$$

Where $P_{onstate}$ is the on state losses, I_{DS}^2 is the drain source current through the power transistors and R_{Dson} is the on state resistance of the transistors. As these circuit losses are dependent on R_{Dson} of the power transistors, the design of these is very important and minimising the R_{Dson} of the transistor is key. Typically for a GaN HEMT with a gate width of 1mm that will be talked about in this paper 3-4mOhm. Although the on state losses are not directly tied to switching frequency, the transistor design and the effects that dynamic R_{on} can present must be considered. As discussed in chapter 1 section 1.3.3, if the transistor has a poor dynamic R_{on} effect this can lead to a largely increased R_{Dson} in the transistors which increases the on-state losses at higher frequencies.

The switching losses in the system are the frequency dependant losses in the system and are power that is lost through the power transistors during the switching transients. These depend on the transistor slew

rate and slew rate of the switching signals fed to the gate driver and that come from the gate driver to the gates of the power transistors. As the duty cycle determines the output power of the system as a whole these losses remain fairly constant across the output power range of the system. They can be calculated as follows in equation 4.5:

$$P_{switch} = \frac{1}{2}V_{in}I_{out}(T_{rise} + T_{fall})f_{sw} \quad 4.5$$

Where V_{in} is the input voltage, I_{out} is the output current, T_{rise} and T_{fall} are the voltage rise and fall times taken to switch the transistors from on to off state and vice versa, and f_{sw} is the switching frequency.

The other losses caused by the active components in the system are the gate driver losses. These typically remain consistent across a range of output powers as the gate voltages and supply voltages needed to switch the power transistors remain constant. The main issue with quantifying these results is the only source of measurement comes from the digital isolator in the testing PCB. This has a fixed current draw regardless of whether the circuit is operating or not so quantifying the magnitude of the gate driver losses in the experimental data is not possible. As such the results presented experimentally will with a fixed gate driver loss value.

The remainder of the losses in the circuit come from the passive components, the inductor and capacitor used as the filter for the switched power signal. The inductor is an external component and not integrated into the monolithically integrated system as well the capacitors. The inductors used are coil wound high frequency inductors with the series resistance as per the manufacturer's specification used to estimate their losses. The capacitors manufacturers resistances are very low at 0.05Ω so will be ignored in the loss breakdown.

4.5 Fabrications

The fabrication of the monolithically integrated buck converter uses the same processes as outline in chapter 2, section 2.2 although there are more steps involved in fabrication and some steps do differ from the basic device fabrications. The fabrication was performed on a 35mmx35mm diced piece from 6-inch GaN wafer that contains several different steps. Initially the mesa isolation and ohmic deposition are identical to the previously outlined steps. This is then followed by Schottky metal (Ni/Au) deposition for the Schottky diodes. The next stage is the gate metal deposition. This follows the EBL step to define the gate region with a length of 250nm using the dual layer resist, PMGI and PMMA 1:1. A metal stack of 30nm/80nm Ni/Au is then deposited onto the sample. Following this is a PECVD deposition of SiN_x with a thickness of 80nm. A via etch is then performed using RIE to access the source ohmic pads on the device to allow the source connected field plate metal deposition. A 40/200nm Ni/Au metal

stack is deposited for both the source field plates on the device and also the bottom metal used in the Metal-Insulator-Metal (MIM) capacitors. Following this a thick SiN_x deposition is performed to act as the insulator between the two MIM plates

Further metal deposition is then performed to deposit the top capacitor plates, with a 40nm/200nm Ni/Au stack. The next step is a 250nmSiN passivation to aid the capacitors in having a higher breakdown voltage. This is done with the extra layer of passivation ensuring the bond pad tracks that connects the capacitors together has a thicker passivation between it and the edge of the capacitor top plate. Again, it is aimed for around 200nm of SiN_x in this step. A via opening is etched using the RIE to access the top layer of the MIM capacitors and the source, drain and gate terminals of the transistors. This is followed by the bond pad and interconnect patterning and deposition, as this is carrying the current across the device a thicker deposition is necessary to ensure the interconnect resistance doesn't limit the current. Two separate depositions of 60/400nm Ni/Au and 400nm Au are evaporated for a total of over 800nm of metal interconnect. The final steps of the process are required to connect the source pads of the large area devices. After the bond pad step, a thick layer of PECVD SiN_x, 1µm, is deposited using the PECVD. This is then etched through and the connect between the source pads and the interconnect is then patterned and evaporated on the sample with a thickness of 40/400nm Ni/Au.

4.6 Fabricated Buck Converter

The single level buck converter complete with gate driver and capacitors integrated into is can be seen below in figure 4.6.

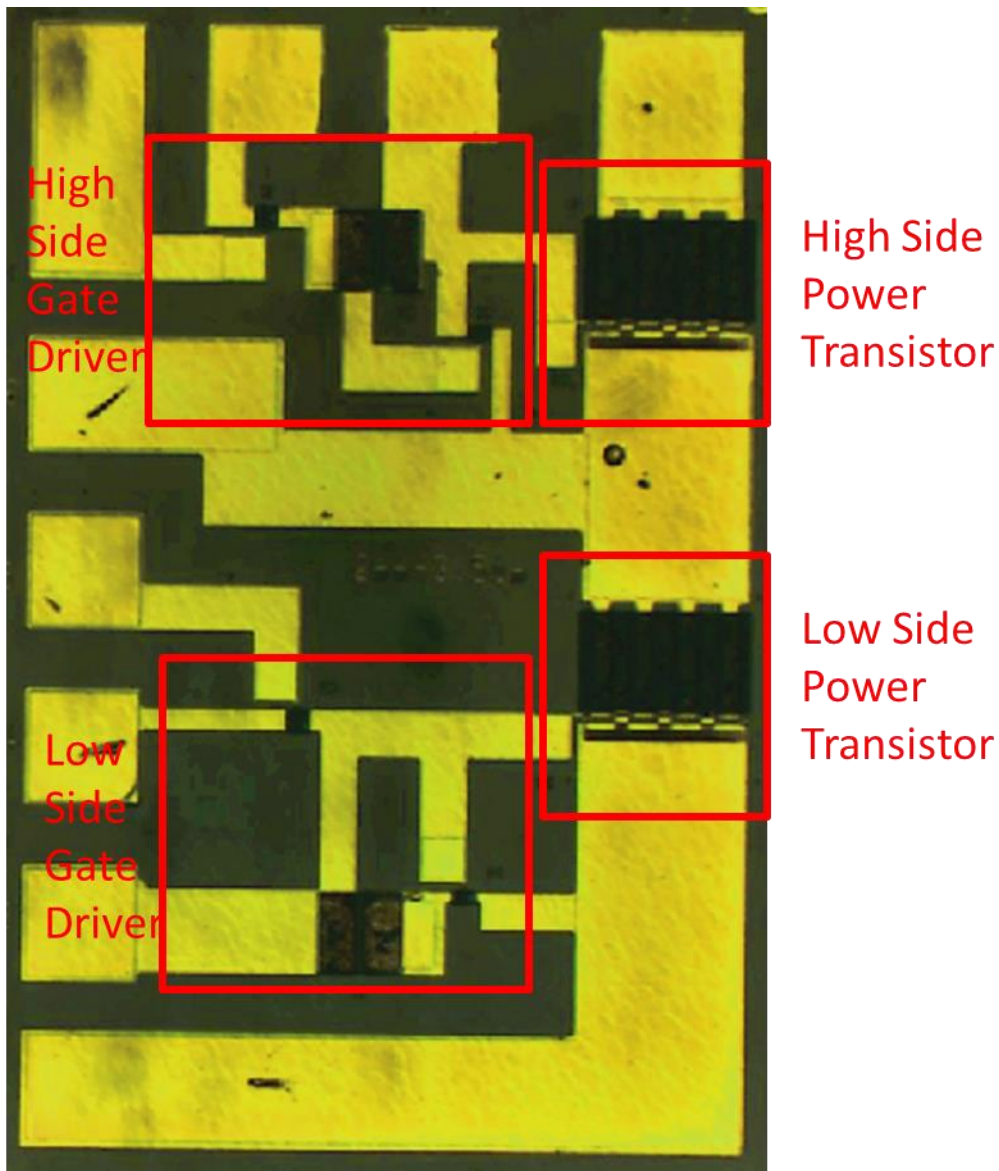


Figure 4.6: A picture of a fabricated buck converter showing the high side and low side sections of the circuit.

4.6.1 Power Transistors

The power transistor configuration for the buck converter are 1mm devices with 8 fingers all with a width of 125um. This gives an on state resistance of between 3-4mOhm when tested in DC conditions and can be expected to conduct 1A of current. This was extracted from an IV curve with a V_{ds} of 1V. This can be seen in figure 4.7.

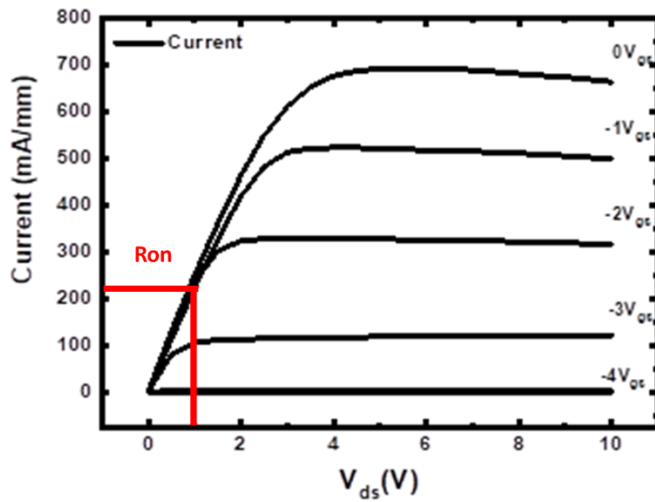


Figure 4.7: The IV plot used to extract a typical 1mm gate width device, the R_{on} value is extracted at a V_{gs} of 0V and V_{ds} of 1V.

Considerations have also been made for the device's performance at high frequency particularly in regard to reducing the dynamic R_{on} effect that presents in GaN HEMT devices. The addition of a field plate extending into the drain source region $1\mu\text{m}$ from the gate of the device can help reduce the dynamic R_{on} effect. The source field plate is placed above the channel region on approximately 80nm of SiN passivation. This field plate acts to spread out the peak electric field in the drain-side gate regions which leads to lower dynamic R_{on} when the device is stressed with a large V_{ds} . Figure 4.8 shows a comparison between a device with no field plate and a source and gate field plate. Without a field plate the R_{on} will increase by as much as 200% for a stress voltage of 50V ^{7,8}.

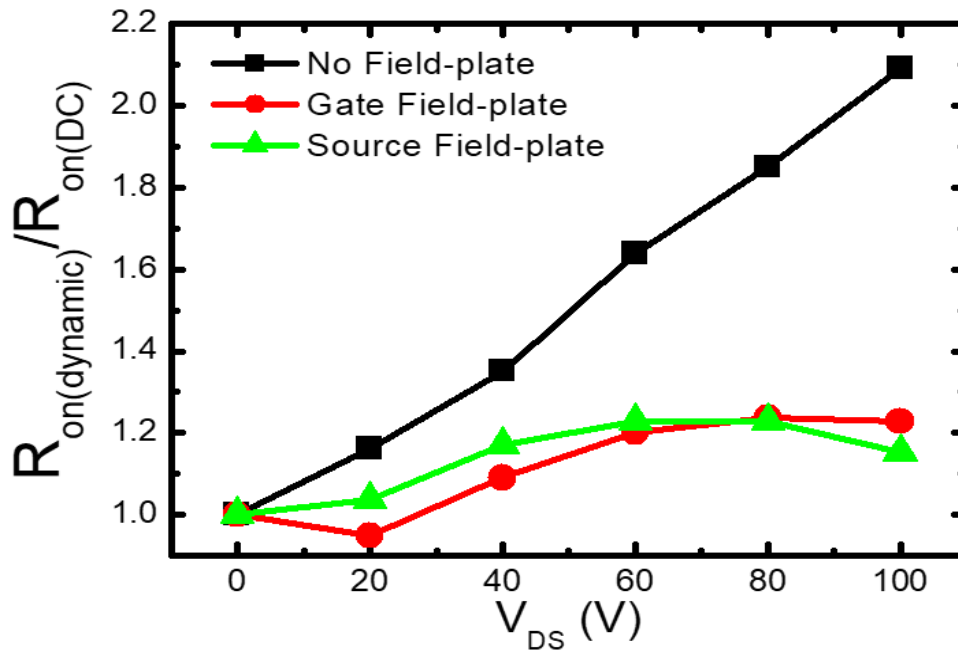


Figure 4.8: A dynamic R_{on} comparison between a device with no field plate, a source field plate and a gate field plate.

As mentioned previously the smaller devices used in the gate driver circuits are 25 μ m width devices that can deliver at least 25mA of current. They also contain the source field plates used to reduce the dynamic R_{on} effects.

4.6.2 Capacitors

The input and output capacitors present in the buck converter are MIM structures consisting of two gold pads with a SiN passivation deposited in between^{9,10}. The thickness of the passivation is approximately 200nm and should withstand breakdown voltages up to 100V. The target capacitance for the input capacitor is 350pF and the target capacitance for the output capacitor is 50pF. Some initial results for the capacitor values are presented below in Table 4.1.

	Target (50 MHz Design)	Achieved
<u>On-Chip Capacitors</u>		
C_{in}	257 pF	214 pF
C_{out}	41 pF	41 pF
C_{in} (gate driver)	50 pF	52 pF

Table 4.1: A Table presenting the measured capacitance from the MIM structure input and output capacitors on the monolithically integrated buck converters.

As well as this performance of the capacitors up to 100V has been measured and show a consistent leakage current up to a high voltage¹¹, this is presented below in figure 4.9.

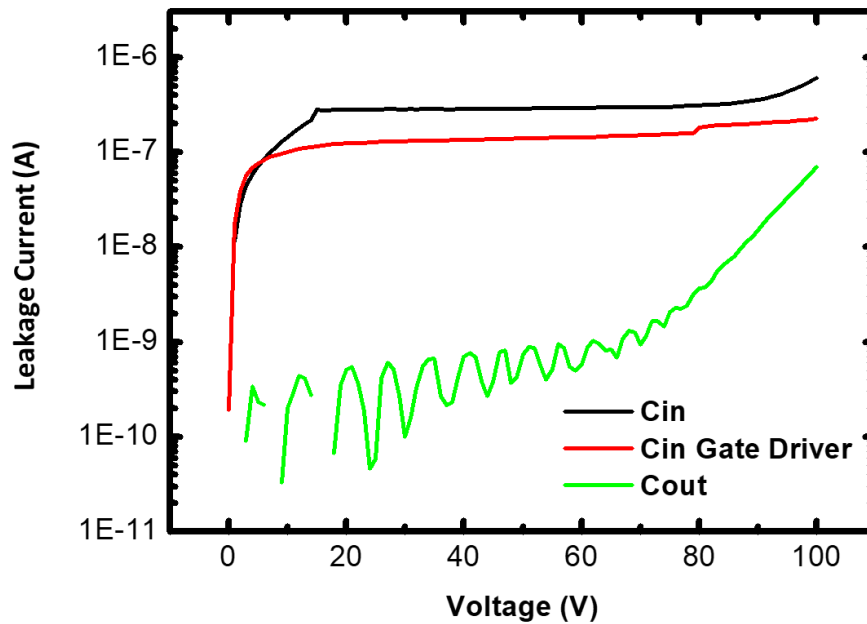


Figure 4.9: The leakage current in the input and output capacitors measured up to 100V

While the experimental capacitance measurements are very close to the calculated targets and should correctly, the main problem during fabrication was the yield of the MIM capacitors. Some of the on-chip capacitors in the integrated buck converter circuit show a short-circuit behaviour. This presents an issue for the functionality of the buck converters. To ensure the fabricated buck converter integrated circuits can be tested, it was decided that external capacitors (rated at 100V) would be used in place of the on-chip capacitors.

4.7 Bonding and packaging

The devices once fabricated are placed in packaging and gold wire bonded¹² to connections that lead externally out of the packaging. This allows the circuit to be soldered onto the PCB testing circuits. The packaging used for the circuits is a 28-pin gold plated CQFN package, LCC02834. This is done by first sawing each of the separate circuits out from the 35x35mm sample. Each circuit is then attached to the package using either solder or gold epoxy. The

chips are placed close to the centre of the packaging to minimise the parasitic effects from the bond wires that may affect device performance. An example of the bonded device in the packaging is shown in figure 4.10.

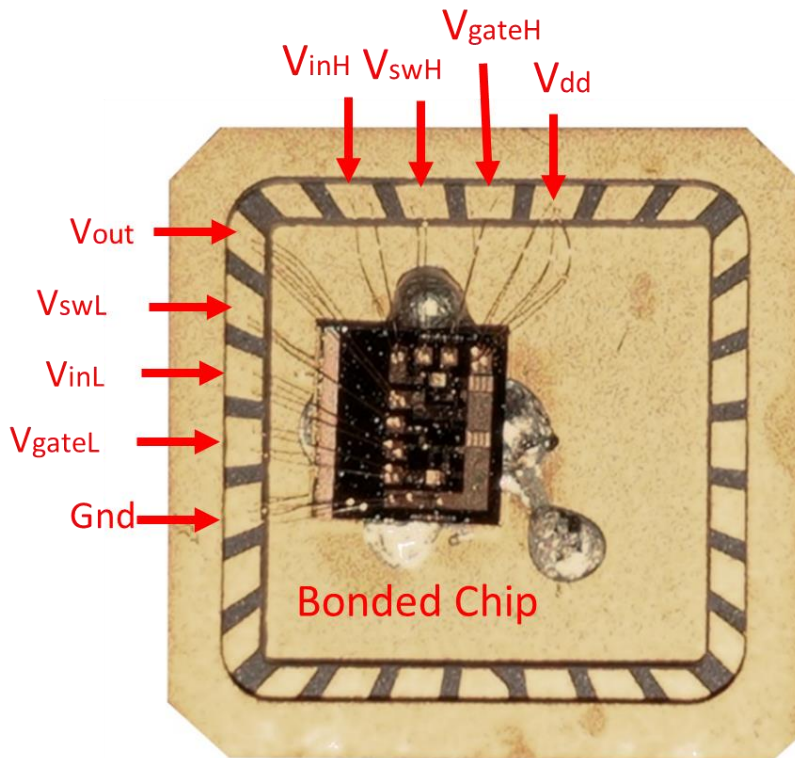


Figure 4.10: A bonded chip in the CQFN package. Showing the connections to various pads on the buck converter. $V_{in,H/L}$ is the fixed input voltage to the gate driver, $V_{sw,H/L}$ is the switching voltage fed to the gate driver. $V_{gate,H/L}$ are the high and low side power transistor gate pads, V_{dd} is the input voltage to the buck converter and Gnd is the ground connection.

The thermal characteristics of the packaging are not ideal as the bottom of the packaging does not have a thermal connection to the bottom so the addition of a heat sink would not remove any more heat efficiently. This excess heating will cause worsened device performance so further investigation into improved packages may be necessary.

4.8 Input Pulse Signal Generation

4.8.1 – 1MHz pulse signal generation

The input pulse signal generation for 1MHz switching frequency was done using a Rigol DG4162 high speed signal generator. The turn on and turn off speed of this signal is

approximately 2ns. This is low enough to only have a very small impact on the switching time in the circuit and as such the efficiency as the slew rate is less than 1% of the signal period. This signal is then fed through the digital isolator which subsequently to the gate driver in the converter circuit as shown in figure 4.11.

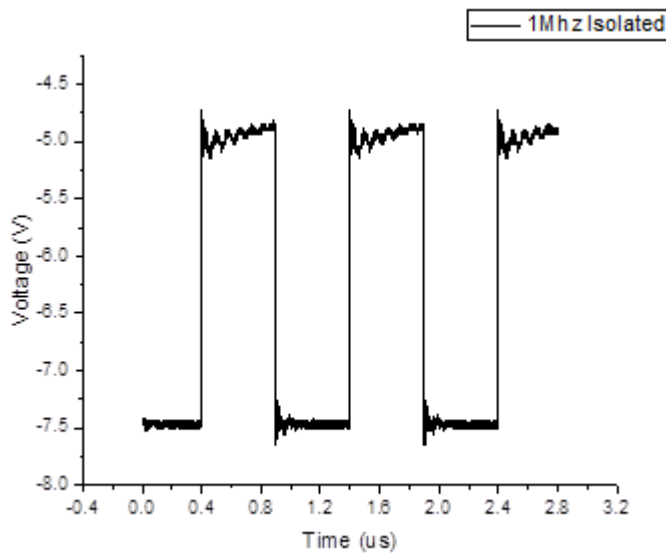


Figure 4.11: The output signal from the digital isolator fed into the gate driver of the buck converter circuit.

4.8.2 – 50MHz input signal generation using a Field Programmable Gate Array (FPGA)

The signal generated and fed into the testing circuits is created from an FPGA. The intel Stratix V is the FPGA that was chosen to deliver high frequency switching signals to the system. Internal clocks in the device operate in excess of 600MHz so the system producing switching signals at 50MHz should be within the scope of the system. The FPGA is programming using Quartus prime software which has internal Phase Locked Loop (PLL) controllers that can be used to adjust the signals from the clock into digital output signals that will be able to switch the digital isolator and in turn gate driver. One of the internal Ips is a PLL that can be used to configure the clock signals to output at a specific frequency, duty cycle and phase shift the signal. This is key to allow two separate signals to be generated that will not overlap with each other, causing the circuit to short to ground. The output signals from the FPGA are from 0-2.5V, with approximately 16mA of output current which when fed into the digital isolator are large enough to allow the output from the isolator to produce a 5V swing.

The signals however are not perfect digital signals and at increasing frequencies do have poor rise and fall times. At 50MHz the rise and fall times of the signal are approximately 5ns and

the peak voltage of the signal also fluctuates between 2.5 and 3.3V, although operation within the circuit only requires 2.3V to function correctly. The example output signal at 50MHz 50% duty cycle can be seen in figure 4.12.

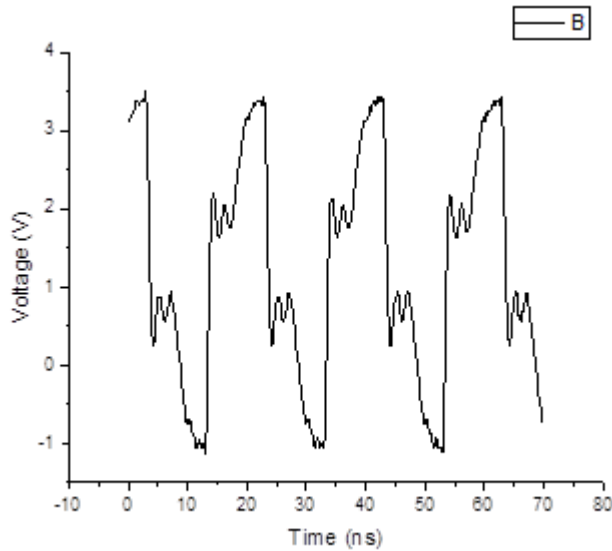


Figure 4.12: The 50MHz output signal from the FPGA with a 50% duty cycle

The rise and fall times will determine the maximum frequency the circuit could operate at. This increased switching time also means that an increased dead time between the switching signals is required to ensure there is no overlap in switching cycles.

4.9 Testing Circuits

The testing circuit for the buck converter uses an ISO7760 digital isolator that under testing conditions can effectively pass-through signals up to 80MHz. The operation of the isolator relies on a 2.5V swing on the input to generate the output 5V swing from -7V to -12V. This provides a large enough gate voltage swing to switch the power transistors from off state, $V_{GS}:-5V$, to on state, $V_{GS}:0V$. The GaN epitaxial in this study have a threshold voltage up to -4V. The single level testing circuit can be seen below in figure 4.13.

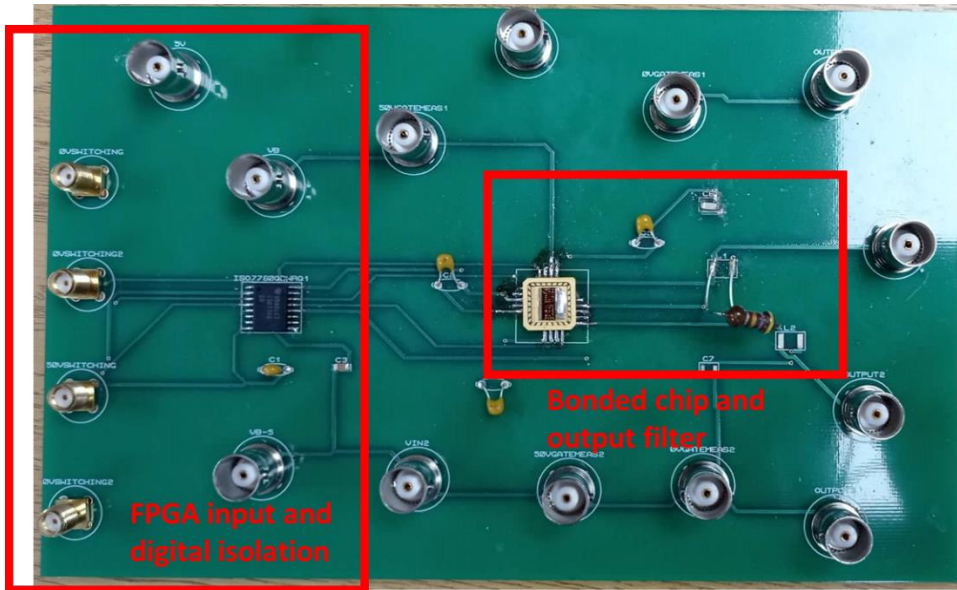


Figure 4.13: The PCB used for testing the single level buck converters.

This isolated signal is used in conjunction with the fixed -7V DC signal to switch the gate drive. An example of the switching signal measured from the output of the digital isolator at 50MHz is shown below in figure 4.14.

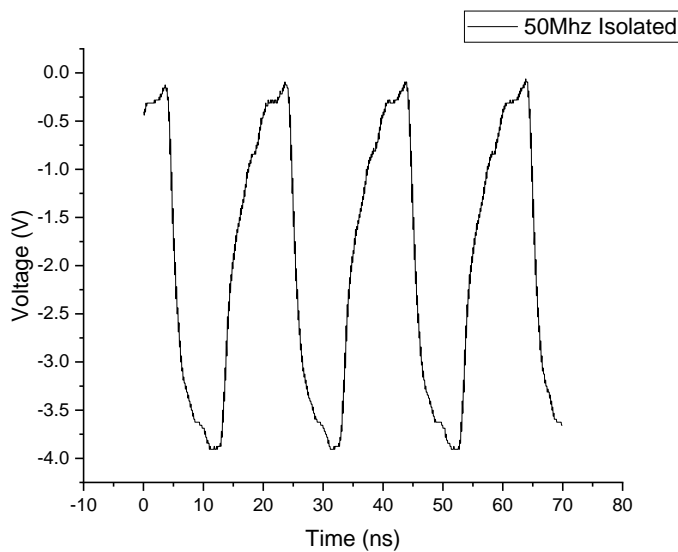


Figure 4.14: The digitally isolated gate driving signal measured at 50MHz.

The rise and fall time of this signal are approximately, 5ns. This is substantially higher than would be ideal. The rise and fall times combined account for 50% of the total switching signal which is very poor and will lead to increased losses. Slew rates that are a very low percentage of the total period are needed for efficient switching particularly when the signals are slow at

the point of generation. The increased slew rate in this case is due to poor signal generation from the FPGA and occurs as the speed of signal generation increases.

4.10 Experimental Setup

Once bonded and soldered into the testing PCB a number of signal generators, oscilloscopes and DC power supplies are used in the circuit testing. Two fixed DC signals are fed into the testing circuit to provide the 5V swing needed to switch the power transistors. These are set to -5V and -10V in order for the biasing voltage fed through to the power transistor to switch it to be -5V. 5V is supplied to power the digital isolator and then the input switching signals are fed into the circuit. A high speed 20GHz oscilloscope is used to take all the measurements alongside high speed probes rated for 600MHz.

An example of a circuit being tested is shown in figure 4.15.

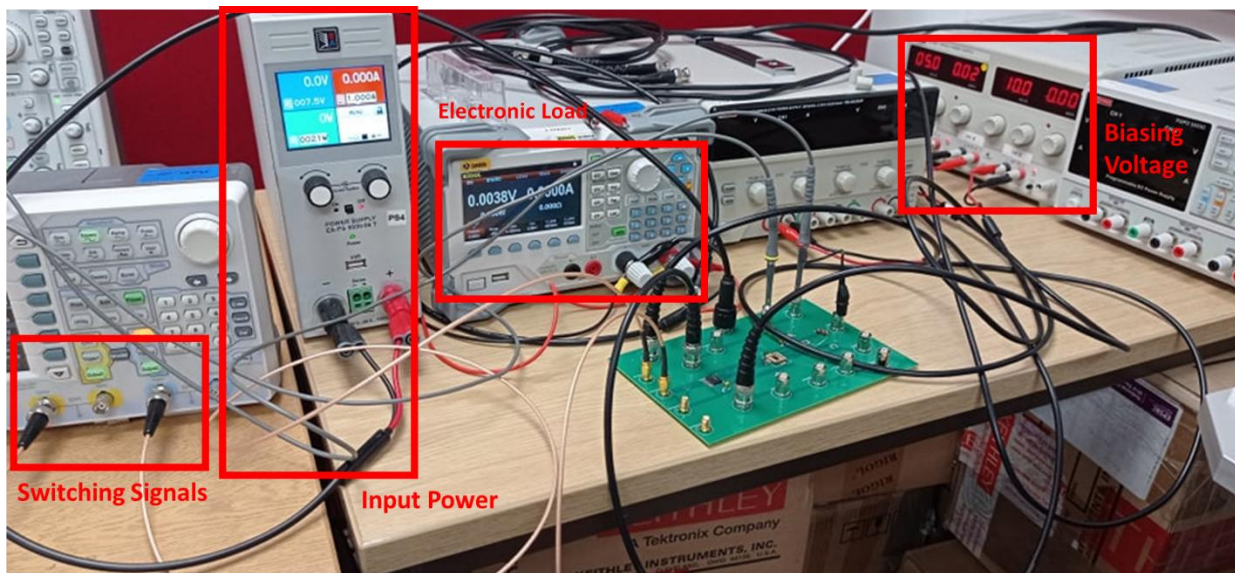


Figure 4.15: A photo of the testing circuit connected to the power supplies mid testing.

The collection of the experimental results was performed in two main stages. First low voltage measurements were taken, the input voltage set to 10V. This ensures that the voltage is low enough to not damage any components if shorts in the circuits appear. To do this a fixed DC power supply is used to generate the 10V and also to monitor the current and total power that is applied to the circuit. An electronic load is then connected to the output terminal of the testing circuit and set to a fixed resistance of 50ohms. This also measures the output voltage, current and power to allow accurate extraction of the efficiency of the circuit under test conditions.

4.11 Experimental Results

4.11.1 1MHz 10V Operation

The first testing of the integrated buck converters was at input voltage of 10V with a 1MHz input signal frequency with a varying duty cycle from 20% to 75%. The 1MHz input signal generation is as described in Section 4.8 was fed into the integrated gate drivers in the buck converter. The output signals of the gate driver which are fed into the gate of the power transistors is shown in Figure 4.16. The turn on and turn off times of the output signal from the gate driver are the same as the output signal from the digital isolator. This shows no degradation in the signal slew rate is introduced by the gate driver.

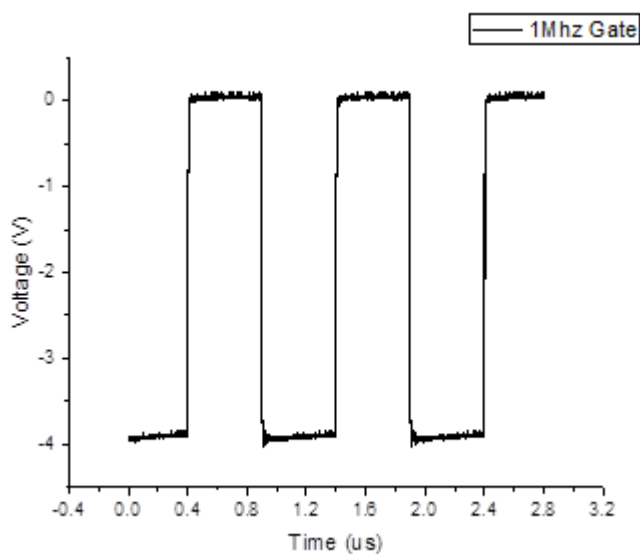


Figure 4.16: The voltage on the gates of the power transistors measured with reference to ground.

The switching node voltage of the integrated buck converter at 10V (with 50% duty cycle) can be seen in figure 4.17. The voltage levels of the switching node would be between the input voltage (10V) minus the voltage drop across the drain-source terminals of the high-side power transistor and the voltage drop across the drain-source terminals of the low-side power transistor in the buck converter. The voltage drop across the power transistors is determined by the on-state resistor, R_{on} and the on-state current flows through the transistors which effectively translates to the conduction loss of the power transistors. The rise and fall time of the switching node voltage can be used to quantify the switching losses through the power transistors. The output filter of the buck converter then smooths the switching node voltage into a DC voltage as shown in Figure 4.18.

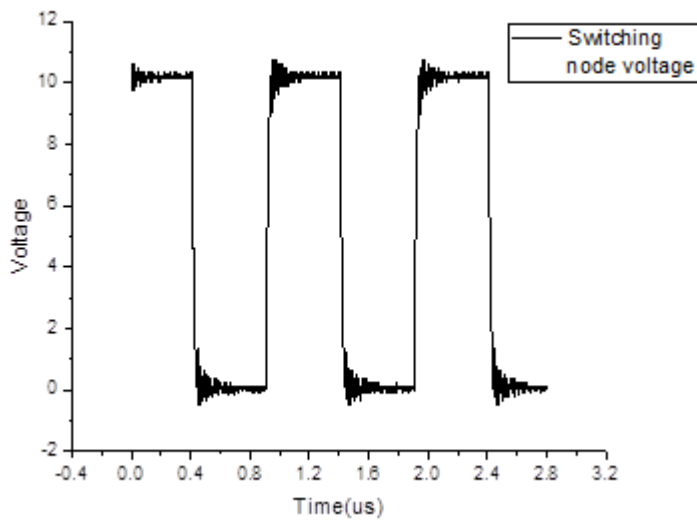


Figure 4.17: The switching node voltage shown between the two power transistors with an input voltage of 10V and a duty cycle of 50%.

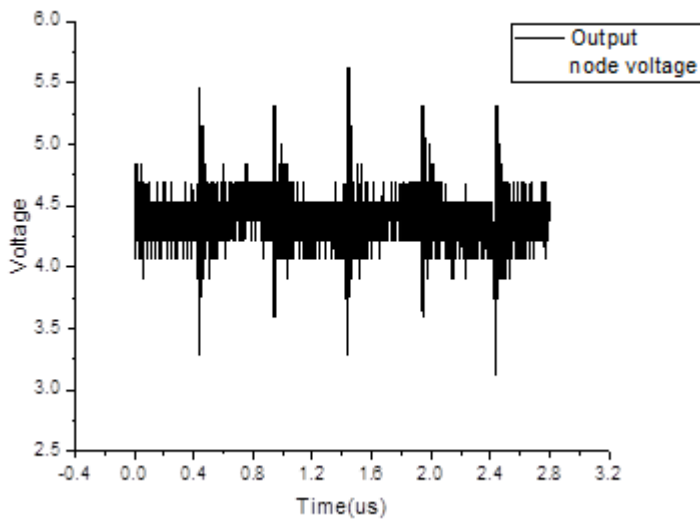


Figure 4.18: The final output signal for a 10V input 50% duty cycle after smoothing via the filter.

The total efficiency of the buck converter is extracted from the input power and the output power as measured by the electronic load connected to the output of the output filter of the buck converter. This is done for a range of duty cycles to show the total efficiency of the converter across a range of output powers. This is important to quantify as the converters used

in an envelope tracking system will require a range of output powers that change over time and may spend more times in a certain value of the output power.

Figure 4.19 shows the efficiency versus output power of the buck converter. The efficiency in the converter ranges from 43% to 81% across the studied output powers. The duty cycle between 20% and 75% were measured which translates to an output power range in the converter between 0.077W and 0.833W.

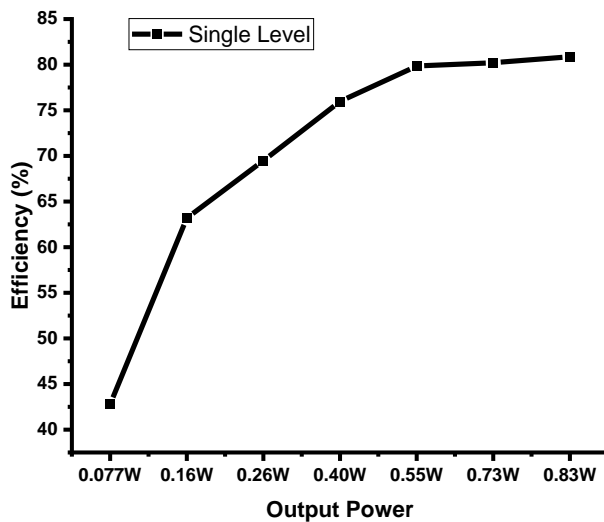


Figure 4.19: A plot of the efficiency vs output power in the system operating at 10V 1MHz.

The losses in the gate driver section of the circuit remain constant across the varying duty cycles at 0.02W. This contributes a small amount to the total losses at the system even at low output powers, the low current present through the gate driver is to thank for this.

The inductor used for this setup has a value of 47 μ H calculated from the previously given equation in section 1.5. Separating the losses through the inductor is not possible using the current testing setup although can be estimated as the inductor is a commercial one using the manufacturer provided value for the series resistance. This is given to be around 5 Ω leading to an estimated power loss that varies with duty cycle and voltage fed through the system. After the estimation of inductor and gate driver losses the rest of the circuit losses are attributed to the power transistors. The total breakdown of losses for each component is shown in figure 4.20.

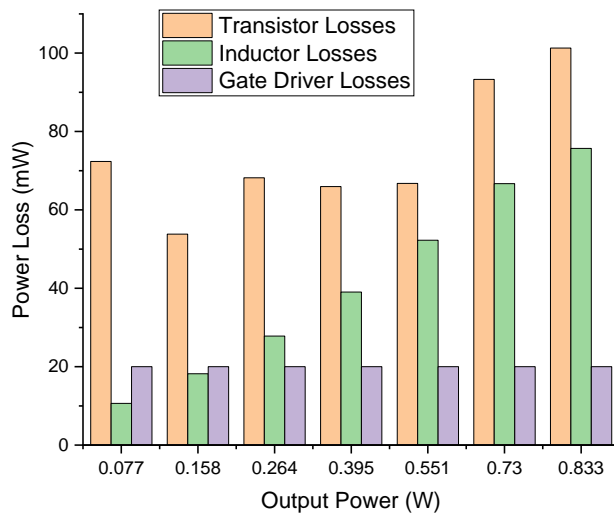


Figure 4.20: The breakdown of losses presents in each component operating at 10V 1MHz

The dominating loss of the buck converter comes from the power transistors as observed in Figure 4.20. It is noted that the power transistor loss remains constant with output power which varies from 0.077W to 0.83W. Below 0.551W, the transistor loss doesn't increase with increasing output power, this leads to the large increase in the efficiency of the buck converter as shown in Figure 4.19. Figure 4.21 shows the conduction and switching losses breakdown of the power transistors versus the output power. It is noted the proportion of the switching losses to the total transistor loss is small (about 5%). Most of the power transistor losses come from the conduction losses. The high side power transistor conduction loss increases with increasing output power while the low side transistor loss decreases with increasing output power. This is expected as the output power increases with increasing duty cycle which leads to the high side transistors to conduct at an increasing proportion of each switching cycle.

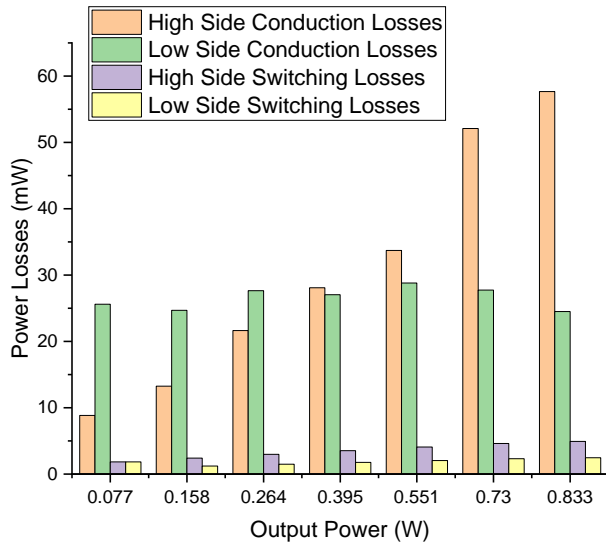


Figure 4.21: The measured switching and conduction losses for a range of duty cycles measure at 10V 1MHz

4.11.2 1MHz 25V Operation

The next operation of the circuit to analyse is at a higher input voltage. In this section, the integrated buck converter with an input voltage of 25V at 1MHz will be analysed. The 1MHz input pulse signals are as described in Section 4.8 with a duty cycle between 20% and 75%.

One of the main considerations to make when operating the circuit at 25V is the voltage/current slew rate of the high side switching transistor. If the slew rate is too slow to fully switch off the high side transistor before the low side transistor is on, this could lead to the breakdown of the power transistors as both the high voltage (25V) and current are present. An introduction of a total dead time of 10% between the high side and low side input pulses is sufficient to prevent this from occurring.

A measured output power ranges from 0.32W to 4.44W with the duty cycle varied from 20% to 75%. The switching node voltage at 50% duty cycle is shown below in figure 4.22.

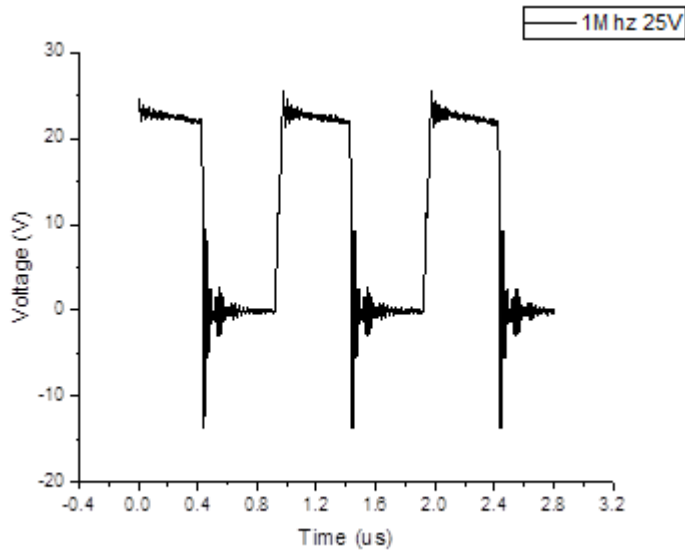


Figure 4.22: The Switching node voltage operating at 25V 1MHz with a 50% duty cycle

It is noted from Figure 4.22 that the increased voltage the high side transistor must rise too has an increased rise and fall time compared to the 10V operation. In the 25V operation, the rise time and fall time are approximately 20ns, compared to the previous results at 10V of 2ns.

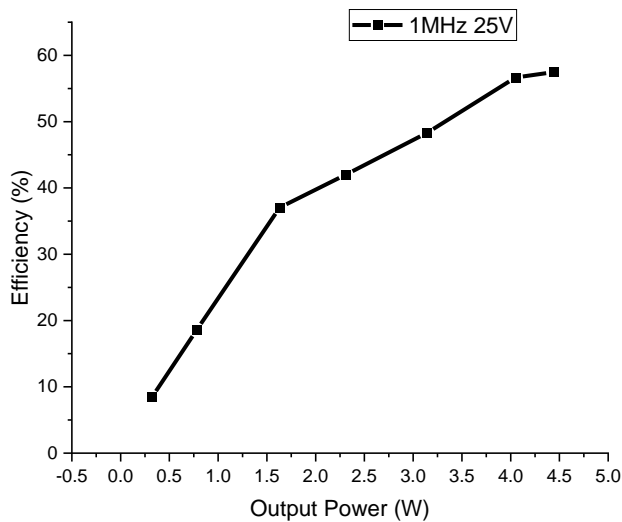


Figure 4.23: The efficiency of the circuit operating at 25V 1MHz.

The efficiency of the buck converter with varying duty cycle (output power) at 25V input voltage is shown in Figure 4.23. The efficiency is lower than that of the 10V operation. To investigate this further, the loss breakdown analysis is carried out.

The dominating loss of the buck converter is from the power transistor losses. An increase in the losses through the inductor are also expected and are estimated to be 0.44W at 4.4W. The contribution of each loss component can be seen in figure 4.24.

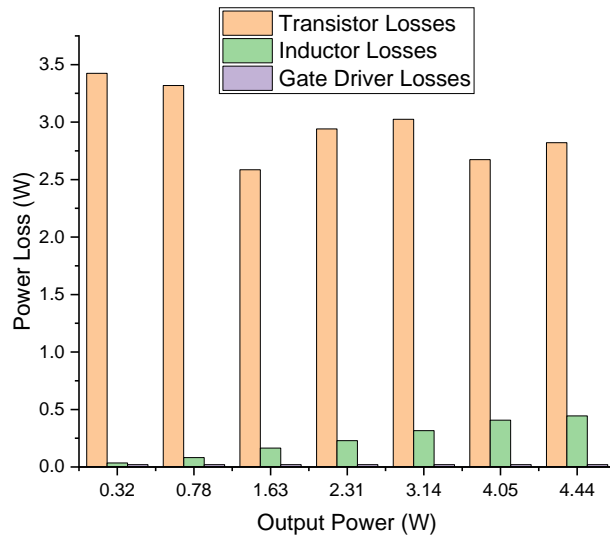


Figure 4.24: A breakdown of all the losses in the circuit operating at 25V 1MHz.

To understand the loss contribution of the power transistors, the switching and conduction loss analysis is performed. The breakdown of both the switching losses and the conduction losses in the circuit is shown in Figure 4.25. The proportion of the switching loss to the conduction loss for the power transistors is higher for the 25V operations compared to that of the 10V operations particularly at high output powers. This is due to the increased slew rate of the signal and therefore the switching time. Due to the non-linearity of the intrinsic capacitances at this higher voltage slower switching characteristics within the devices are seen. This leads to more time for power loss to occur and as such an increase in switching losses.

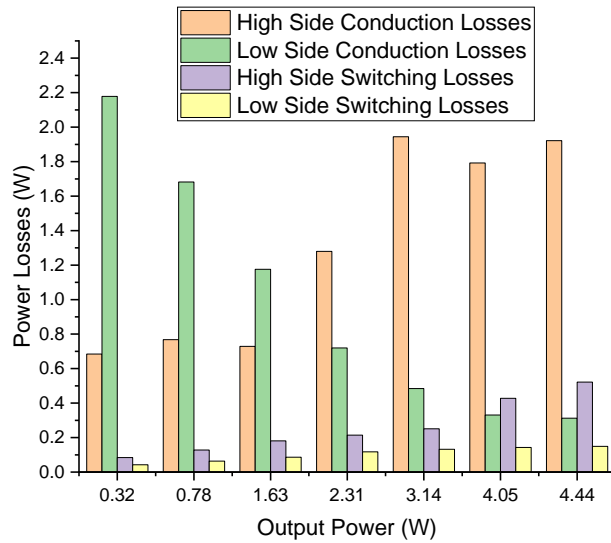


Figure 4.25: A breakdown of the switching and conduction losses in the power transistors operating at 1MHz 25V.

The conduction loss of the power transistors at 25V operations is higher than that of the 10V operations due to the higher power. The increasing (decreasing) trends in the conduction loss of the high (low) side power transistors are also observed with increasing output power as discussed in Section 4.11.1 for the 10V operations.

4.11.3 50MHz 10V Operation

After the 1MHz characterisations, the integrated buck converter was next tested at a higher switching frequency of 50MHz and an input voltage of 10V. At 50MHz, it is no longer possible to use the signal generator to produce the input pulses and the switch over to the FPGA is made. The details of the input pulse signal generation using FGPA is provided in Section 4.8. The input signals vary from 0V (low level) to 2.5V (high level) and allow the duty cycle to be changed between 30% and 70%.

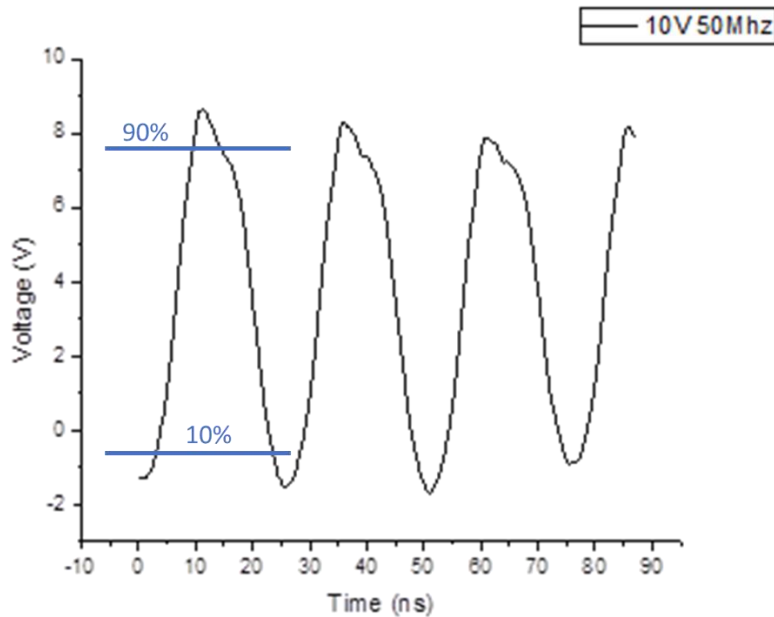


Figure 4.26: The switching node voltage at 50MHz, 10V, 50% duty cycle showing the rise and fall time taken between 10% and 90% of the maximum value.

Figure 4.26 shows the voltage waveform at the switching node of the buck converter. It is noted that unlike the 1MHz operation, the switching node voltage waveform shows a ‘sinusoidal’-like with 50MHz switching frequency. This is attributable to the slew rate of 50MHz input signal generation from the FPGA as described in Section 4.8. The rise and fall time is estimated to be around 7ns, which is larger than the on-time of the power transistors based on a 50% duty cycle. The integrated buck converter can only be tested between 30% and 70% duty cycle at 50MHz. This is because the slew rate of the FPGA signal generated waveforms prevents the switching of the digital isolator when operating less than 30% duty cycle and more than 70% duty cycle.

Figure 4.27 shows the efficiency of the buck converter against the output power between 30% and 70% duty cycle at 50MHz. The efficiency increases with increasing output power, similar trend observed in the 1MHz operation. However, the efficiency of the 50MHz operation is lower than that of the 1MHz.

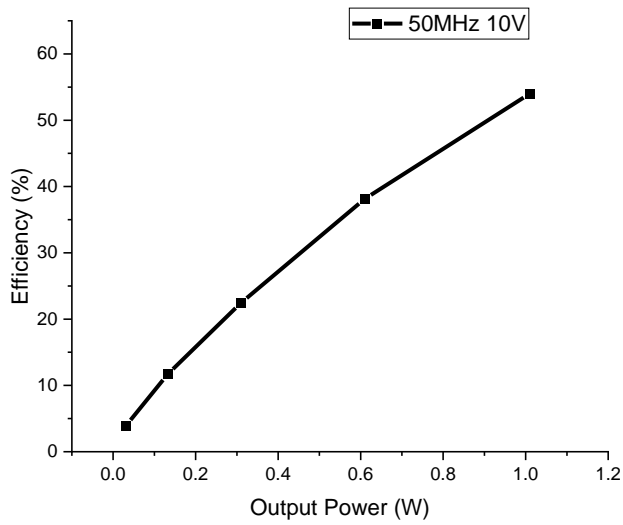


Figure 4.27 - A figure showing the efficiency of the circuit operating at 50MHz 10V between 30% and 70% duty cycle.

A full breakdown of the losses present in each component of the circuit is shown in figure 4.28. Unlike the 10V 1MHz operations, a larger proportion of the losses come from the power transistors at 10V 50MHz.

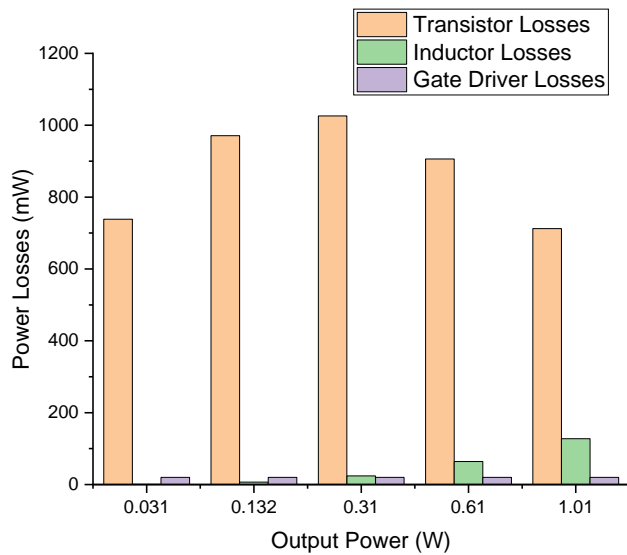


Figure 4.28: A breakdown of all the losses in each section of the circuit at 50MHz 10V.

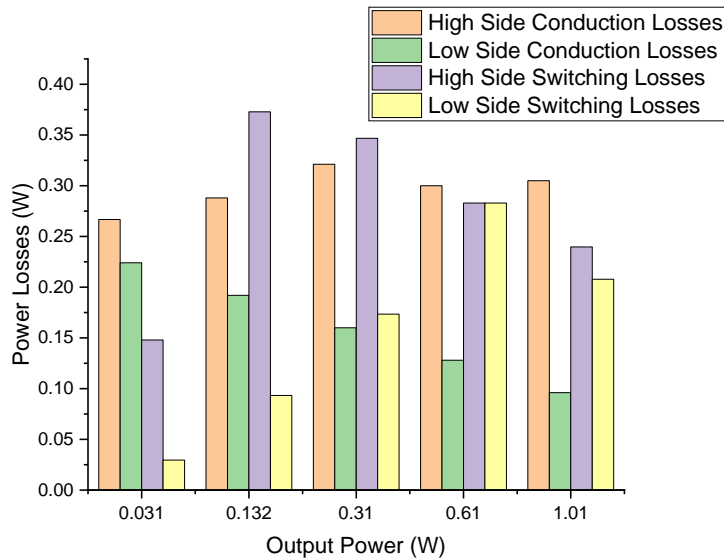


Figure 4.29: The switching and conduction losses in the circuit operating at 50MHz 10V.

A breakdown of the switching and conduction losses from the power transistors is presented in figure 4.29. Separation of the switching and conduction losses at 50MHz is particularly difficult as the switching node voltage waveform is not a square wave, which leads to the difficulty in defining the switching times and the conduction on-state time. In this study, the switching losses are estimated from the extraction of the rise time and fall times from 10% to 90% of the maximum switching node voltage. And the conduction loss is estimated from the time between the switching cycle. There is a large increase in the switching losses through the power transistors in comparison with the 1MHz operation which is to be expected. This is due to the increase of the switching cycle with a higher switching frequency. In addition, as the switching signal is not a well-defined square wave and is close to a sin wave in nature as a result of the slew rate, this will increase the switching losses as effectively the signal is never entirely on or off. Further investigation on this will be made using SPICE simulation in Section 4.14.

The inductor used in the buck converter is different to the 1MHz operation due to the higher frequency. 1812PS coil wound inductor from Coilcraft was chosen for its ability to operate at high frequency and low value tolerance as well as a lower series resistance of 0.6ohms at 50MHz. The estimations of the power losses of the inductor is based on the series resistance value provided by the manufacturers. Gate driver losses remain constant across the range of duty cycles at 0.02W.

These experimental results are promising but due to limitations that will be examined in the simulations the potential efficiencies are not reached. Our peak efficiency operating at 25V,

1MHz was under 60% and a peak efficiency at 10V of 82%. At the higher operating frequencies, 50MHz, the peak efficiency again is under 60%.

4.12 Simulations

LTSpice simulations of the buck converters were performed to produce estimates of the maximum operating frequencies and the efficiencies that could be achieved at different output powers. Figure 4.30 shows the basic buck converter schematic that was simulated in LTSpice.

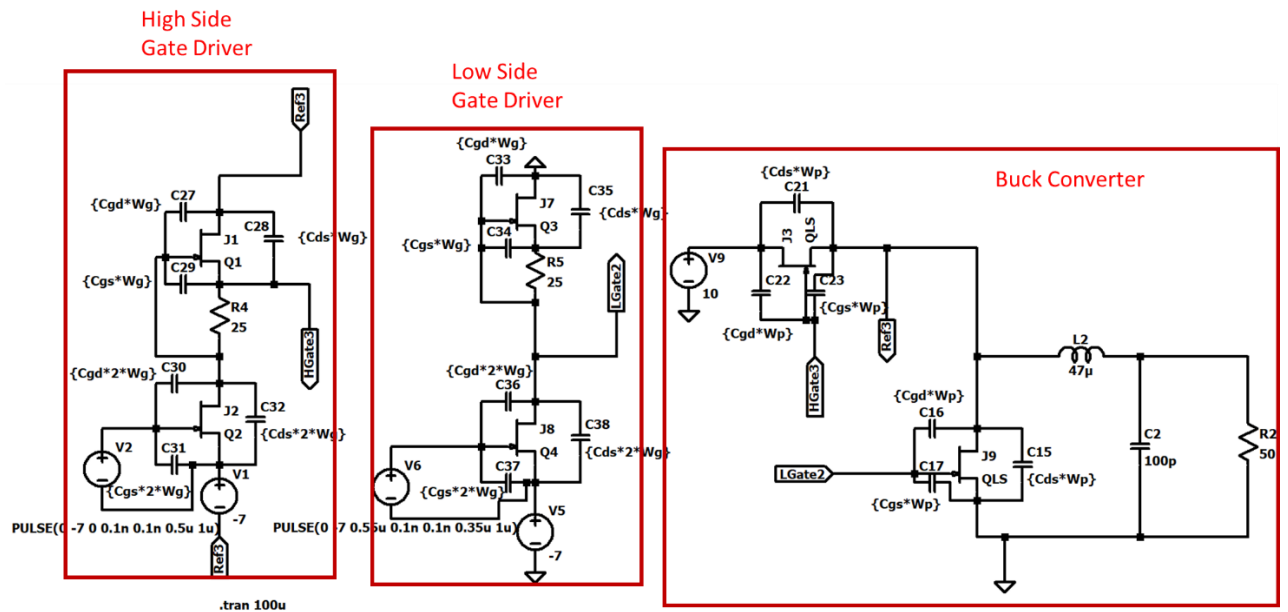


Figure 4.30: Single level buck converter spice simulation operating at 10V 1MHz

A number of SPICE parameters are defined in order to model the GaN transistors and the monolithically integrated buck converters that have been fabricated. There are two main types of transistors used within the buck converter, small gate width (25 μm) transistors for the gate driver and large gate width (1mm) power transistors. For the SPICE models, an n-type JFET model in the LTSPICE software was used. The threshold voltage, transconductance parameters, drain and source ohmic resistances of the JFET model were set to fit the fabricated GaN transistors in this study. A V_{th} of -3.5V is used, the transconductance is defined by the W_g and W_p , the device widths used in the gate driver transistors and power transistors. The R_d and R_s , drain and source resistances, are defined by the R_{on} of 3ohm.mm which is scaled appropriate to the power transistors and the gate driver transistors.

Three capacitors are added to the JFET model to match the intrinsic capacitances of the fabricated GaN HEMTs. A source gate capacitance (C_{gs}) of 1.25 pF/mm, a source drain

capacitance (C_{ds}) of 0.5pF/mm and a gate drain capacitance (C_{gd}) of 0.1pF/mm, were set to match measured values in the GaN HEMTs.

The other components in the system, the resistors inductor and capacitor, are chosen to match the experimental components. The inductor is an external component, a wire wound power inductor named 1812PS-102JLC with a maximum resistance of 50mohms. As such the inductor in the simulations is given this resistance. The load in the system is assumed to be a fixed load of 50Ohms.

The input signal driven into the gate driver is assumed to have a rise and fall time of 0.1ns for the initial simulations. As these initial simulations are performed for ‘ideal’ conditions they will give a representation of the best-case scenario results that are possible with the currently producible device characteristics. In Section 4.13.4, the discussion will expand and compare the simulations to the experimental values with different rise and fall times of the input signals as well as the heating effect.

4.13 Simulation Results

4.13.1 1MHz 10V Operation

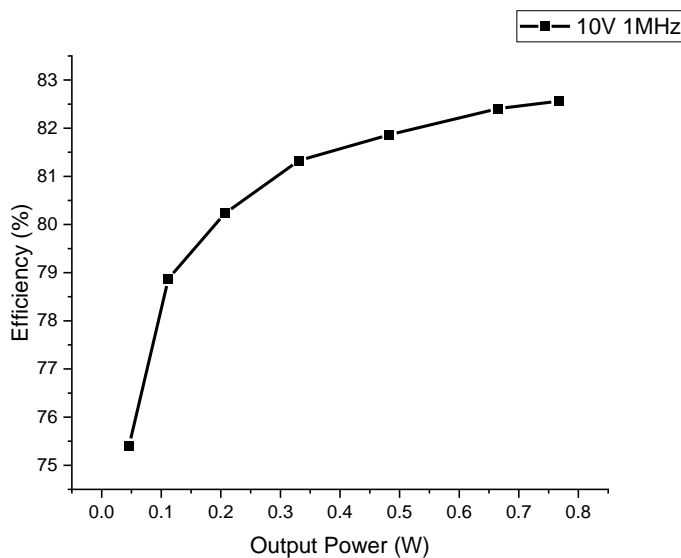


Figure 4.31: The efficiency curve of the buck converter operating at 10V 1MHz.

The simulated efficiency of the buck converter at 10V and 1MHz across a range of output powers has been plotted in figure 4.31. As can be seen the efficiency starts low at 75% and increases to 88% at higher output powers. The increasing efficiency trend agrees with the

experimental result trend and is expected as the transistor losses become a smaller percentage of the total power through the converter. However, the overall efficiency of the simulated efficiency is slightly higher than the experimental results.

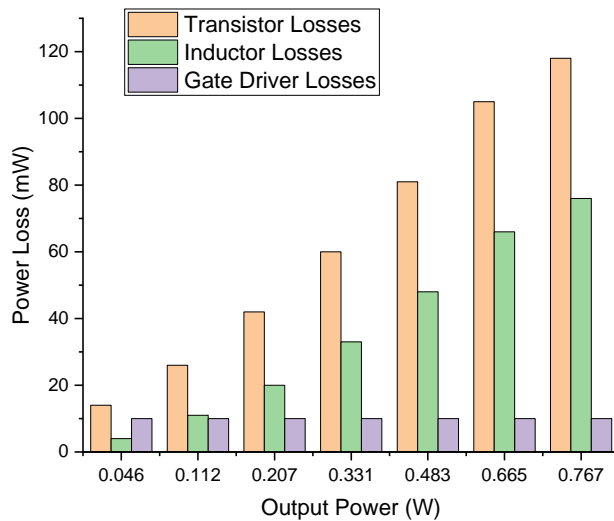


Figure 4.32: A breakdown showing how much each component in the circuit contributes to the losses.

The loss breakdown of the simulated converter versus the output power is as follows in figure 4.32. The majority of the losses come from the power transistors and the losses increase with the output power, making up around 90% of the total losses at the highest output power. This is consistent with the experimental results as shown in Section 4.11.1. Compared to the experimental results these simulated results show lower losses at lower output powers than the real devices but very similar values for losses at peak output powers. This leads to a peak efficiency value very closely matched between the two, 83% for the simulations and 82% for the experimental results, showing the accuracy of the simulations. One of the main reasons for the high efficiency at lower output power for the simulated results

A breakdown of the simulated switching and conduction losses within the power transistors is presented below in figure 4.33.

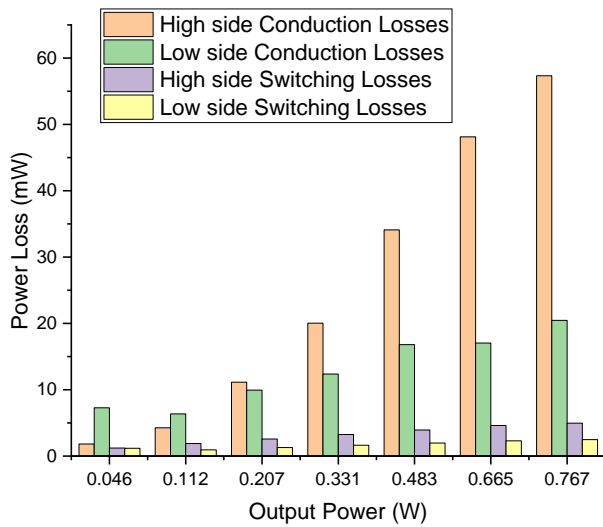


Figure 4.32: The breakdown of the simulated conduction and switching losses in the buck converter operating at 10V 1MHz

This aligns closely with the experimental results with conduction losses dominating the loss profile of the transistors.

This has led to results close to the experimental results particularly when looking at the peak efficiency achieved in section 4.11.1.

4.13.2 1MHz 25V Operation

In the next step, the input voltage of the simulated buck converter circuit was increased to 25V. The simulation of the efficiency of a 1MHz circuit operating at 25V is shown below in figure 4.33.

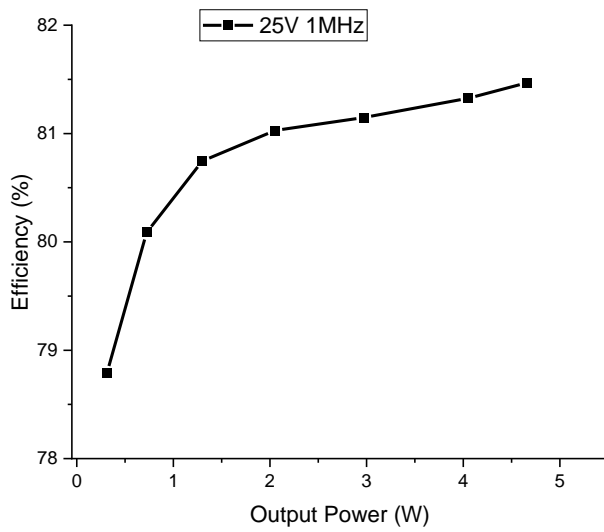


Figure 4.33: The efficiency curve of the buck converter operating at 25V 1MHz.

The observed increasing efficiency trend with increasing output power of the buck converter is expected as described previously. However, the total efficiency is lower than the simulated 10V operation, which agrees well with the experimental results in Sections 4.11.1 and 4.11.2.

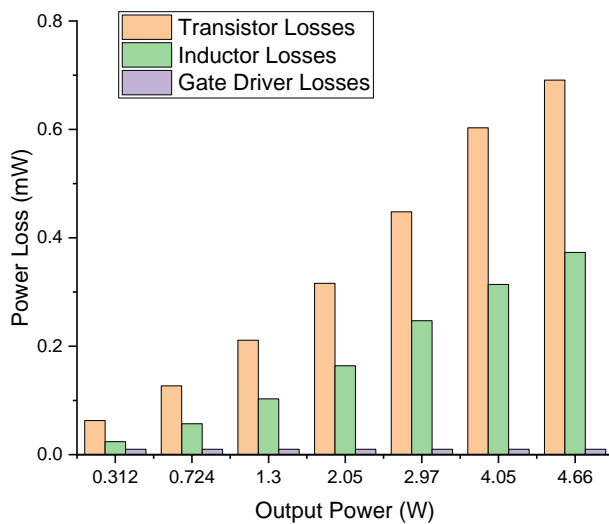


Figure 4.34: The loss breakdown in the simulated circuit operating at 25V 1MHz.

The loss breakdown in each component is shown below in Figure 4.34. These are larger than the 10V switching which is to be expected due to the lower efficiency of the circuit. Compared to the experimental results, the efficiency and losses are substantially higher and lower, respectively. This is likely due to the heating effect becomes more dominant at higher output

power, which has not been considered in the simulations here. The heating effect will be discussed in more details in Section 4.14.

A breakdown of the switching and conduction losses has been performed and is shown in Figure 4.35.

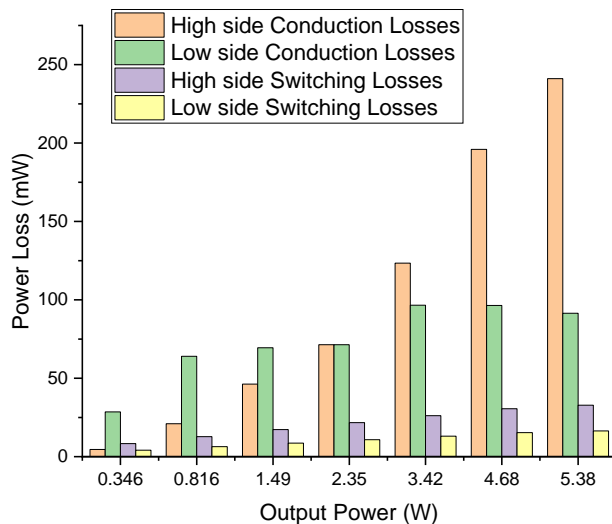


Figure 4.35: A breakdown of the simulated switching and conduction losses , operating at 25V 1MHz

This again follows the same loss profile observed in the 10V 1MHz simulated results. The low profile is similar to the experimental results for the 10V 1MHz results although compared to the 25V the values are much lower.

4.13.3 50MHz 10V Operation

Simulations of the buck converter at 50MHz, 10V to compare to the experimental results has also been performed. The input pulse signals used in the simulations are with 0.1ns turn on and off times in the initial simulations. The duty cycle is varied between 30% and 70% to match the experimental testing conditions. The simulated efficiency of the buck converter versus output power is shown in figure 4.36.

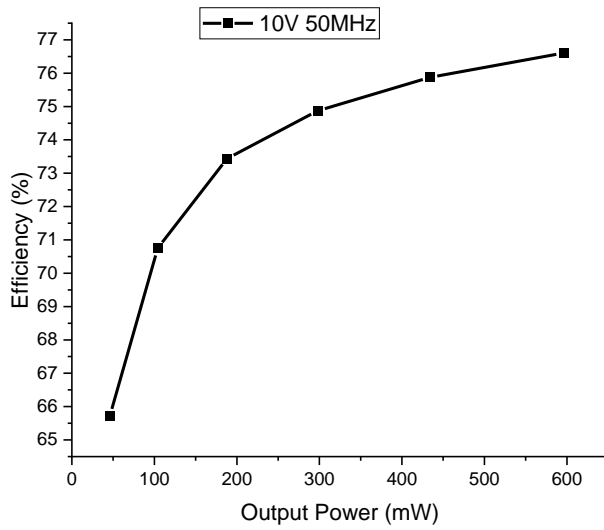


Figure 4.36: The simulated efficiency of the buck converter at 50MHz and input voltage of 10V.

A peak efficiency of 81% is simulated with 50MHz and 10V, which is lower than that of the 1MHz, 10V simulated efficiency. The loss contribution from each component is broken down across a range of output powers in figure 4.37. Similar to the 1MHz simulations, the transistor loss is the dominating loss in the 50MHz operations. However, the magnitude of the transistor loss is higher at 50MHz primarily due to the increased in the switching losses at higher switching frequency.

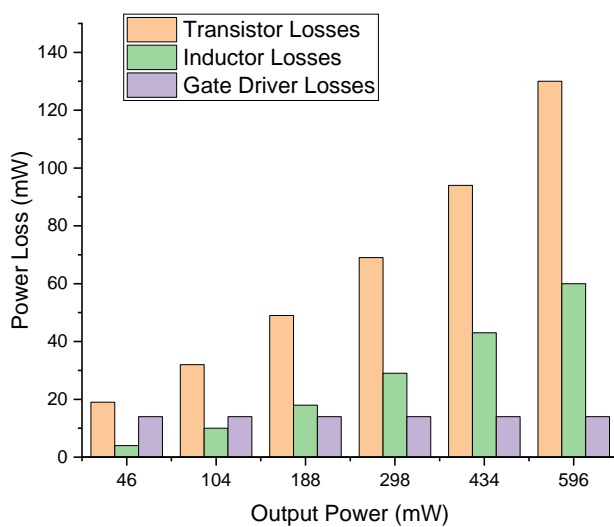


Figure 4.37: The loss breakdown of the buck converter at 50MHz and 10V.

It is noted that the simulated efficiency is higher than that of the experimental efficiency at 50MHz. As described above, the rise and fall times used in the simulations is 0.1ns, which is significantly lower than the rise and fall times measured from the pulse signal generated from the FPGA. The effect of the slew rate of the input pulse signal on the efficiency of the buck converter at 50MHz will be discussed below.

The switching and conduction losses are shown below in Figure 4.38.

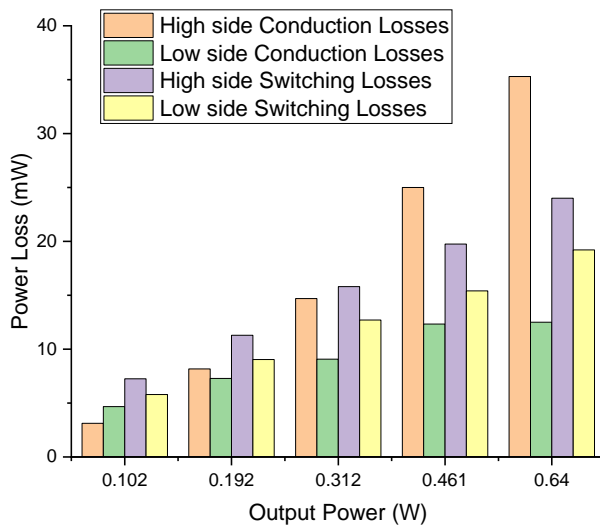


Figure 4.38: The simulated results showing the switching and conduction losses in the power transistors operating at 50MHz 10V.

This shows the much higher switching losses in the circuit when operating at 50MHz. This is to be expected and follows the trend of the experimental results. Although the switching signals used in this simulation were given a much faster rise and fall time than what was observed in the experimental results so the magnitude of these is smaller. Section 4.14.1 will examine in greater detail the simulation efficiencies achievable with a simulated switching time close to the experimental observations.

4.14 Further Simulations

4.14.1 Heating Effects and Slew Rate

While the 10V 1MHz simulations produced results close to those observed in the experimental results, both the 25V 1MHz and 10V 50MHz simulated efficiencies are somewhat higher than the experimental efficiencies. The first element to consider is the switching time of the signal used in the 25V setup. This was altered to match the same rise and fall times of the switching

node voltages for the experimental results. As well as this, it is assumed that heating effects in the power transistors contribute to the reduced performance within the devices^{13,14}. One observation regarding the switching node voltage that points toward this effect is the decrease in the switching node voltage during the on-state of the high side power transistor. This is observed in the experimental result in section 4.11.2 figure 4.22. To take the heating effect into account in the simulations, an increased channel resistance is assumed within the device as would occur with heating effects within the device. As well as this the signal fed into the gate has a roll off the voltage. This produces the same effect as what is observed in the switching node voltage when heating effects are present as in figure 4.22. As a result, the switching node voltage in the simulation also exhibits a decrease during the on-state of the high side power transistor as shown in figure 4.39.

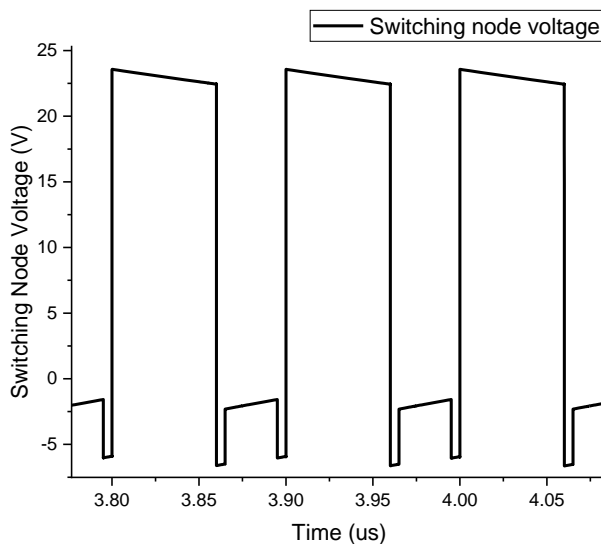


Figure 4.39: The switching node voltage in the 25V 1MHz simulation accounting for heating effects and an increased switching time.

Following on from this, the simulated efficiency was extracted across a range of output powers corresponding to the same duty cycles tested in the experimental setup. The simulated efficiencies are shown in figure 4.40. This shows a peak efficiency now close to the experimental results, showing that the heating effects and the increased switching times of the switching node voltage are the probable causes of the lower efficiency observed in the experimental buck converter. This larger switching times observed in the experiments compared to the initial SPICE simulations in Section 4.13 is likely due to the non-linearity of the intrinsic capacitances of the power transistors with applied voltage. On the other hand, the

SPICE simulation assume constant intrinsic capacitances which likely under-estimate the real capacitances in the fabricated power transistors.

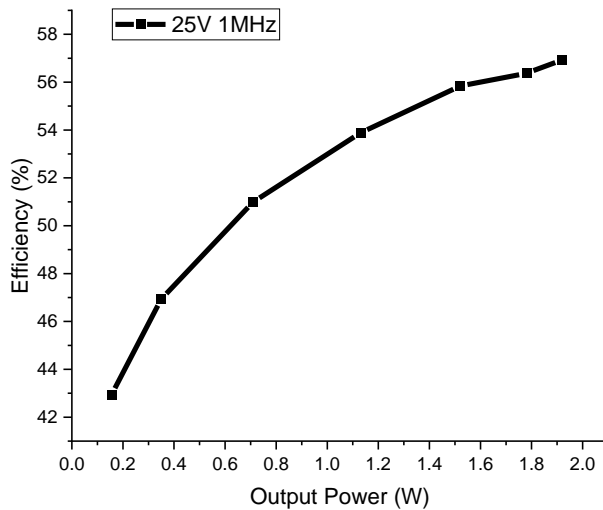


Figure 4.40: The 25V 1MHz simulated efficiency against output power

The next set of comparative simulations were done with the 10V 50MHz setup. The rise time and fall time for the input pulse signals were set as 7ns in the simulations to match with the rise/fall times of the input pulse generated from the FPGA. Heating effects were not included in 10V simulations as the discrepancies between the simulated efficiency and experiment efficiency are minimal with the 1MHz switching frequency. It is assuming that the output power (and the total loss) with the 10V operation is low enough not to induce significant heating effect unlike the 25V operations. The simulated efficiency of the buck converter at 10V 50MHz is shown in figure 4.41.

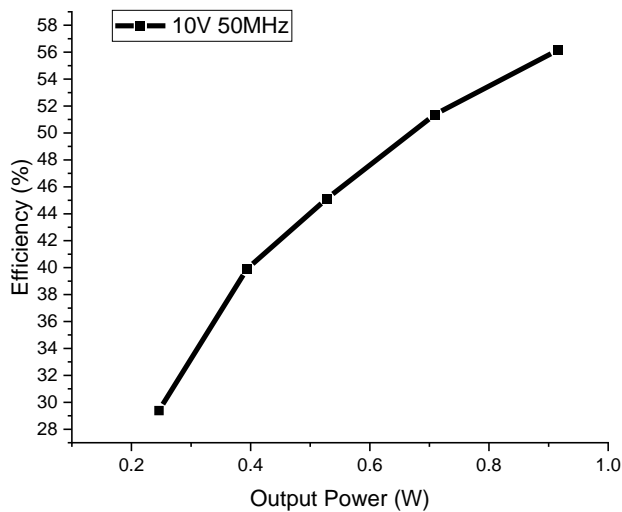


Figure 4.41: The efficiency of the 50MHz 10V simulation with increased input signal slew rate.

With an increased slew rate of the input pulse signal, the simulated efficiency aligns more closely with the experimental results reaching only a slightly higher efficiency peak of 56% compared to 54% in section 4.11.3.

These results demonstrate that with a better input pulse signal generation, it should be possible to achieve the efficiencies shown in section 4.13.3 under these operating conditions using the device layout and components fabricated within the buck converter.

4.14.2 Transistor Design

This highlights the importance of the transistor design and how changing the layout of the transistor, for example reducing the source-drain separation (Lsd) to reduce the Ron and in turn the conduction losses, are key. Reducing the Ron of the transistors in this manner will reduce the conduction losses but will also reduce the breakdown voltage of the transistor. Considering the trade off in the gate width and switching speed is also important to reduce switching losses. The target breakdown voltage for the power transistors is 100V to give enough of an over design to allow for any possible overshoots during the switching transient operation. In order This leads to a smallest Lsd of 5 μ m which from experimental data can sustain a blocking voltage of 100V. For a design that allows only a 50V maximum breakdown voltage from experimental data gives a Lsd of 3 μ m and a lower Ron of 2.5mohm. This will reduce the conduction losses and a comparison between the efficiency of a 5 μ m Lsd and 3 μ m device is shown below in figure 4.42.

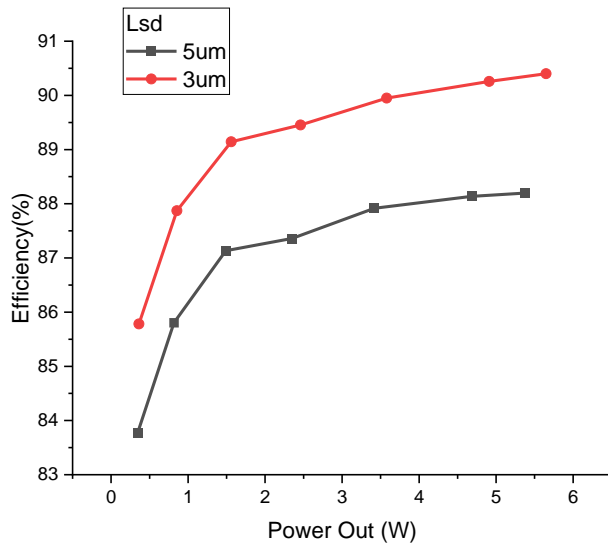


Figure 4.42: A simulated efficiency comparison of the buck converter with power transistors devices with L_{sd} of $5\mu\text{m}$ and $3\mu\text{m}$ operating at 1MHz, 25V.

4.15 Field Plate Design in Buck Converters

As discussed in Chapter 2, the dynamic R_{on} effects primarily come from charge trapping in the GaN HEMTs. This trapping mechanism as a result of GaN buffer and surface trapping leads to a higher resistance of the GaN HEMTs when a high off state voltage is applied. Buffer trapping can be optimised by the growth of the wafer structure and it is beyond the scope of this study. On the other hand, the surface trapping can be reduced by the inclusion of a field plate into the device structure^{15,16}. The field plate helps to spread out peak electric fields at the gate edge and hence reduces the surface-related dynamic R_{on} effects. However, introducing a field plate does have effect on the intrinsic capacitances and is not without drawbacks. Considerations must be made for the power transistor field plate design as they can have a large impact on the intrinsic capacitances.

These capacitances are an important factor on the switching time of the transistors which can in turn impact the total circuit efficiency. In this section of the report, device and circuit level simulations have been performed based on the experimental measurements to investigate the performance impact the field plate can have and provide an avenue into some further experimental work that would be useful to analyse. The potential of even further device level improvements to improve the switching times will lead to higher operating frequencies and higher efficiencies at these frequencies.

4.14.1 Field Plates

There are two main types of field plates typically used to suppress dynamic Ron effects within GaN HEMT devices, the gate field plate (GFP) and source field plate (SFP)^{17,18}. These are as their names suggest, connected to the gate terminal and source terminal of the device respectively. These layouts can be seen below in figure 4.43.

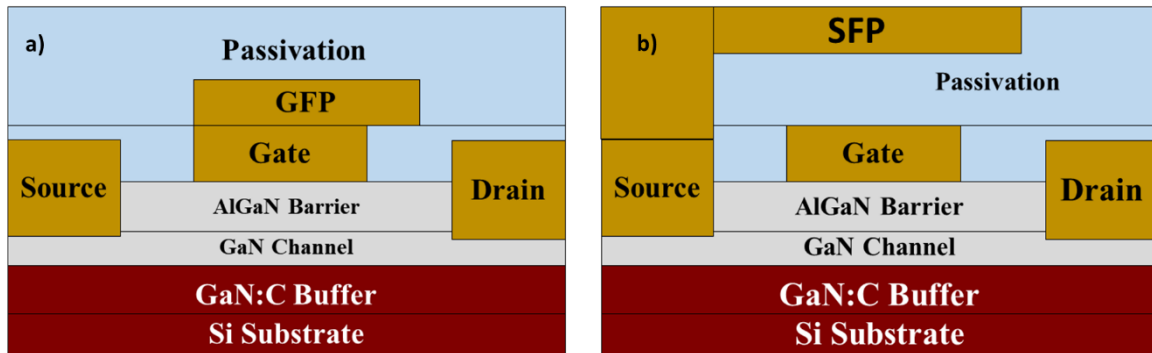


Figure 4.43: The field plate configuration for a) the gate field plate b) the source field plate.

Figure 4.44 shows the dynamic Ron comparison of the GaN HEMTs without field plate, with a gate field plate and with a source field plate. The results clearly demonstrate the effectiveness of the field plate in suppressing the dynamic Ron in the GaN HEMTs. Both gate field plate and source field plate GaN HEMTs shows the similar level of dynamic Ron.

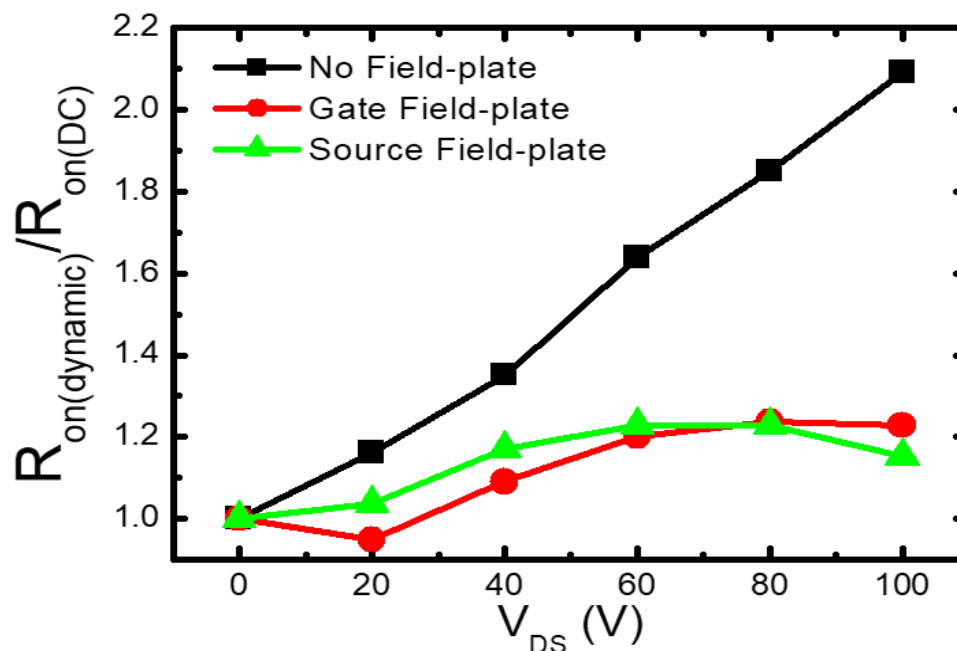


Figure 4.44: The dynamic Ron performance of the devices with no field plate, a gate field plate and a source field plate.

This means that other factors must be considered regarding the device layout when deciding which field plate to choose. The fabrication steps needed are slightly different for each as they connect to different pads on the device although in terms of complexity, they are similar. The other major consideration that must be made is regarding the effect the field plates have on the capacitances within the device. Typically, in a standard GaN HEMT device, C_{gd} is the intrinsic capacitance that determines the switching time of the device and is also known as the miller capacitance^{19,20}. Therefore, it is vital to minimise the capacitance value of C_{gd} in the transistor. C_{ds} can also influence the switching time although as it is typically charged with the drain and source current, this is typically larger than the charging current for C_{gd} . Thus, C_{ds} is usually not dominant.

Simulations of the devices and more specifically the C_{gd} , were first done in Sentaurus TCAD and matched to an experimental device to verify the accuracy of the results. An example of the device layout used in the simulation with a gate field plate is shown in Figure 4.45. The wafer structure and device structure is the same as the other device level simulations previously performed in Chapter 3 with the only difference being the field plate in the device.

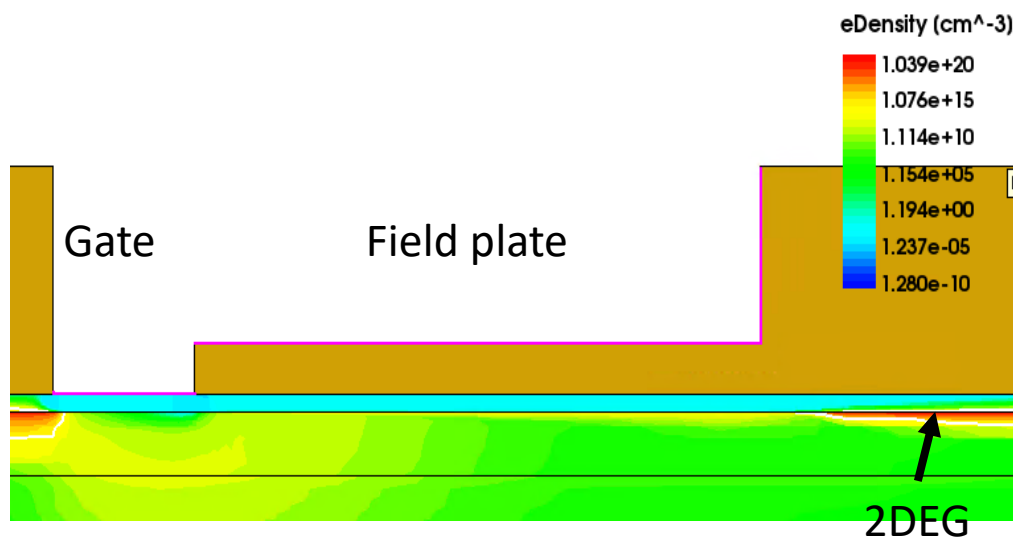


Figure 4.45: The gate field plate device layout simulated in sentaurus.

An 8mm GaN transistor with a gate field plate was characterised experimentally to extract its intrinsic capacitances. These were then used to match the simulated results close to what would be expected in a real device. This simulation was then extended to provide the results for the devices with no field plate and source field plate. The simulated C_{gd} results for all three configurations are shown below in Figure 4.46.

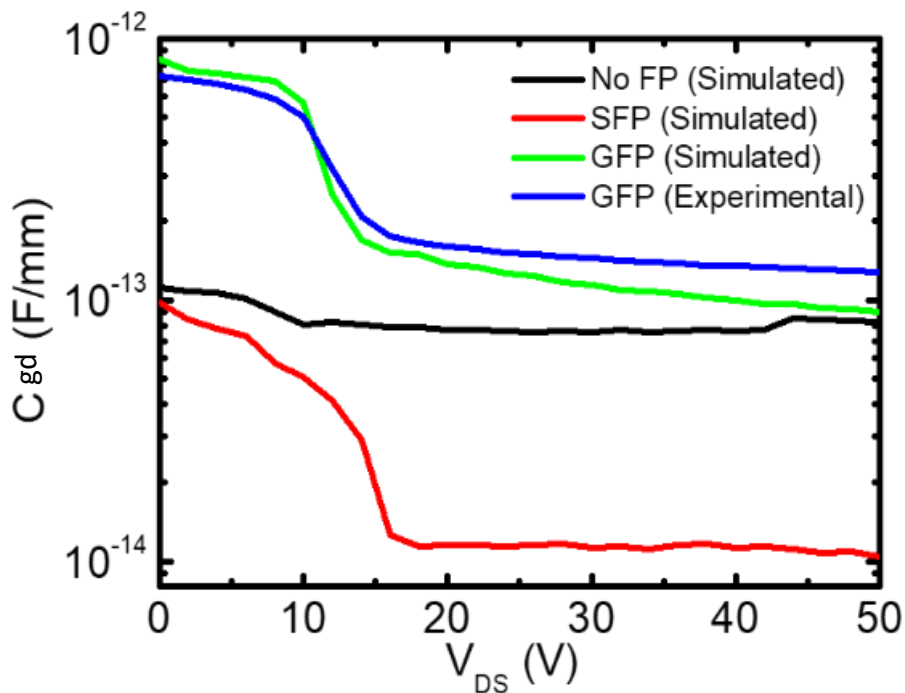


Figure 4.46: The C_{gd} results simulated for the devices with no field plate, a SFP and a GFP.

The result shows both the close matching between the experimental and simulation results for the GFP devices. Both the device without field plate and the SFP device show a lower C_{gd} value in comparison with the GFP device. The C_{gd} of the SFP device shows a large drop off above 15V. This shows the performance advantages that can be brought about especially when operating at higher voltages, in our case at 25V operation. The step change is also present in the GFP device although the capacitance value that is higher than the other configurations.

The step change occurs at around 15V is caused by the field plate effectively ‘pinching off’ and depleting the channel region under it. This is the point at which the peak electric field at the gate edge stops increasing with the applied bias and a second peak of the electric field in the channel region is now present at the edge of the field plate. The voltage that this occurs at is controlled by the thickness and permittivity of the SiNx passivation deposited underneath the field plate. The thinner this region is, the lower the voltage the depletion of the channel occurs at is, although considerations must be made for the breakdown of the material to ensure the field plate does not short, particularly with the SFP which could short to the gate of the device and prevent correct functionality.

LTSpice simulations were then created for the integration of the varying field plate devices into the standard buck converter layout. The device simulation layout is identical to the ones

used in chapter 4. With different values used for the C_{gs} and C_{gd} , 1.25pF and 0.06pF. The simulated switching speed for each configuration, GFP, SFP and No FP are shown below in table 4.2 and figure 4.47.

Parameters	Without FP	GFP	SFP
Turn On (ns)	0.39	1.5	0.32
Turn Off (ns)	0.11	0.46	0.18

Table 4.2: A table showing the simulated buck converter switching speed operating at 50Mhz for different FP configurations

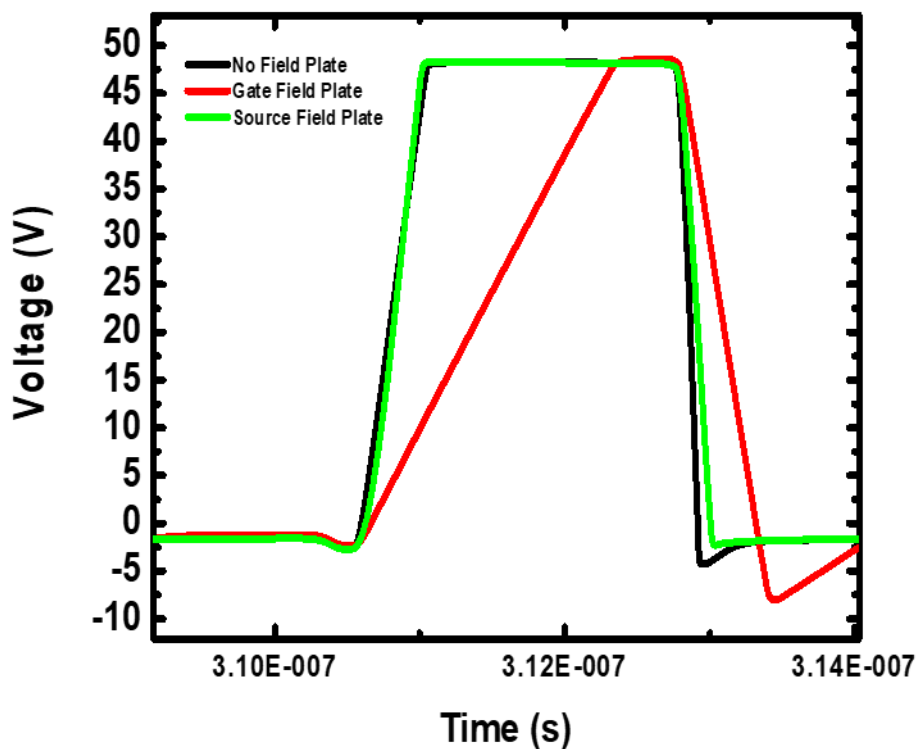


Figure 4.47: A Figure showing the simulated buck converter switching speed operating at 50Mhz for different FP configurations

The clear increase in switching times from the GFP matches with what would be expected due to the increase in C_{rss} and the effect his has on transistor switching speeds. The SFP has a

small overall increase in switching speed although is very close to no FP at all, the increase in turn on speed from 0.39ns to 0.32ns is offset by the decrease in turn off speed 0.18ns to 0.11ns. This change in switching time translates directly to a change in the overall circuit efficiency. This can be seen in figure 4.48 showing the efficiency of the buck converter with each power transistor field plate setup.

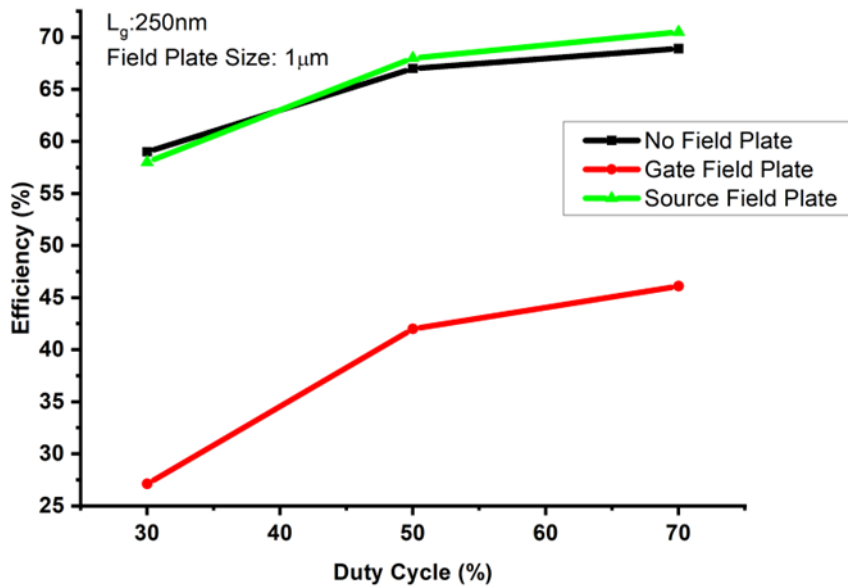


Figure 4.48: A Figure showing the simulated buck converter efficiency operating at 50Mhz for different FP configurations

The increased capacitance from the GFP greatly negatively affects the efficiency seen and offsets any improvements in dynamic Ron that the setup can provide. The SFP and no FP setups are very close with the SFP showing a slightly higher efficiency owing to the reduction in turn on time. As well as this the dynamic Ron benefits it can provide will further increase the efficiency as these are not present in the LTSpice simulation setup.

4.16 Conclusion

It has been demonstrated both experimentally and using simulations the feasibility and potential improvements in efficiency that can be achieved using AlGaN/GaN HEMT devices in monolithically integrated buck converters. Efficiency results in excess of 80% have been demonstrated for 1MHz 10V operation. Single phase demonstrations at 25V 1Mhz show efficiency values up to 57%. The maximum frequency demonstrated experimentally has been

50MHz 10V. Operation in these operating parameters shows efficiency values of 54% significantly lower than the 10V 1Mhz efficiency.

These efficiency values do however decrease at higher frequency and higher voltage operation. A number of explanations for this have been investigated, higher power through the transistors is expected to give lower efficiency at higher voltages although this does not explain the entire discrepancy. Investigations into the devices heating effects were performed in simulated results and justifications for the evidence that this is occurring were presented. This provided simulations more closely matching the experimental work. As well as the poor input signals at higher frequency factoring a large part of the reason for lower efficiency as demonstrated with 50MHz simulations matching the experimental setup.

As well as this device level changes, more specifically the field plate, have been considered to further analyse the performance of the devices and any potential improvements. Simulation analysis of field plate configurations and how this would affect the capacitances in the devices was performed. Simulations of these capacitances were then placed into circuit level simulations of the single level buck converter.

Further work on device parameters as well as improving the signal generation and digital isolation methods would be key to fully demonstrating the feasibility of GaN HEMT devices operating at these conditions.

References

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Chapter 5 – Multi level buck converters

5.1 - Introduction

Following on from the standard monolithically integrated buck converter that was demonstrated in chapter 4 there are other buck converter topologies that will be investigated to analyse any advantages they can provide. One of the major changes in circuit topology that can improve performance particularly in the lower output power range is by using a multi-level circuit schematic^{1,2}. This buck converter topology effectively splits up the input voltage to different voltage levels which reduces the switching node voltage and improving efficiency. The number of times the split occurs is related to the number of levels in the converter, previous work has investigated simulated systems up to 9 levels³. This shows diminishing efficiency improvements as the number of levels increases while also causing increasing fabrication complexity.

This chapter will investigate the performance of 3 and 5-level integrated buck converters. The 3 and 5-level monolithically integrated buck converters were fabricated and tested. Performance comparisons between the standard integrated buck converters in Chapter 4 and the multi-level integrated converters have been made to highlight where advantages of these topologies lie. The experimental results are also compared with the SPICE simulated results. Key differences between the simulated and experimental results on the multi-level buck converters are discussed and investigated incorporating experimental effects that can explain these differences.

5.2 – Circuit Schematics

The basic device operation principles are the same as the standard buck converter circuit. There is a power transistor switching on and off the input voltage at a required frequency and duty cycle followed by an inductor and capacitor filter to smooth the output voltage. The main difference lies with the fact the circuit has multiple ‘levels’ that control a ratio of the input voltage to reduce the switching voltage that is switched by the power transistors⁴. The two main configurations that will be investigated in this work are the 3 level and 5 level multi-level converters. The number of levels refers to the number of voltage levels that the switching node will switch between. For example, a 3-level system with a maximum input voltage of 10V will have a switching node that can switch between 10V, 5V and 0V and a total of three power transistors responsible for this. An example of a 3-level schematic can be seen below in figure 5.1.

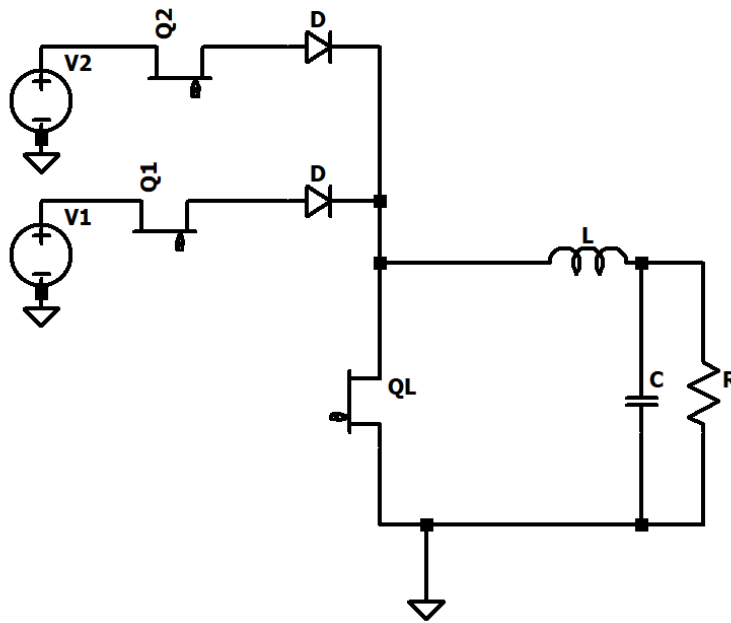


Figure 5.1: A basic circuit schematic of a three-level buck converter.

For the 5-level system it would have a switching node that switches between 10V, 7.5V, 5V, 2.5V and 0V and contain five switching power transistors. An example of the basic schematic of this system is shown below in figure 5.2.

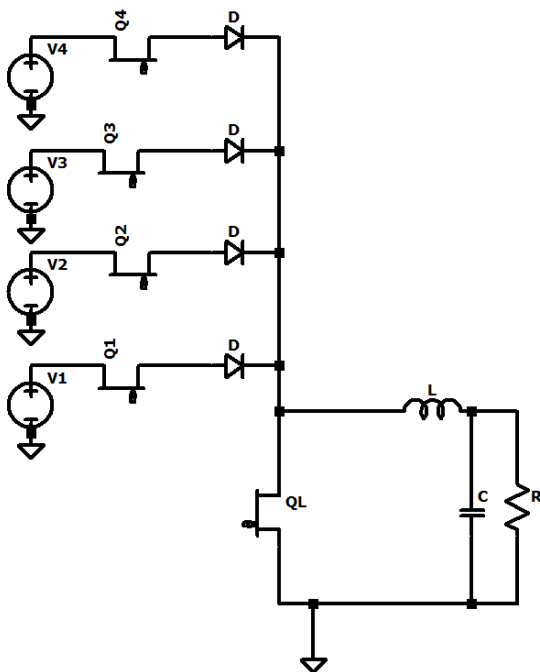


Figure 5.2: The basic schematic of a five-level buck converter.

Because of this change of both input voltage at certain levels as well as the increase in number of power transistors, the operation of this circuit is different to a standard buck converter. The key difference between the standard converter and the multi-level converter is that the multi-level converter has more than one mode of operation. The number of modes of operation is dependent on the number of levels within the circuit. For a three-level converter, there are two different modes of operation, which are referred to as high level operation and low-level operation. The three-level converter with a 10V operating voltage in Figure 5.3 shows the two switching node voltages associated with the lower-level operation and higher-level operation. The switching node voltage in this example is switched between 0 and 5V for the low-level operation and 5 and 10V for high-level operation. For the 10V operation, V1 will be set to 5V and V2 will be set to 10V each controlled by Q1 and Q2 transistors respectively. These two circuit branches are defined as the high level 'legs'. The low output operation mode functions identically to the standard buck converter operation. With the high side transistor Q1 determining the duty cycle with its on time and low side (QL) transistor switching inversely to this, Q2 is turned off during this operation mode. The higher output operation mode is where the operational differences occur. QL is turned off in this operation mode, Q1 will be turned continuously on and Q2 will be switched to determine the duty cycle and switching node voltage. As Q1 is turned on continuously, the switching node voltage ideally should not drop below the voltage set by V1, in this case 5V. Q2 then will switch, bringing the voltage at the switching node up to 10V. Due to the multiple levels of operation present in the multi-level converters, the duty cycle used for switching does not correspond to output power as with the standard converter. In the standard converter a 10% duty cycle corresponds to a 10% output voltage, however the addition of extra levels and therefore switching voltages means this is not the case with the multi-level converters. As an example of this consider a five level, three level and a standard converter operating at 10V. For an output voltage of 3V a standard converter would be switched with a 30% duty cycle. For the three-level converter however the low-level operation is used, switching between 0-5V. This means to achieve the 3V output a 60% duty cycle is needed in this operation mode. For the five-level converter it would operate between 2.5V and 5V and switch with a 20% duty cycle. Going forward in this chapter rather than referring to duty cycle a reference to the output voltage or power will be made.

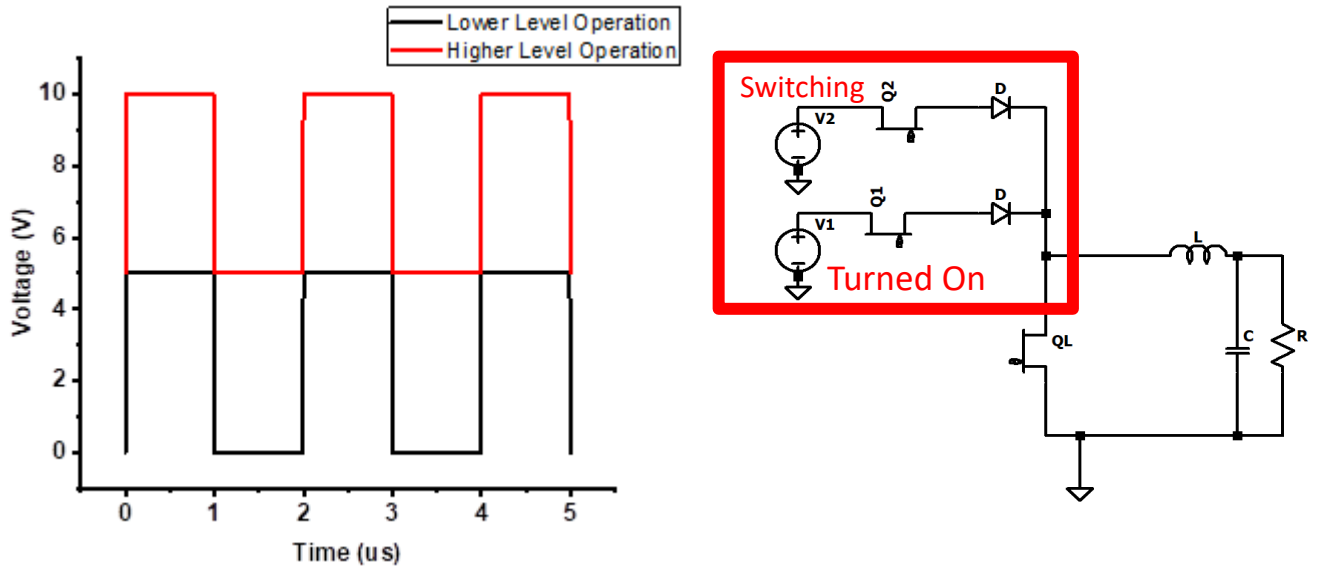


Figure 5.3: A diagram showing a three-level converter operating at 10V and the switching node voltage associated with the higher output operation.

Because of this difference in operation compared to the standard buck converter, there are several circuit level considerations that are made to both improve performance and accommodate this. The introduction of a Schottky diode is required on all the power transistors except for the low side power transistor in the circuit to prevent the switching node voltage feedback passing into the gate driver circuit of the other arms. If this occurred, it would cause damage to the gate driver transistors and prevent switching operation as the gate driver transistors are designed with a lower breakdown voltage than the switching node voltage. These diodes⁵⁻⁷ are designed to block up to 100V to prevent any overshoot causing damage to them or to allow leakage through them. The IV characteristics of a typical diode used in the circuits is shown below in figure 5.4.

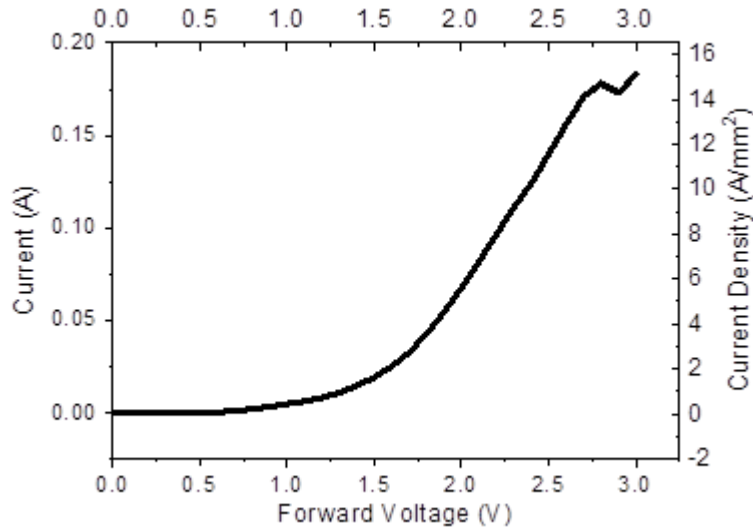


Figure 5.4: The typical diode IV characteristics for a multi-level buck converter.

Ideally the diode would have the lowest turn on voltage possible to increase the conduction current at operating voltages, shown later in simulations the losses from the diode will be shown to be large. There is a trade-off between the turn on voltage of the diode and the leakage current that will be seen within the device. An example of a diode leakage current is shown below in figure 5.5.

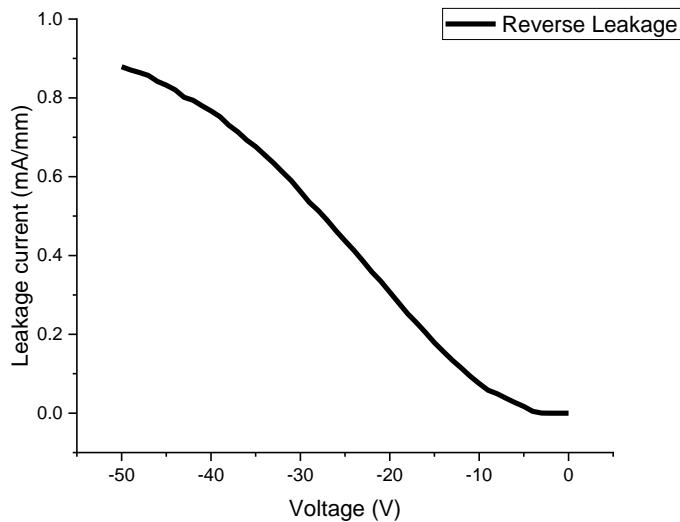


Figure 5.5: The reverse leakage current observed in the diode used within the buck converters with a voltage swept between 0V and -50V, the maximum that could be observed in normal operation.

As shown in chapter 3 section 3.3, the turn on voltage of the Schottky diode is directly linked to the work function of the Schottky metal. The lower the metal work function for the Schottky contact, the lower the forward voltage but at the expense of the device leakage current. Nickel was chosen for the Schottky diode such that the leakage current is targeted to be below 1mA/mm at -50V. If titanium was chosen as in chapter 3 to provide the lower turn on voltage, the leakage current would increase above the target set for good performance.

As in both the three and five level buck converters, the high-level legs that only provide a voltage at half the maximum or less, the source-drain spacing (Lsd) of the power transistors can be shrunk. In the Chapter 4 simulations, it was shown how using a lower Lsd in the transistor can reduce the Ron and in turn lower the conduction loss in the power transistors. This in theory should help improve the efficiency of the system at lower output power operation.

5.3 - Efficiency and Losses

The efficiency and losses throughout the circuit can be calculated mostly the same as the standard buck converter schematic and is explained in chapter 4 section 4.4. The only addition of the circuit is the usage of a Schottky diode on the high-level legs. These will introduce additional losses into the circuit, and these can be calculated from equation 5.1.

$$P_{onstate} = I^2 * R_{on} \quad 5.1$$

where $P_{onstate}$ is the on-state losses, I^2 is the current through the diode and R_{on} is the on state resistance of the diode.

The loss calculation for the power transistors in the multi-level converters is like the standard buck converter losses as described in Chapter 4. The primary difference in the loss calculations are that at higher operating voltages where two of the high side transistors are operating at the same time and the low side transistor is off. Only one of the high side power transistors is switching and the other one is constantly on, this means one of the transistors is only subjected to conduction losses and the other is both switching and conduction losses. This should reduce the operating losses of the whole circuit at higher frequencies where the switching losses will be increasingly higher.

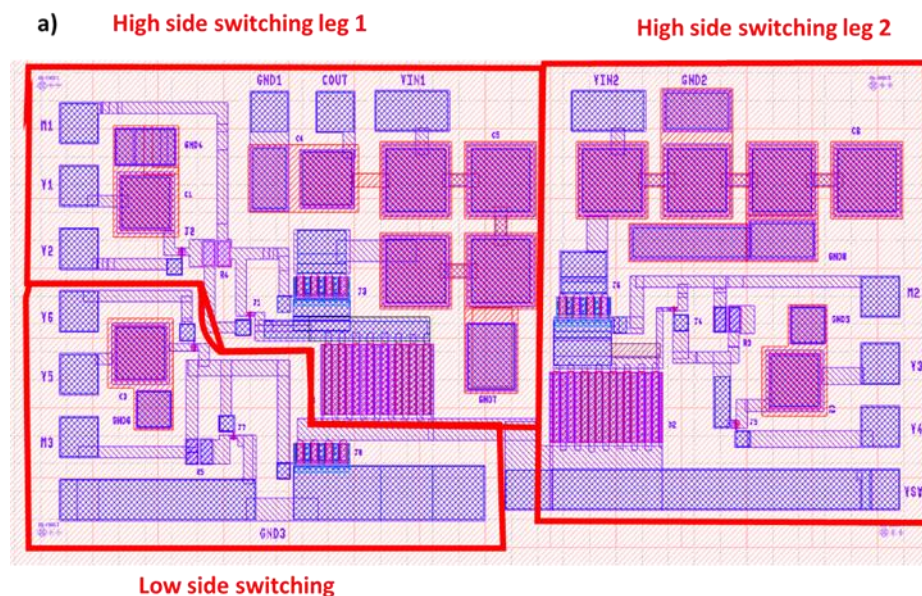
5.4 - Fabrication and bonding

The basic structure of the buck converter is like a standard device except with multiple high level transistor legs. Each with its own gate driving circuitry. This increases fabrication

complexity and requires every transistor to function correctly to be able to output power across the full range. This increases failure rate with increasing levels in the system, five level fabrications being less reliable than three level fabrications. As well as the increased fabrication complexity the size of the system increases and the number of input and outputs to the system increases.

The primary difficulty stemming from the increased complexity lies within mainly the gate driving section of the circuit. As the switching transistors are the smallest size component there. As an extra full gate driver is required for each extra level within the circuit it becomes increasingly likely for failure in the fabrication process in the three and five level circuits.

This increased complexity and size also makes the mask layer design larger and makes the chip occupy more space. Although the bonding packages selected were chosen to accommodate all the sizes of buck converter and to have enough pins to allow every connection necessary. The mask designs for both the three and five level systems are shown below in figure 5.6.



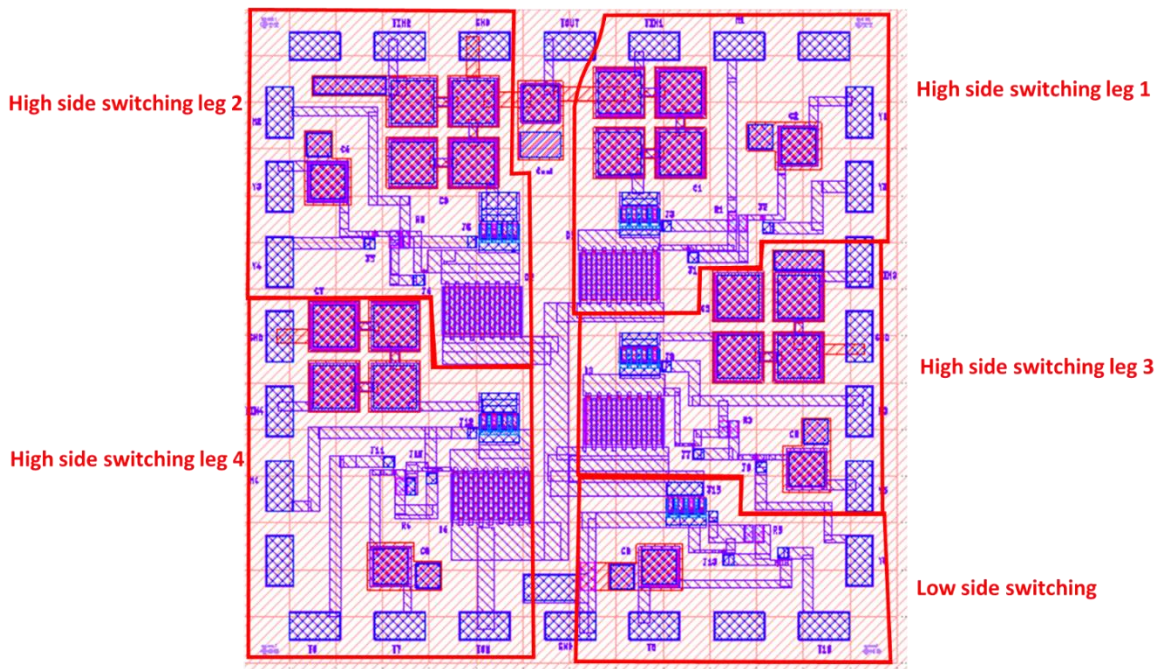


Figure 5.6: The mask designs for the a) three-level system and b) five-level system, showing the separation of each switching leg within the buck converter circuit

The mask layout is designed to spread out the system and have a continuous loop through the system for the power flow. In both the three and five level systems the power loop goes from top to bottom with the V_{in} pads as close to the top as possible and the switching node voltage at the bottom. The gate driver inputs, and control voltage pads are placed on the sides of the layout. This is to ensure the smaller high speed voltage signals fed into the gate drivers are not subject to interference from the higher voltage.

The fabrications remain the same as the process used in the standard buck converter outlined in Chapter 4 section 4.5. This is because the process used fabricates all the variations and testing devices on the same wafer of size 35x35mm.

The bonding process is fundamentally the same, gold wire bonds⁸ are made between the package and the output pads on the circuit. The package used is the CQFN LCC02834 package with gold connections and 28 output pins. The three level circuits are soldered into the package to allow reuse of these. The five level circuits are fixed into the package using gold epoxy as the package is unable to be soldered into the package due to its size. Gold epoxy is placed onto the base of the package, the chip on top then baked at 180⁰C for one hour to solidify the epoxy and provide a good connection to the package. The bonding of the devices is more complex than the standard buck converter with the three level converter requiring 15 bonds and the five

level 24 bonds. The bonded and packaged devices for the three and five level converters are shown below in figure 5.7.

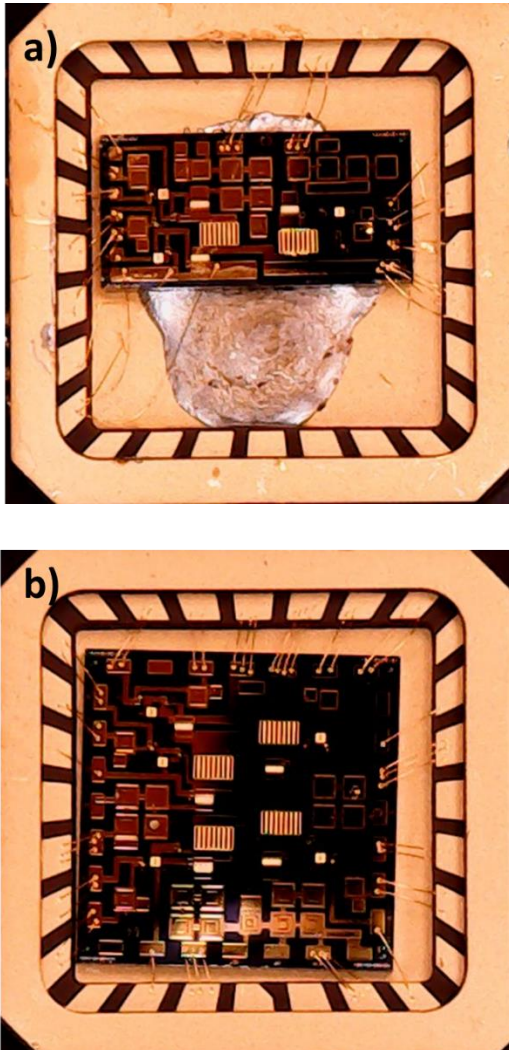


Figure 5.7: A photo of the fabricated devices bonded in a QFN package ready for testing a) three level bonded device and b) five level bonded device

As the gate driver of the circuit is the same schematic and design as the standard buck converter the signal as fed through each stage can be seen in chapter 4 section 4.5.

5.4 - Testing Circuitry

The testing circuit design uses the ISO7760 digital isolator, a full overview is given in chapter 4 section 4.9, providing an output voltage swing of -7 to -12V that is fed into the gate driving section of the circuit. The isolator has up to 6 channels which is sufficient meaning it has enough channels to operate the five-level circuit on its own meaning the testing circuit design remains the same between the circuit levels. The bias voltage in the testing circuit remains the

same and all output connections remain the same as the standard buck converter testing circuit. The three and five level testing circuits can be seen below in figure 5.8.

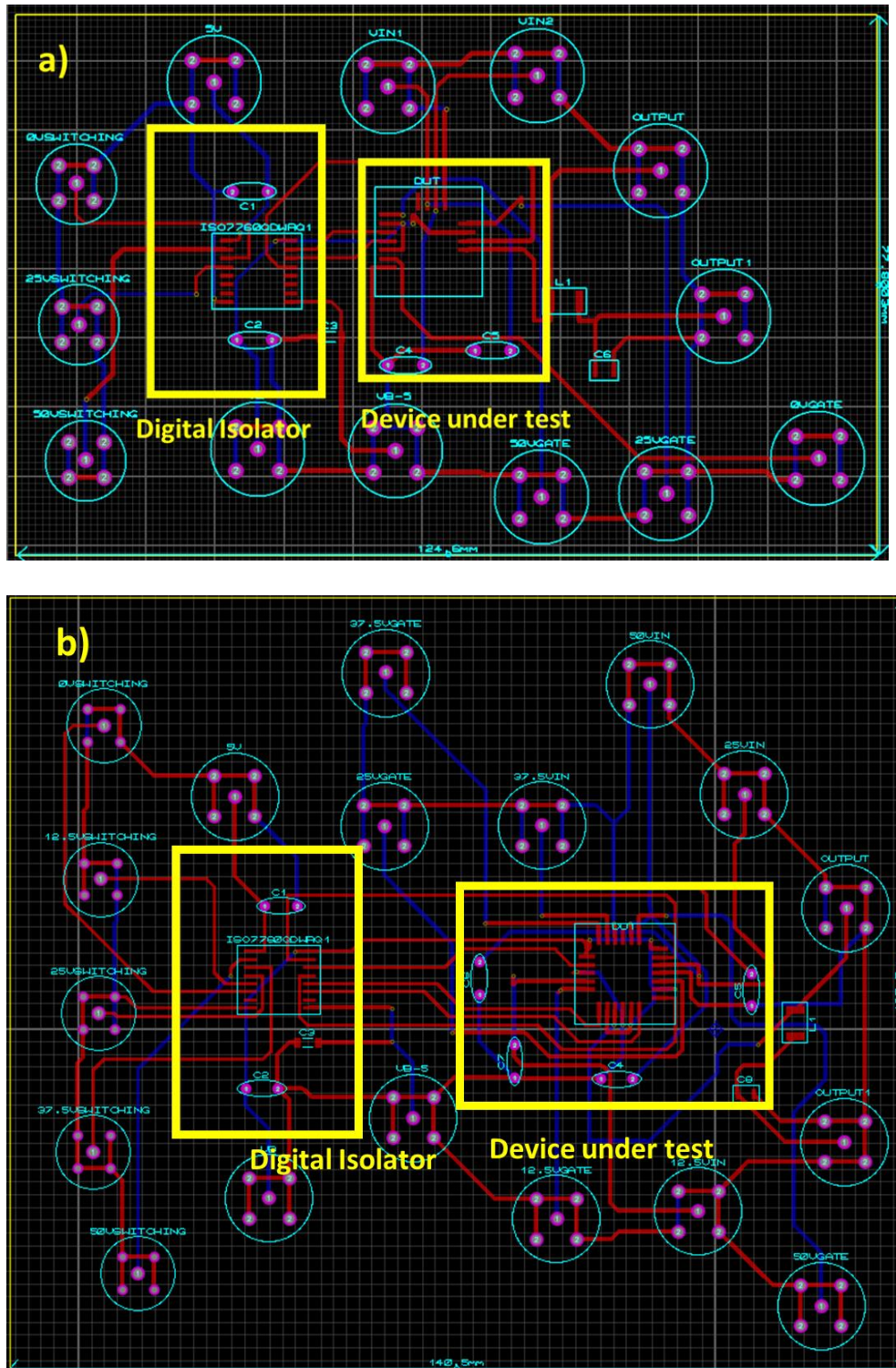


Figure 5.8: The a) three level circuit schematic and PCB and b) five level circuit schematic and PCB

The signal generation methods used for the multi-level converters are the same as that of the standard buck converter discussed in Chapter 4. The lower frequency signals at 1MHz are generated using a high speed Rigol DG4162 signal generator and the higher frequency signals at 50MHz are generated using the Intel Stratix V FPGA.

5.5 - Experimental Results

This section will break down the efficiency and losses through the multi-level circuits as well as providing a comparison with the standard buck converter. Explanations for why these advantages are present will be made as well as comparisons between this work and other similar work previously conducted will be made. Due to the increased complexity of the circuits, extraction of some component loss breakdowns will not be possible although these will be covered in the next section examining the simulations of the devices.

The same operating voltages and switching frequencies of operation are used in testing the multi-level buck converter as in Chapter 4 to allow a full comparison across a range of operation parameters. The same DC power supplies and oscilloscopes are used with the addition of one extra DC power supply to provide the input to the high levels. This is required as at higher switching node voltages two different input voltages are required to correctly operate the circuit.

5.5.1 – Three Level buck converter at 10V, 1MHz

The testing set-up and conditions for the three-level converter are similar to those of the standard buck converter at 10V, 1MHz. Due to the limitation of the testing circuitries, the duty cycle used in the standard buck converter is between 20% and 75% in Chapter 4. However, due to operating nature of the three-level converter, it is possible to provide a wider range of the output power compared to the standard buck converter despite the limitation of the testing circuitries on the duty cycle.

The switching node of the power transistors is either operating in ideal circumstances between 0 and 5V or between 5 and 10V. There is still a voltage drop that occurs across the diode and power transistors due to R_{on} which reduces the efficiency of the circuit. Figure 5.9 shows the switching node voltage of the three-level buck converter. As can be seen, the voltage drop in the switching node is in excess of 1V. This is caused by the forward voltage of the Schottky diode.

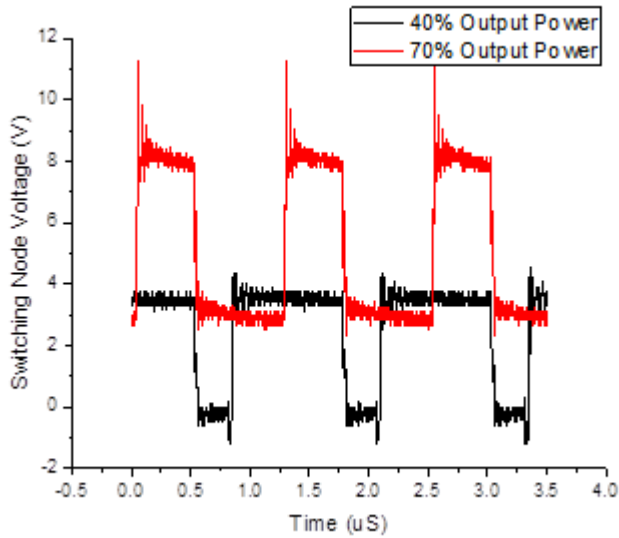


Figure 5.9: A three level converter operating at 40% and 70% output power.

This is shown in figure 5.10 presenting the total efficiency of the circuit across a range of output powers. 50% output power is missing as in the operation of this circuit it would just be a fixed input voltage with no switching due to the voltage of the levels.

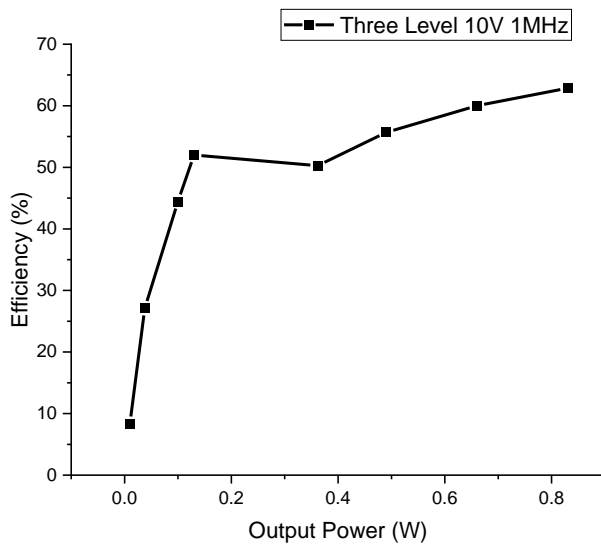


Figure 5.10: The efficiency of the three level converter against output power operating at 10V 1MHz.

It is noted that the efficiency of the three-level buck converter is lower compared to that of the standard buck converter in Chapter 4. This is primarily due to the large forward voltage of the Schottky diode, which is a larger proportion of the total switching voltage. This will be

explained further in the simulation section and separation of the losses in the transistors and diode in the circuit will be analysed. Separation of these losses is not possible with the experimental data as there is no measurement point between the transistors and diode in the integrated circuit. Losses for the transistors and diode have been grouped together and the inductor losses are separated out. A breakdown of the losses is shown in Figure 5.11. This is more pronounced at lower input voltages and results in a lower efficiency at lower output powers in the multi-level circuits. This primarily stems from the addition of the diode present in the circuit resulting in a $\sim 1V$ drop across it. This remains constant regardless of the input voltage so will have a smaller effect on the overall efficiency at higher input voltages which will be shown when 25V input is examined.

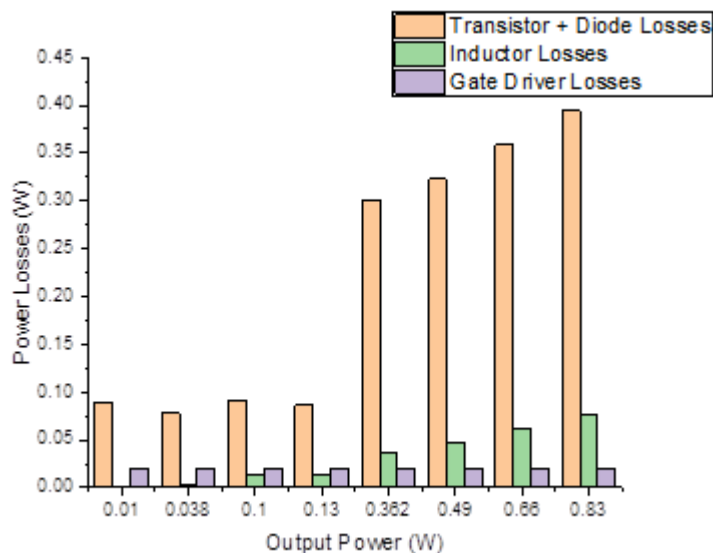


Figure 5.11: A breakdown of the losses in each component in the three level buck converter at 10V 1MHz across the range of output powers.

The same inductor was used as in chapter 4 with a series resistance of around 5 ohms for the loss estimations, and the gate driver within the circuit again has a constant power loss across the range of duty cycles used.

5.5.2 – Five Level buck converter at 10V, 1MHz

Following this, the same testing was performed on the five level converter. The same testing signal generation was used and the output power range was again varied from 10% to 90%. Operation levels in this converter are 0 to 2.5V, 2.5 to 5V, 5 to 7.5V and 7.5 to 10V, giving

five separate voltage levels that the switching node can be at. The switching node voltage at each of these voltage switching transitions can be seen in figure 5.12.

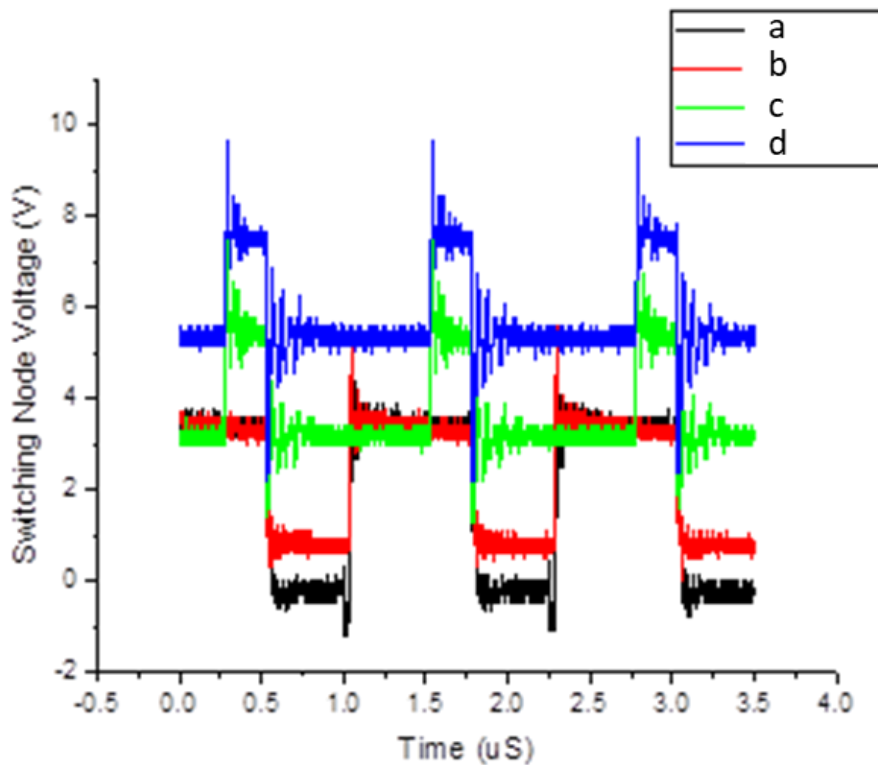


Figure 5.12: The switching node voltage with output powers at a) 10% b) 30% c) 60% d) 80%.

As can be seen in Figure 5.12, similarly to the three level converter results, the switching node voltage drop is above 1V for each of the switching transitions. The voltage drop seen at the switching node leads to poor efficiency in the five-level buck converter. This can be seen in the extracted efficiency of the circuit against output power presented below in figure 5.13.

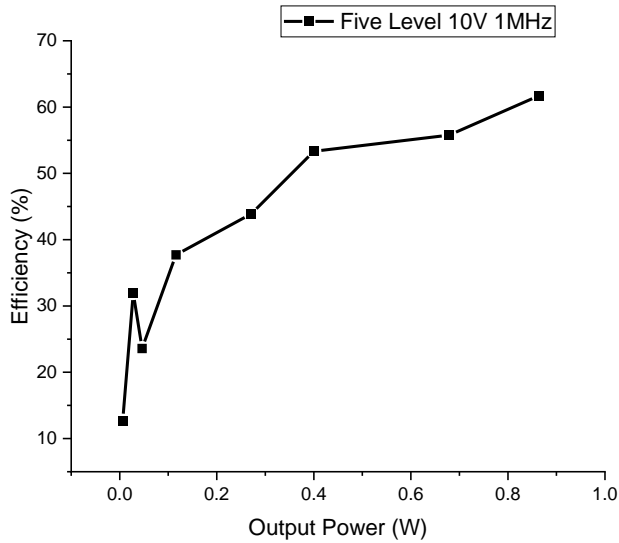


Figure 5.13: The efficiency of the five level converter circuit across a range of output powers operating at 1MHz 10V.

To understand the main contributor of the losses in the circuit, a breakdown of the losses of the components is presented in Figure 5.14. The losses share a similar proportion as the three-level circuit with the vast majority of losses coming from the power transistor and diode as expected, based on the voltage drop measured at the switching node.

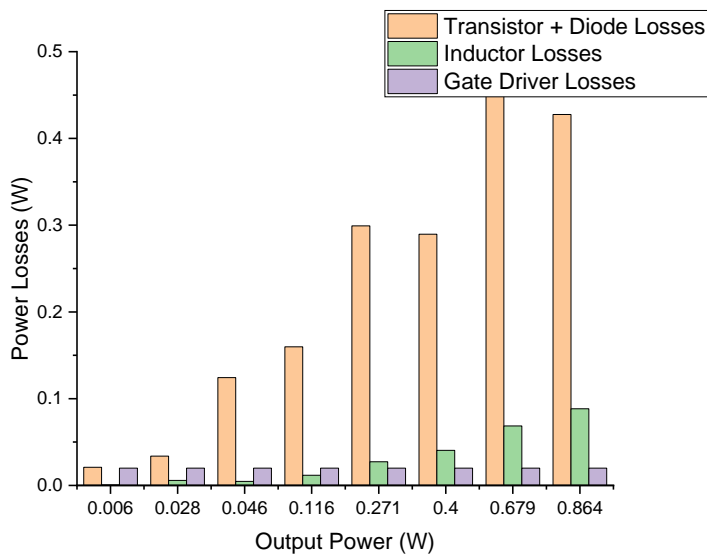


Figure 5.14: A breakdown of the losses in the five level circuit operating at 1MHz 10V.

The improvement in the efficiency is not observed when comparing the multi-level converter with standard buck converter schematic at this frequency and input voltage. A comparison between the three buck schematics is shown below in figure 5.15. As can be seen at these operating conditions, the standard buck converter is more efficient across every output power. This is primarily owing to the lack of a diode in the high side of the standard buck converter. Further loss analysis will be performed in the circuit simulations in Section 5.7.

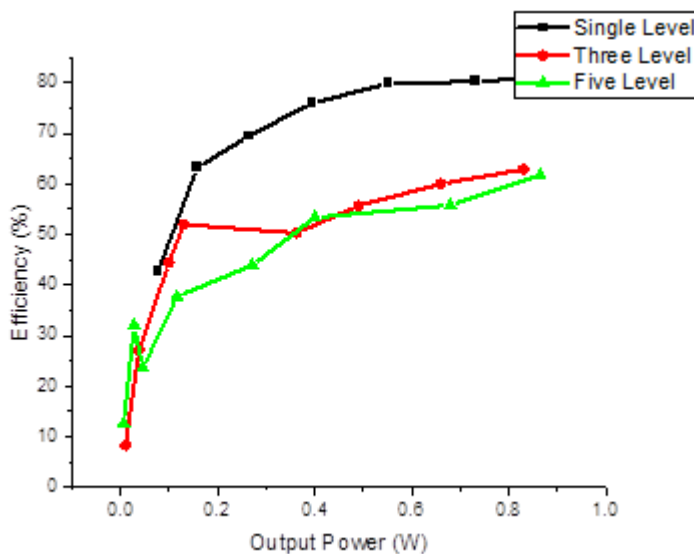


Figure 5.15: The efficiency comparison between the standard buck converter, three level buck converter and five level buck converter at 1MHz 10V.

5.5.3 – Three Level buck converter at 25V, 1MHz

The three-level buck converter circuit was also tested at 25V with 1MHz switching frequency, a higher voltage than previously tested and the same voltage level as the standard converter. The same gate driving signals that were used in the 10V tests were used for these tests so output powers between 10 and 90% were performed. The two-switching node operational voltages for the 25V 1MHz operation are shown in figure 5.16.

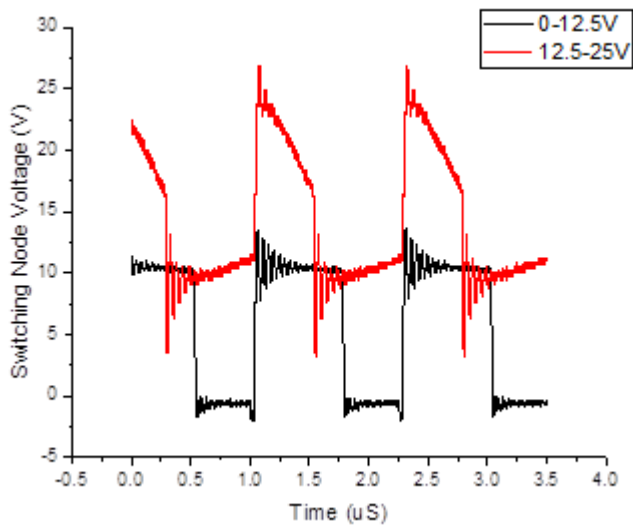


Figure 5.16: The switching node at 30% and 70% output power for the three level converter at 25V 1MHz.

At 25V, the higher power in the circuit results in the heating effect more prominent compared to the 10V operation. This can be observed in the roll-off the switching node voltage during high level operations in Figure 5.16. In the lower power operation mode (between 0 and 12.5V), the roll-off in the switching node voltage is not observed due to reduced heating effect.

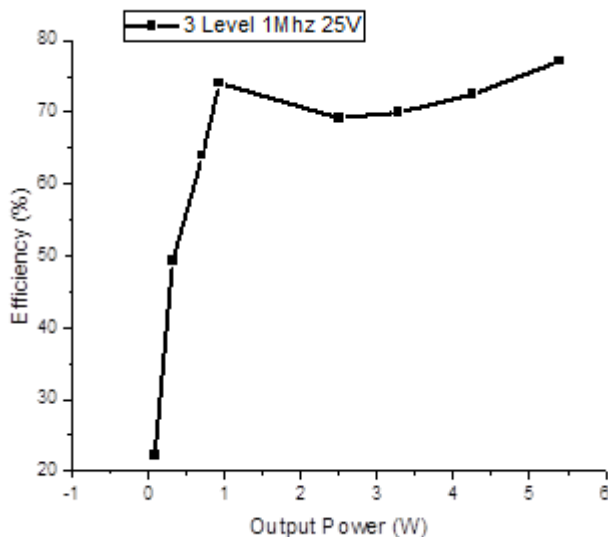


Figure 5.17: The overall efficiency of the circuit when operated between 10-90% output power.

The overall efficiency of the circuit between output power of 0.1W and 5.4W was collected and is shown in Figure 5.17. The level of efficiency in at the 25V operation is more in line with

what should be expected. A rapid increase in the efficiency at low output powers show where the primary advantage of employing a multi-level design comes in. The small dip in the efficiency between 1 and 2W output power is observed in Figure 5.17. This is due to the switch from low level to high level operation modes in the multi-level buck converter as expected.

The breakdown of the component losses has also been performed. This is shown in figure 5.18.

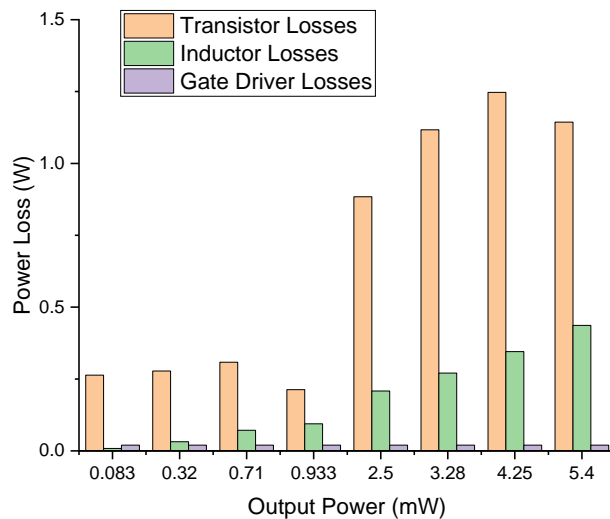


Figure 5.18: A breakdown of the losses in the three-level circuit operating at 25V 1MHz.

The losses primarily come from the power transistors and diodes, in which making up between 65% and 90% of the total loss, depending on the duty cycle. The inductor losses are larger in magnitude compared to the 10V operation due to the higher power of operation.

5.5.4 – Five level buck converter at 25V, 1MHz

The five-level converter testing at 25V 1MHz used the same testing setup as the three level. 10-90% output power switching signals were fed from the signal generator to the gate driver of the circuit. Similar to the three-level testing circuit the four level transitions at the switching node have been presented in figure 5.19.

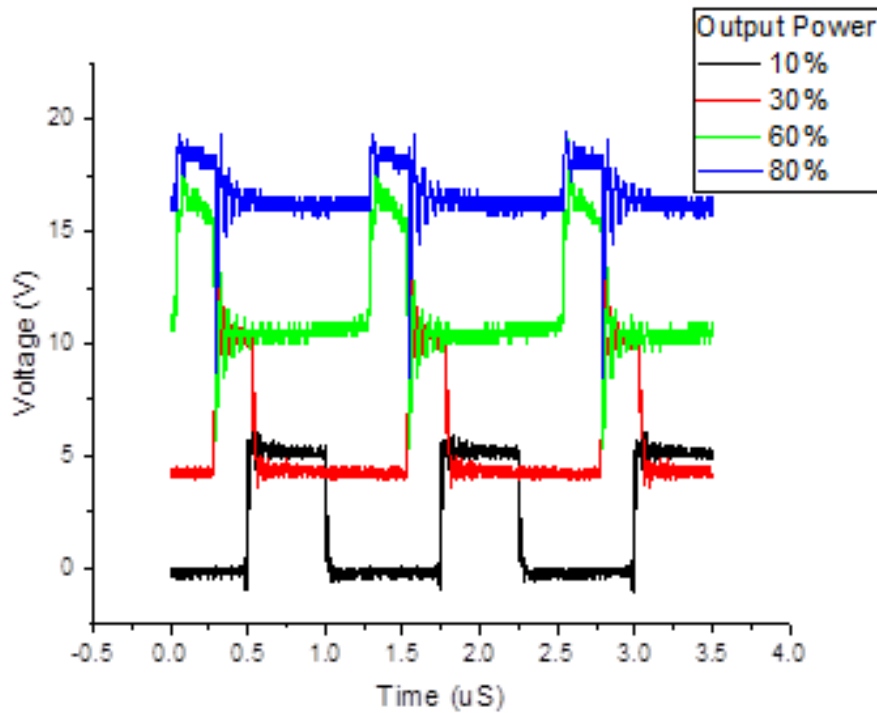


Figure 5.19: The five-level converter switching node voltage levels at 25V 1Mhz for a) 10% output power b) 30% output power c) 60% output power d) 80% output power

The turn on and turn off times for each operation are shown in table 4.

Output Power	Turn on time	Turn off time
10%	23ns	16ns
30%	25ns	16ns
60%	27ns	13ns
80%	16ns	8ns

Table 4: The turn on and turn off times at the switching node for the five level converter

These are similar to both the three level and the standard buck converter switching times at 25V presented in Chapter 4.

A figure the efficiency across a range of output powers is shown in Figure 5.20.

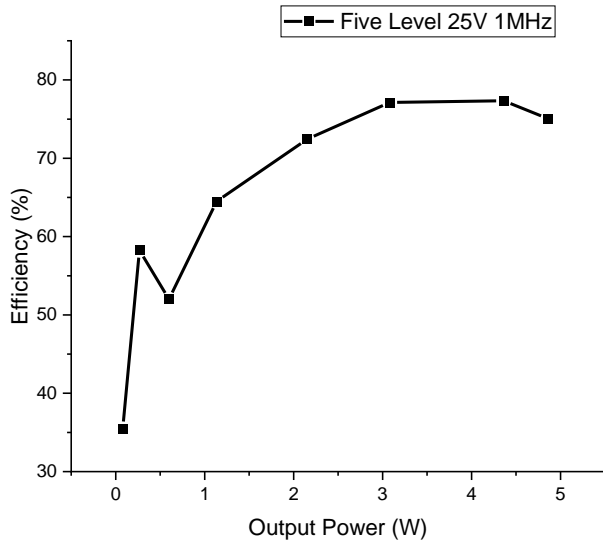


Figure 5.20: A figure showing the efficiency of the five level buck converter against output power operated at 25V 1Mhz.

The efficiency in the five-level converter is very similar to the three-level converter varying between 35% and 77%. The efficiency increase starts at the lower output powers, however, as should be expected with the increase in levels in the circuit and therefore a decrease in the switching node voltage. At a very similar power out around 0.08W the three-level converter shows a 22% efficiency compared to a 35% efficiency for the five level converter. In addition, the top end of the output power efficiency is slightly higher than the three level and reaches that peak at a lower output power than the three level converter. The breakdown of the losses in this setup is shown below in figure 5.21.

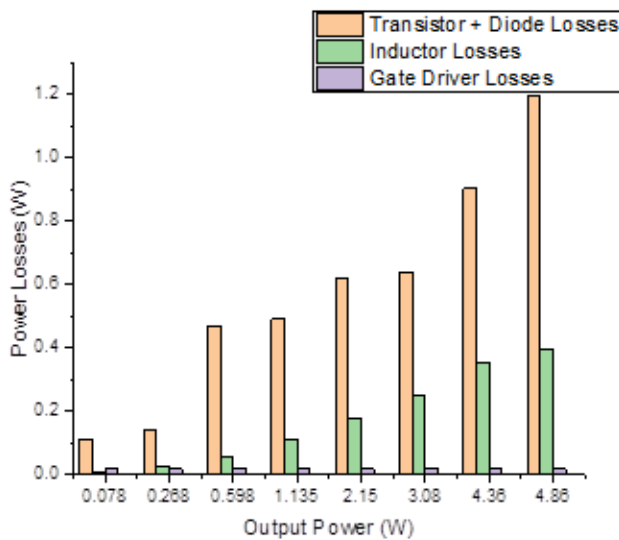


Figure 5.21: A breakdown of the losses in the five level converter at 25V 1Mhz

Consistent with the other configurations the losses through the power transistor and diode are the majority of the losses between 0.078W and 4.86W. The loss distribution is very similar to the three level configuration if only slightly lower. This suggests that at even higher voltage operation the five level advantages would become even more prevalent as the diode losses contribute less to lower power operation.

A full comparison at 25V 1Mhz operation is then made between the three circuits. The plot of the efficiency over output power is shown below in figure 5.22.

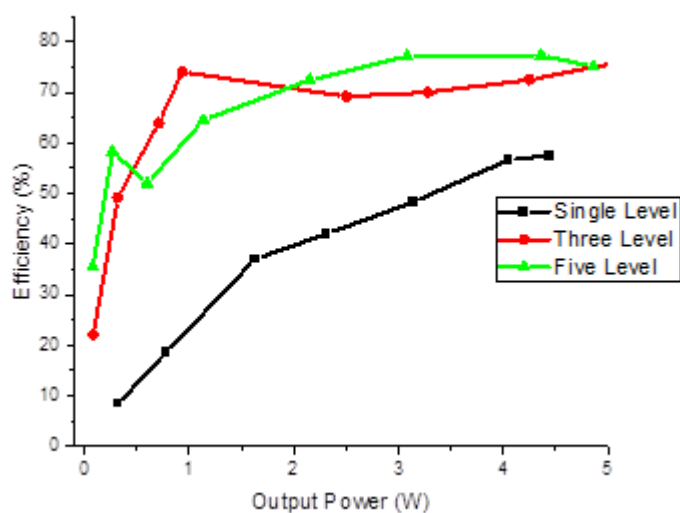


Figure 5.22: A plot of efficiency over output power for the standard, three level and five level buck converter.

This plot clearly illustrates the advantages in efficiency the multi-level converters have over a standard converter. The largest increase in efficiency at lower output powers is present for both multi-level converters although the reduction in losses is present across the whole output power range. Varying between a 13% and 45% efficiency advantage between the standard and the three level and 3% and 13% between the three level and five level considerations of yield and circuit complexity vs efficiency increase should be considered when designing the converters. Additional levels added to the converter would be expected to increase efficiency even further although as can be seen the jump from a standard to a three level is much larger than between the three and five level.

5.5.5 – Three Level 10V 50MHz

The following experimental results are concerned with a higher frequency of operation at 50MHz the same as the previous testing on the standard buck converter. Again, this has been performed at 10V and both new configurations will be analysed and compared to the previous results. The first analysis is done on the three-level circuit operating at 50MHz 10V, with the signal generation being performed by the FPGA using the same signals shown in chapter 4 section 4.8.2.

Similar to the standard buck converter the turn on and turn off times are a much larger ratio of the total signal time at this frequency. Owing to mostly the poor signal generation from the FPGA although the slow switching of both the digital isolator and gate driver will also have an effect. The turn on and turn off time at the switching node are 8ns and 7ns, and the circuit never reaches the maximum voltage due to the poor slew rate leading to much larger losses than in ideal operation. Worse efficiency across the range of output powers is a fallout from this and can be seen below in figure 5.23.

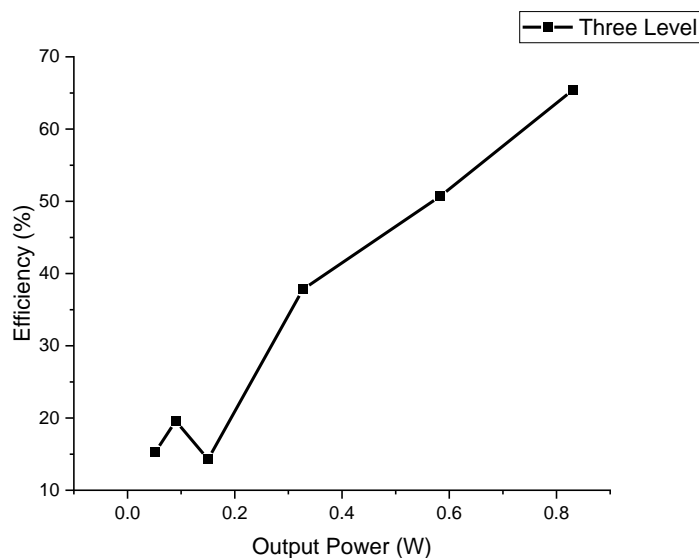


Figure 5.23: A breakdown of the efficiency across a range of output powers for the three level converter operating at 50MHz 10V.

A plot of the two frequencies of operations is shown below in figure 5.24 for easy comparison. The efficiency at this operating frequency ranges from 15% to 65%, lower than that of the 1 MHz measurements at 10V. The slightly higher efficiency in the 50MHz operation is presented at the highest output power but is only a marginal increase and could be within a margin of error for the device.

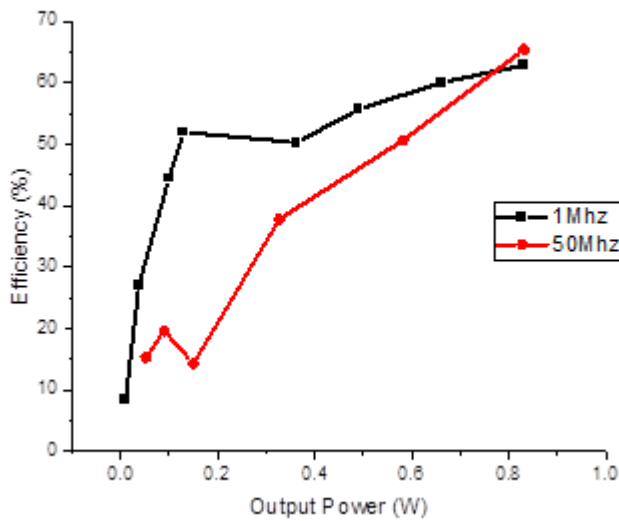


Figure 5.24: A comparison of the three level converter operating at 1Mhz and 50Mhz 10V.

A breakdown of the losses for this configuration is shown below in figure 5.25 for 50Mhz 10V operation.

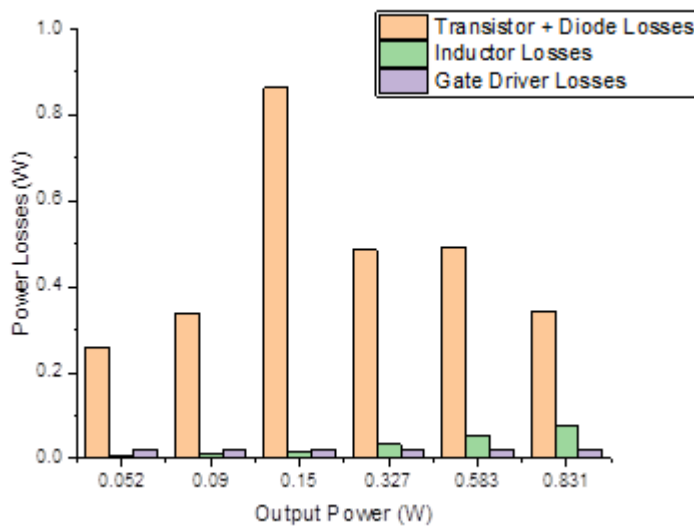


Figure 5.25: The loss contribution in a three level converter operating at 50Mhz 10V.

The majority of the losses again come from the power transistor and diode combination, although it can be assumed that in this configuration the switching losses will be much larger due to the poor switching signal as shown in chapter 4 section 4.11.3 as the same switching signal setup was used.

5.5.6 – Five Level 10V 50MHz

Following this the five level converter was characterised at these operation parameters. The same signal generation method was used as previously documented and the FPGA generated signals are the same ones used to characterise the standard converter and the three level converter. The switching node voltages for each separate operation mode are shown below in figure 5.26.

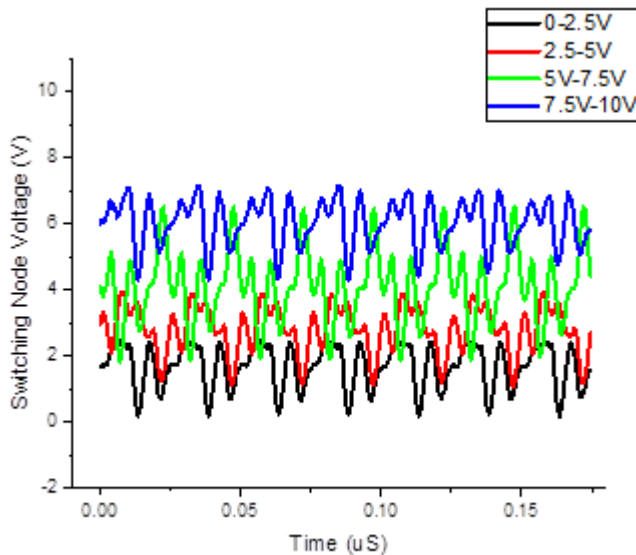


Figure 5.26: The five level converter operating at 50Mhz 10V switching node voltage between a) 0-2.5V b) 2.5-5V c) 5-7.5V and d) 7.5-10V.

This shows both the poor switching times in the circuit as well as the voltage drop caused by the diode in each of the high-level legs of the circuit. Quantifying the turn on and off times for each of the switching nodes is extremely difficult as the signal never reaches the maximum voltage the signals appear closer to sin wave signals rather than digital ones. The efficiency breakdown across the range of output powers for this setup is shown below in Figure 5.27.

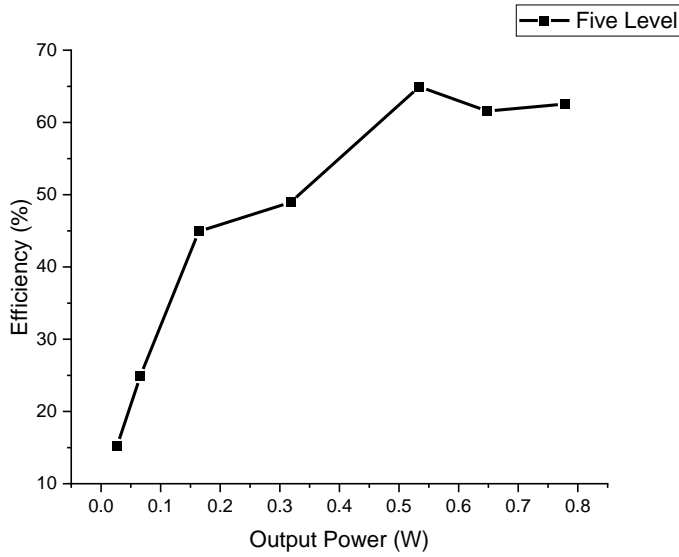


Figure 5.27: The efficiency breakdown of the five level converter across the range of output powers operating at 50Mhz 10V.

The efficiency breakdown shows a slight increase in efficiency particularly across the lower output power ranges compared to both the three level and the standard converter operating at this configuration. The top end of the efficiency remains constant at a similar value to the three level converter. A comparison between the three configurations is shown below in figure 5.28.

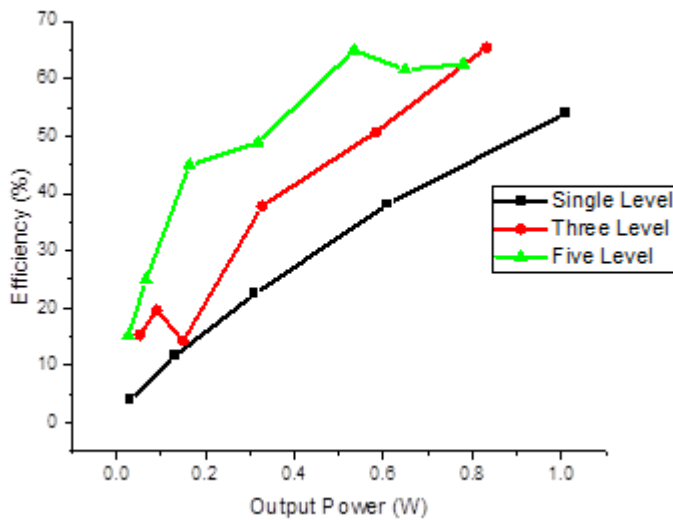


Figure 5.28: A comparison between the standard, three-level and five level converters operating at 50Mhz 10V.

Even though the overall efficiency numbers are much lower than the ideal efficiency shown in the later simulations the general trend of all three of the converters is as expected. The multi-level converters showing an increased efficiency primarily at lower output powers due to the improved switching losses and lower switching node voltage

The breakdown of the losses for the five-level converter is shown below in figure 5.29.

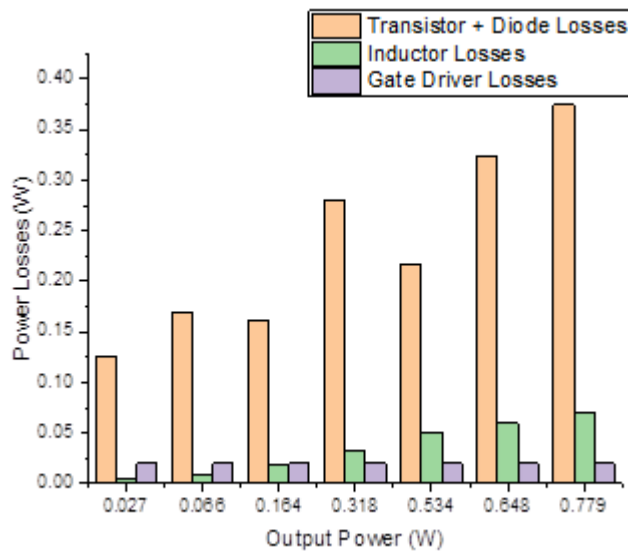


Figure 5.29: The breakdown of the five level converter losses operating at 50Mhz 10V.

Consistent with all the other experimental results the power transistors and diodes provide the main contribution of the losses and inductor losses and gate driver losses remain consistent with previous configurations.

Although high efficiency targets above 80% have not been achieved the comparison between the setups shows how the topological changes can bring about improved performance and increased efficiency. Particularly when investigating higher output powers and more specifically the 25V input. A more complete breakdown of the circuits and particularly the losses in each component will now be done with simulations based in LTSpice.

5.6 Simulations

The simulations of the circuit schematics were performed using LTSpice and the transistors use the same model as defined in chapter 4 to allow for comparisons between the standard results and multilevel results.

The only difference is the addition of the diode in these circuits, which is designed to match the experimentally measured device performance. As they are fabricated on the same wafer and with the same metals for the ohmic stack and Schottky contact they are similar in performance to the transistor. The turn on of the diode is set to 1.1V however the R_{on} of the device is much lower than the power transistors owing to larger area and is set at 1.3ohms, the output capacitance is set to 20pF. The diodes are placed on each leg of the high side of the circuit, the three level and five level schematics including gate drivers are shown in figure 5.1.

The rise and fall times for the input signals in the simulations are set to match with the experimentally generated test signals as performed in the simulations of Chapter 4. This will allow accurate extractions of the component losses and the share of the losses between the diode and transistors, which was not extractable experimentally.

The simulations have been performed for both the three level and five level setups at the same frequencies and voltages as the experimental data. Dead times and duty cycles have been kept the same and output powers are close to the real data.

5.7 – Simulation Results

In this section of the results, it is possible to break down the component losses in the power stage of the circuit. This will help to give a better understanding of the contribution of the losses by both the transistors and the diodes. Reference will be made to each component in regard to its switching state and depends on the operation mode of the circuit and will be as follows. The high side transistor losses will refer to the transistor that is switching the highest voltage for a given operation mode. An example would be for a 7.5V output in a three-level converter the two high legs of the converter will operate, one with an input of 5V the other with an input of 10V. The high side transistor refers to the transistor switching the 10V input. The switching diode refers to the diode connected to this same leg of the circuit. The low side transistor refers to which ever transistor is connected to the lowest input voltage in operation, 5V in the example case. Or this could be the low side transistor in the case of the lowest mode of operation. The on-state diode refers to the diode connected to this leg of the circuit, although there is no diode present on this leg in the lowest operation mode.

5.7.1 – Three Level 10V 1MHz

The first stage of testing is the 10V 1Mhz operation mode of the circuits. The efficiency curve of the three-level circuit is shown below in figure 5.30.

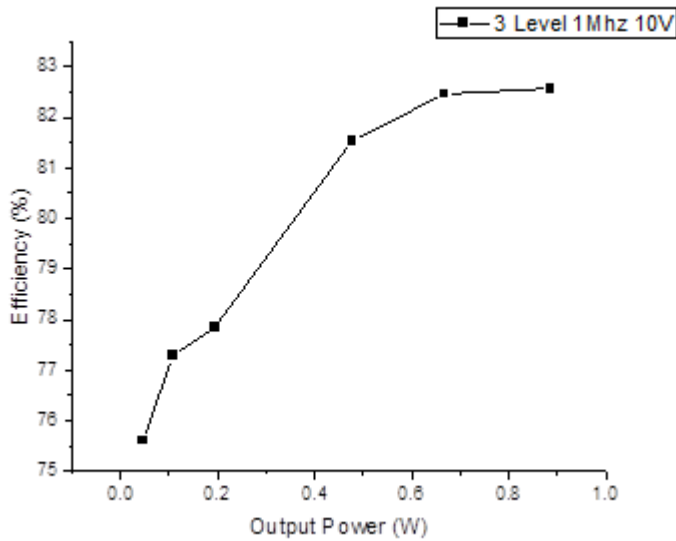


Figure 5.30: The output power against efficiency of the three-level converter operating at 10V 1Mhz

Similar to the experimental results for this setup the efficiency starts low then increases as the output power increases. Starting at 75% at 10% output power and increasing to 83% at 90% output power, the simulated efficiency is higher than the experimental results. and a breakdown of the losses will show the components that produce lower losses than the real circuits. A loss breakdown of the circuit operating in both operation modes is shown below in figure 5.31 across the range of output powers.

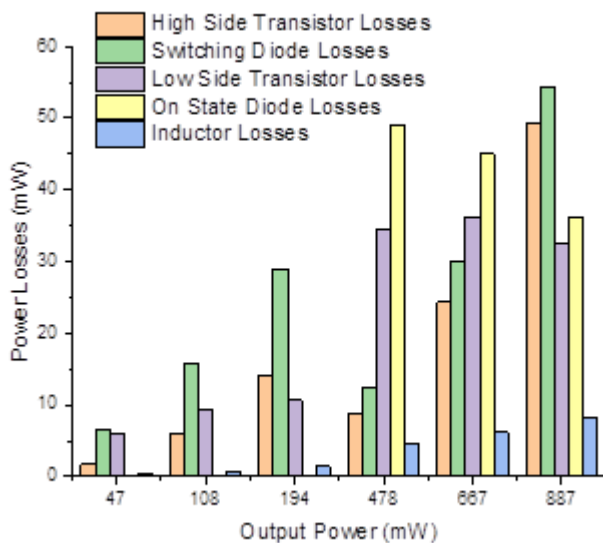


Figure 5.31: A simulated breakdown of the losses in the three-level circuit operating at 10V 1Mhz

The power transistors and diode are both the largest contributors to the total losses. Before the higher mode of operation (<50% output power), the switching diode dominates the losses owing to a high forward turn on voltage. Operation above 50% output power gives similar results with the majority of the losses coming from the power transistors and diodes. These losses are lower than the experimental results shown previously although as separation between the two cannot be done for experimental results it is not entirely evident whether the transistor or diode is mostly the cause of this. Using these simulation results for this, it appears the diodes are the biggest contributor that could be improved upon and contribute more to the total losses than the transistor. Like the work in chapter 4 there are also several reasons the transistor losses are most likely lower than experimentally. Non ideal capacitances in the real devices will lead to increased switching losses and the devices Ron will be different on a device-to-device basis so may be higher than what is set in the simulations. Bonding parasites and parasites through the packaging and PCB traces will provide resistance and reduce the efficiency. As well as this heating effects within the devices could explain the decrease in losses as in chapter 4 section 4.14.

5.7.2 – Five Level 10V 1MHz

Following this a breakdown of the five-level circuit operating in these conditions has been performed. Below is the efficiency of the circuit shown in figure 5.32.

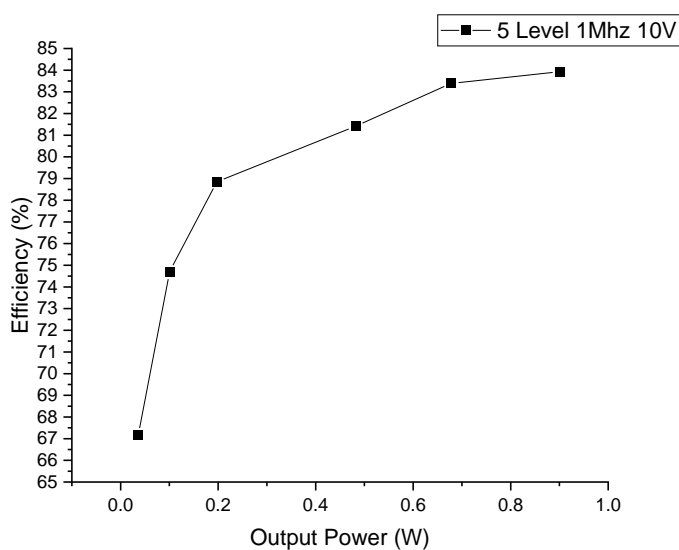


Figure 5.32: The efficiency of the five-level circuit operating at 10V 1Mhz.

In this case the efficiency starts slightly lower than the three-level circuit at 67% and increases to a higher top end of 84%. This is attributable to the high diode loss which dominating the overall losses. A breakdown of the losses in the circuit operating in all of its different operation modes is shown below in figure 5.33.

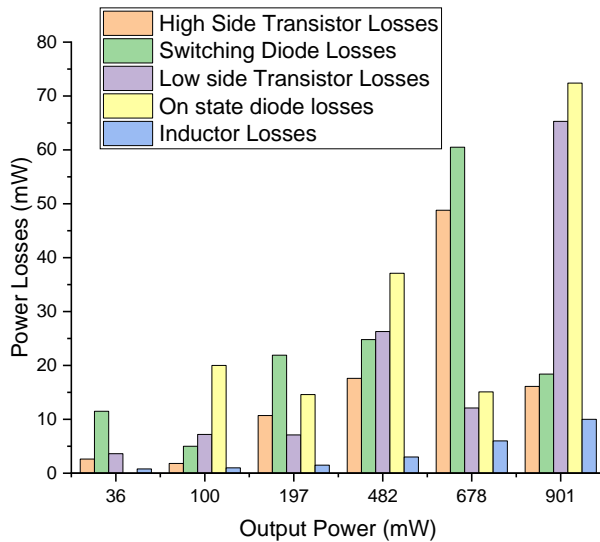


Figure 5.33: The losses shown in the five-level circuit operating at a) 20% b) 40% c) 60% and d) 80% output power.

Again, the diodes contribute a similar proportion to the losses as the transistors, showing how the extra losses introduced by them reduces the overall efficiency. The large increases in the on-state device losses is due to the different duty cycles applied to the circuit to achieve different output power level.

A full efficiency comparison between all three configurations is shown below in figure 5.34 to easily highlight the advantages the multi-level circuits can bring.

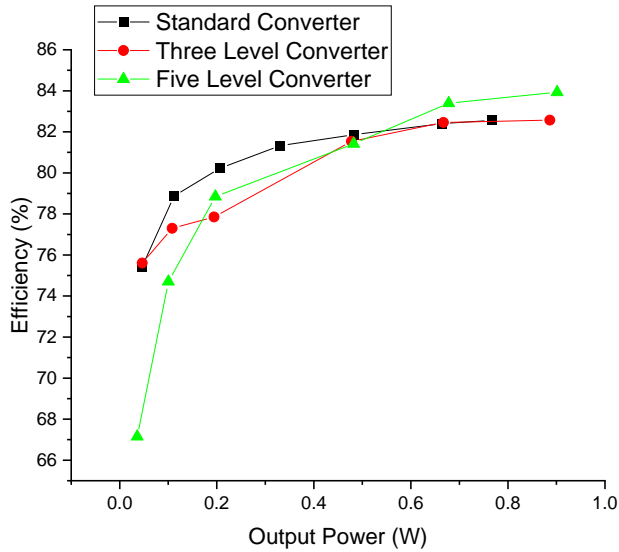


Figure 5.34: A comparison in simulations between the three configurations of buck converter operating at 1Mhz 10V.

Figure 5.34 shows the efficiency comparison between the three converter schematics and all reaching very similar peak efficiencies. As can be seen from the figures showing the individual losses in the circuit the diodes contribute a large proportion of the total losses. This means any advantage gained from having a new topology is lost through the addition of the diode at these relatively low voltage operating conditions. This also agrees with the experimental results shown previously as the 10V 1MHz operation for both the three and five level converter produce lower efficiencies than the standard converter.

5.7.3 – Three Level 25V 1MHz

The next operation mode tested was the 25V 1Mhz operation in the three-level configuration. The efficiency curve from 0.3W to 5.97W is shown below in figure 5.35.

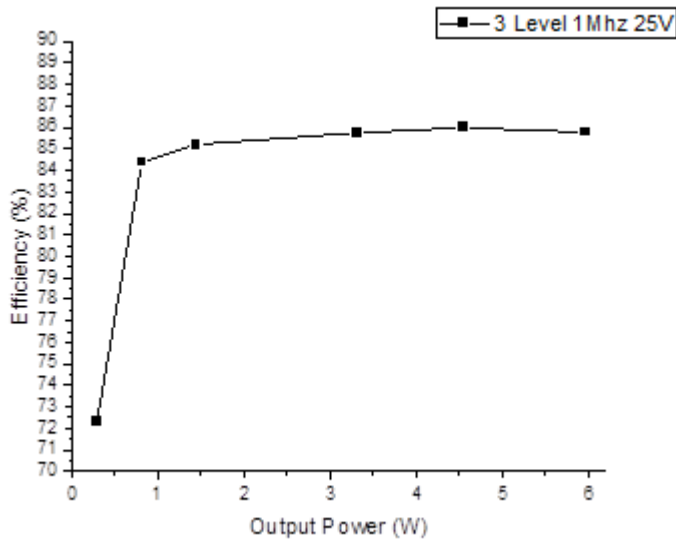


Figure 5.35: The efficiency of the three level simulations operating at 25V 1Mhz.

The efficiency is lower than 10V operation at low output powers and higher at the higher output powers. Low output power meaning the lower operational mode and high output power at the high operational mode. The following loss breakdown in Figure 5.36 again shows the three-level operating at a range of output powers across the two different operation modes of the circuit.

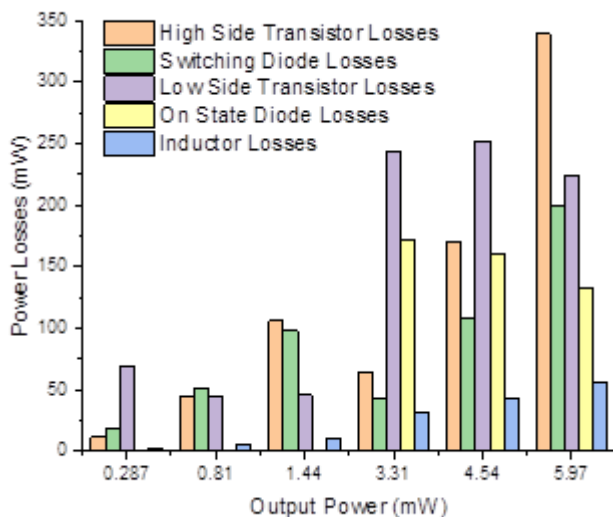


Figure 5.36: The power loss broken down by component for the three-level circuit operating at a range of output powers.

The power losses show a consistent trend with the 10V operation. The diodes being the largest share closely followed by the high side transistor. The two operation modes show a small difference in loss distribution between components. At the lower operation mode, the low side transistor dominates the power losses. In the higher power operation mode, the high side transistor dominates the power losses as the other transistor in this topology is simply switched on so is only dependant on the on-state resistance of the power transistors. As well as this, the high side power transistor will be switching but the permanently on transistor only conducts and is subject to only conduction losses. As the lower power high side transistor, Q1 in figure 5.3, is designed with a lower Lsd leading to a lower Ron within the device further improving performance.

5.7.4 – Five Level 25V 1MHz

A simulation of the five-level circuit in these operating conditions was then analysed to compare with the three level and standard buck converter topologies. The efficiency of the five-level converter is shown below in figure 5.37.

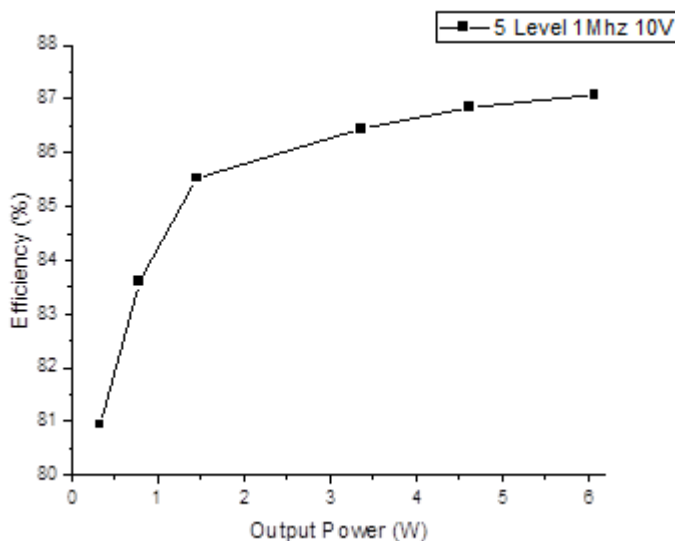


Figure 5.37: The five-level converter operating at 25V 1Mhz between 0.3W and 6.1W

The power range shown from 0.3W to 6.1W shows an efficiency change from 81% to 87% slightly higher than the previous results for the three-level topology. The loss breakdown is shown below in figure 5.38 for the four operation modes of the five-level converter.

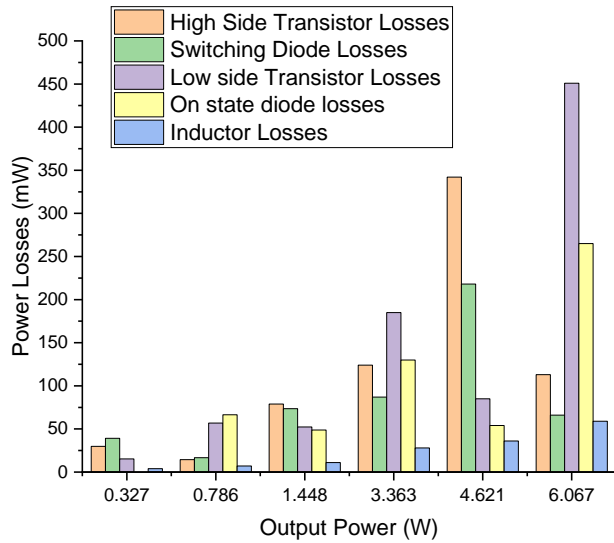


Figure 5.38: The five-level converter operating at various power levels at 25V 1Mhz.

The loss breakdown here mirrors the three-level converter with the lowest power level having the low side power transistor being the largest contributor to losses and the higher power levels having the high side transistors being the largest contributor to losses. Two of the high side transistors in the three lowest levels are a smaller size than the higher levels of operation again contributing to the lower losses due to the reduced R_{on} within the devices. The diode is a large contributor towards the total losses for each configuration which again remains consistent across the multi-level circuit configurations.

A comparison of the three converters operating in this configuration is shown in Figure 5.39.

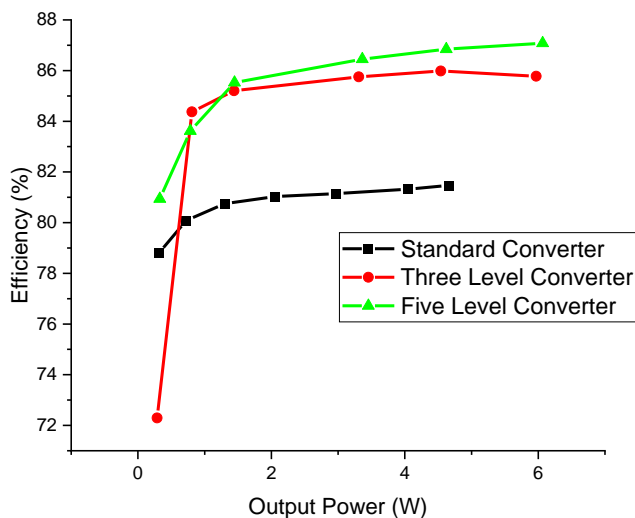


Figure 5.39: A comparison between the three simulated converter topologies operating at 25V 1MHz

At this voltage level the advantages the converters can bring begins to become clearer. Both the three and five level converters rapidly overtake the standard converter in terms of efficiency at low output powers then maintain this efficiency improvement up to the maximum output power in the system.

5.7.5 – Three Level 10V 50MHz

Next, the higher frequency simulations are performed at 50MHz for both circuit configurations to allow comparison with the experimental results. The three-level circuit is operated at 50MHz with a 10V input voltage and the efficiency of the circuit between 0.05W and 0.9W is shown below in figure 5.40.

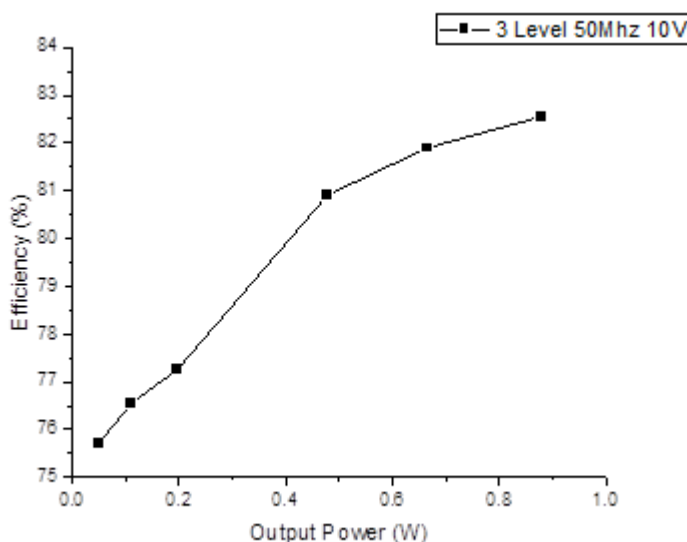


Figure 5.40: The three-level circuit operating at 50MHz 10V for a range of output voltages.

The efficiency is much higher than the experimental results, around 11% higher. As well as the previously outlined advantages the simulations bring about that provide this increase, the signal fed to the circuit is more ideal so will further contribute to lower losses.

A breakdown of the losses in the circuit is shown below in figure 5.41.

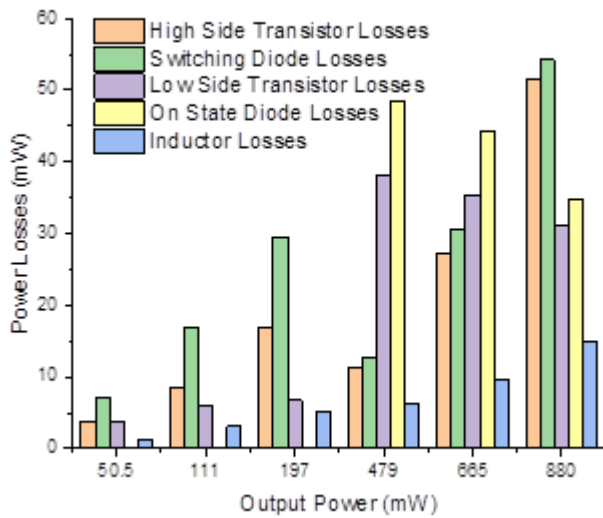


Figure 5.41: The breakdown on the losses in the three-level circuit per component operating at 50Mhz 10V.

The magnitude of the component losses is lower than experimentally found but again is explained by the poor switching signal used for all 50MHz testing. This was outline in chapter 4 section 4.14 where it has been demonstrated that the simulated circuits when operating with the experimentally measured 50MHz signal produce similar efficiencies.

5.7.6 – Five Level 10V 50MHz

The five level simulations at 50MHz were then created and the efficiency is shown below in figure 5.42.

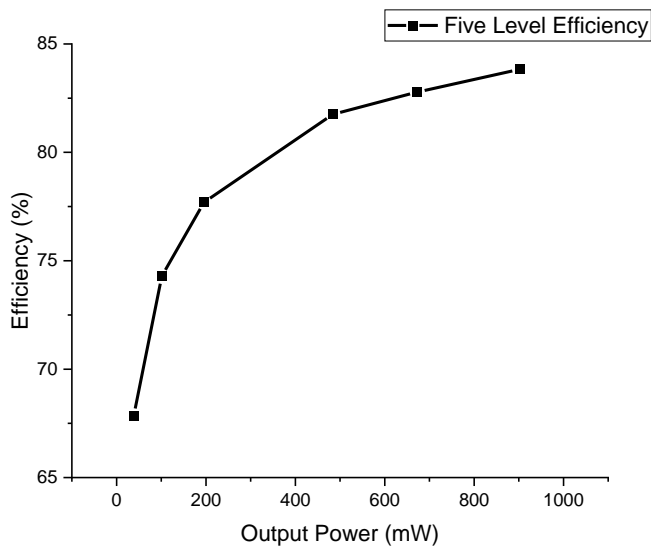


Figure 5.42: The efficiency of the five level circuit simulated at 50MHz 10V.

The loss distribution was then simulated for each component and again is shown below in figure 5.43.

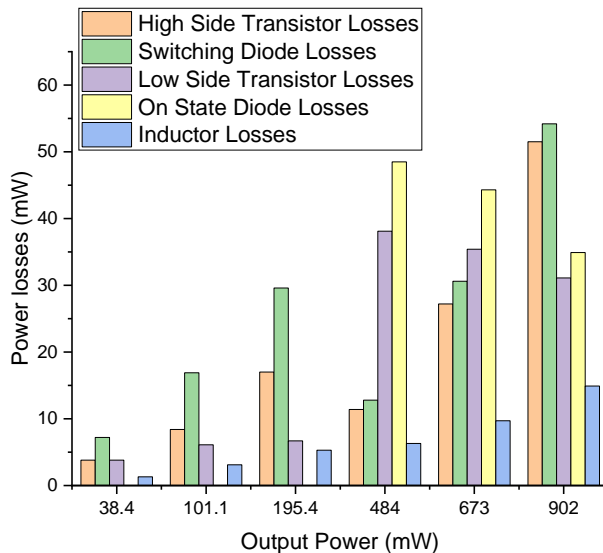


Figure 5.43: The breakdown on the losses in the five-level circuit per component operating at 50Mhz 10V.

Again, this setup follows the trend observed with the three level converter. Lower loss magnitudes which again is attributable to the better switching signal. Figure 5.43 shows the distribution of power losses for each operation of the circuit. Increasing switching losses in the high side components as the output power increases. Then the sudden drop in power as the next operation stage is started and the switching duty cycle decreases.

A comparison of the three converters operating at 50MHz 10V is shown in Figure 5.44.

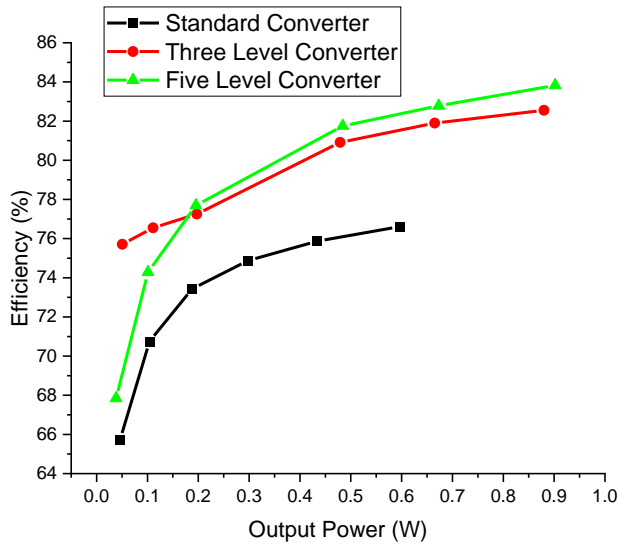


Figure 5.44: A simulated efficiency comparison between the three converter topologies operating at 10V, 50MHz.

This shows an improvement in the efficiency that can be attained by the three and five level converters even when operating at higher frequency.

5.7.7 – Three Level 10V 1MHz Experimental Comparison

These simulations however show the ideal operating conditions of the circuit at 50MHz when the heating effects^{9,10} play a large part in the poor performance. As such the following three level simulations were repeated heating effects adjusted to be the same as in chapter 4 section 4.14.1. This enables a clearer insight into how much this is affecting the overall efficiency and whether these ideal targets set by the simulations are achievable by the circuit and the components that are currently able to be fabricated. Figure 5.45 below shows the new simulated efficiency across a range of output powers.

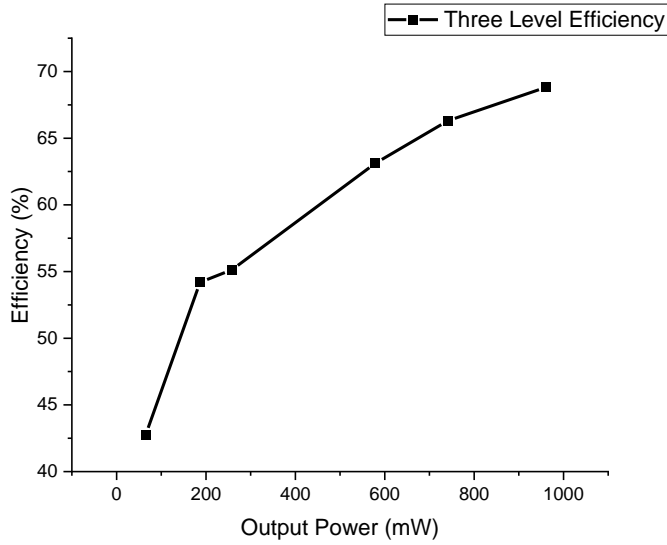


Figure 5.45: The simulated efficiency of the three level converter circuit when operated with the experimental switching signal.

This efficiency is much closer to the measured performance of the circuit with peak efficiencies of 68% compared to 65% in the measured circuit. The slightly higher efficiency can probably be attributed to the heating effects within the experimental circuit as these have not been included in the model. The breakdown of the losses is presented below in figure 5.46.

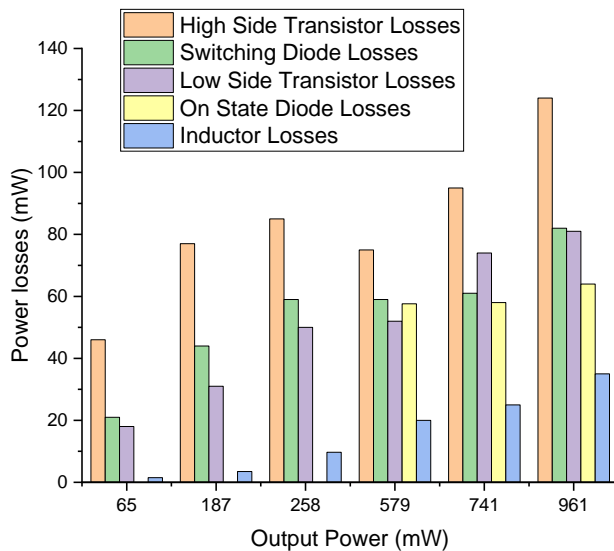


Figure 5.46: The simulated device losses in the three level converter when operated with the experimental switching signal.

Other than the magnitude of the losses increasing the primary difference is the transistor losses becoming larger than the diode losses even at the 10V operation. Compared to figure 40 where the switching diode tended to be contributed the most to the losses. This is to be expected as the transistor is the device that is switching so with worse switching performance larger losses are expected.

5.8 Conclusion

To conclude the findings of this chapter, there are a number of ways to further improve the layout of both the circuit and the transistors themselves to further the work performed in chapter 4. The three level and five level circuit schematics have been demonstrated both experimentally and using simulations and efficiency improvements have been shown across a range of voltages and frequencies. 1Mhz 10V and 25V operation was examined as well as 50Mhz 10V operation. In the higher voltage and higher frequency of these configurations, improvements were shown to be gained from the multi level configurations. The three level and five level showing over 30% efficiency increases at 50Mhz 10V operation at certain power outputs.

The reduction in losses at lower output powers are the primary cause of this improvement as the schematic allows each power transistor to be subjected to a smaller switching voltage and therefore lower losses will be presented to it. Breakdowns of these losses have been performed in simulations to help to quantify the components which give rise to these improved losses.

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Chapter 6 – Conclusions and Further Work

In this work, GaN based HEMTs with novel device architecture as well as monolithically integrated buck converter circuits have been fabricated, tested and the results presented. The dual metal gate devices were presented in chapter 3 and demonstrated two main advantages the configuration can provide compared to standard GaN HEMTs. Improvements in transconductance as well as improvements in the drain induced barrier lowering (DIBL) have been demonstrated in both experimental and simulated work. The metal selection methodology has been outlined and contribution of the metal work function towards this effect has been explained using TCAD simulations.

Threshold voltage extraction measurements were performed to quantify the metals work function that were used in the experiments. The transconductance was then extracted experimentally from single metal gate (SMG) and dual metal gate (DMG) devices with total gate length from $1\mu\text{m}$ to 200nm . This has shown transconductance values from 162mS/mm for $1\mu\text{m}$ DMG devices to 229mS/mm for 200nm DMG devices. These values when compared to the same gate length devices comprised of a SMG show transconductance improvements from 8.7% at $1\mu\text{m}$ to 6% at 200nm . The drain induced barrier lowering effect on the DMG GaN HEMTs has also been characterised and compared with the SMG GaN HEMT. An improvement of around 50% is shown for devices with a gate length between $1\mu\text{m}$ and 200nm . This DIBL reduction leading to lower leakage currents within the device has also been demonstrated using simulations. These improvements have then been investigated using TCAD simulations to demonstrate the physics that give rise to these improvements. Simulations of electron velocity and peak electric field help to explain the improvements in transconductance seen within the device. Improvements in the electrostatic distribution under the gate region help to explain the ‘shielding’ effect that explains the DIBL improvement. Analysis of how the work function controls these effects has been shown and leads to the conclusion that maximising the difference in WF between the two metals leads to an increase in improvements.

In addition, monolithically integrated buck converters have been designed, fabricated, tested, and simulated. Standard synchronous buck converters with a fully integrated gate driver have been created and tested at different voltages and frequencies. Efficiencies above 80% have been demonstrated when operating at 10V with a 1MHz switching frequency. Higher frequency and higher power operation have been demonstrated at 50MHz 10V, with a peak efficiency of

54%, and 1MHz 25V with a peak efficiency of 57%. An analysis into the loss components in the integrated buck converter was then performed both experimentally and using SPICE simulations. It was found that the losses from the power transistors are the major contributor to the total loss in the integrated buck converter. Separating these losses into conduction and switching losses to get a greater understanding of the loss mechanisms in the integrated buck converter was also carried out. As well as this discrepancies with the simulated results and experimental results have been investigated and heating effects as well as the signal slew rate have been shown to explain these differences.

Following on from standard buck converter integrated circuit fabrications and characterisations, multi-level buck converter integrated circuit circuits were designed and fabricated. Two multi-level converter schematics were investigated, i.e., the three level and five level buck converters. The theory behind these circuits is the increased topological complexity is offset by the advantages they can bring to circuit efficiency, particularly when operating at low powers. These advantages come from the addition of the levels within the circuits that provide the ability to operate with a smaller switching voltage presented on the switching node.

The fabricated multi-level buck converters were compared with the standard converter in term of the efficiency and power losses. The multi-level converter circuits were operated in identical conditions to the standard converter, 1MHz 10V, 1MHz 25V and 50MHz 10V. At the 1MHz 10V operation mode the efficiency seen was lower for both multi-level circuits when compared to the standard converter. The three-level circuit demonstrated a maximum efficiency of 63% and 61% for the five-level converter. This was shown to be caused by primarily due to the introduction of a Schottky diode into the circuit which results in the increased losses.

On the other hand, at 1MHz 25V operation, the advantages of the multi-level converters become clear with increased efficiency across all output power ranges for both the three and five level converters. The efficiency peaks at 77% for both three and five level converters compared to 57% for the standard converter. Even more importantly at low output powers, around 10% the efficiency increased by almost three times in the three level from 8% to 22% and increased from 8% to 35% in the five level. The 50MHz 10V operation also showed a slight increase in efficiency for both the three level and five level converters at 65% compared to the standard converters 54%.

Due to the nature of the experimental setup, a detailed breakdown of the contributions to losses was not possible for this setup, simulations were performed to better understand these losses. The simulation results showed that the diode contribute a large share of the losses alongside the power transistors although even with this they can still outperform the standard converter in higher power efficiency.

Investigations into the effect of field plates within GaN HEMTs has been performed. Comparison of dynamic Ron and intrinsic capacitance of the GaN HEMTs with field plate and without field plate were presented. Both the source field plate (SFP) and gate field plate (GFP) in the GaN HEMTs were found effective in suppressing the dynamic Ron compared to the device without a field plate. On the other hand, the GaN HEMTs with SFP exhibit a lower gate-drain intrinsic capacitance or Miller capacitance compared to the GaN HEMTs with GFP. In addition, the step change behaviour in the gate-drain intrinsic capacitance observed in the field-plate GaN HEMTs were discussed. The SPICE simulations on the buck converter with the smaller gate-drain intrinsic capacitance in the power transistors with a SFP suggested a 3 times improvement in the switching times when compared with the power transistors with a GFP.

6.1 - Further Work

There are a few different areas and avenues of further research that could be performed to further the work presented in this thesis.

6.1.1 – Dual Metal Gate GaN HEMTs

With regards to the dual gate devices, there are several aspects that could be investigate which could potentially provide further advantages than the results that presented in the study. One of these avenues is changing the AlGa_N barrier thickness in the device. Some initial simulations performed showed the potential that altering the AlGa_N barrier thickness had an impact on the transconductance improvement seen within the devices. Two identical devices with a different AlGa_N barrier were simulated and the thinner barrier showed a 9% transconductance improvement compared to 7% for the thicker barrier. This was only very preliminary work however and fabrications would need to be made to see if this is an important factor in DMG device improvements.

Investigations on different gate metals and with a larger work function difference between the two gate metals could be performed. A larger metal work function difference, in theory should lead to further improvements in both the DIBL reduction and the improvement in

transconductance. Using aluminium in place of titanium and platinum in place of palladium would further increase the metal work function difference.

Finally, the effect of DMG on the GaN HEMTs with a further decreased gate length (sub 100nm gate length) could be investigated. As the gate length is reduced, the DIBL is expected to become worse and suppression of the DIBL becomes critical for GHz operations.

6.1.2 – Integrated buck converter

For further work regarding the buck converters, there are a few different avenues of potential research regarding the devices in the circuit and the circuit topology itself. For further investigations regarding the devices, integration of the dual gate devices in place of the conventional power transistors could provide efficiency boosts within the circuit. The suppression of the DIBL will contribute to better performance that should lead to improved efficiency.

In addition, a more comprehensive study into the field plate design could lead to both device level and circuit level improvements. Simulations performed in this study suggested the SFP is the most suitable choice for the power transistors in the buck converter and hence the SFP was used in the fabricated buck converters in this project. Fabrications of buck converters with different field plate configurations would verify the simulation results and also help quantify how much of an improvement in the efficiency that the field plated power transistors could provide. Furthermore, a more detailed investigation into the field plate extension and height above the surface of the device may lead to further improvements that could be integrated into the buck converters.

The effect of source-drain separation (L_{sd}) in the power transistors on the R_{on} and hence on the efficiency of the buck converters was investigated in this study. There are other methods to reduce the R_{on} of the power transistors. For example, the gate width of the transistors can be scaled up to achieve a lower R_{on} . Figure 6.1 shows the I-V characteristics of the fabricated GaN HEMT with gate width of 1mm and 2mm at $V_{gs}=0V$. The extracted R_{on} for the 1mm and 2mm devices is 3.8ohm and 1.98ohm, respectively. The reduction in the R_{on} of the power transistors will reduce the conduction loss in the buck converter in the same manner as reduction of the L_{sd} . The advantage of scaling up the gate width over the reduction of L_{sd} is that the blocking voltage capability of the power transistor will not be affected. However, the drawback of the larger gate width power transistor is the increased in the intrinsic capacitances in the transistors. This will lead to an increase in the switching losses of the buck converters.

The trade-off between the conduction loss and switching losses ultimately depends on the switching frequency of the buck converters.

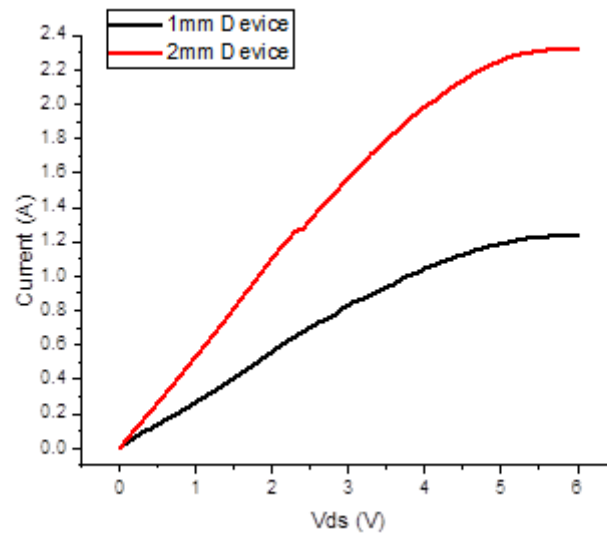


Figure 6.1: A comparison of the on-state current characteristics between a 1mm and a 2mm device.

Further investigations into mitigating the heating effects within the power transistors is also an avenue that should be investigated. Fully packaging the device with a high thermally conductive package then investigating various cooling methods should also lead to increased device performance. Comparisons between different packages and using different methods of air cooling could be investigated and maximum temperatures before degraded device performance would be interesting avenues of investigation.

As well as the improvements in power transistors that could be investigated, the improvements in the Schottky diode could provide large improvements in efficiency. One avenue of this could be implementing a dual Schottky metal pad for the diode. Some work has been published showing the improved turn on voltage and current through the diode that this change can bring¹.

Finally, another key area that has not been investigated in this project is the multi-phase buck converter schematic. Some preliminary SPICE simulation work showed that at high output powers the multi-phase buck converter had the potential to provide the highest efficiency. The fabrication steps for the integrated multi-phase buck converter would be the same as the multi-level buck converter in this study. However, the control mechanism for this type of buck converter is much more complex. Six different input pulse signals would need to be created

and operate at 120 degrees out of phase with each other. Simulations suggested that at low output powers the multi-phase converter did not provide any advantage over the standard converter, and this was a main reason it was not pursued in this project. For voltage conversion applications with a high output power requirement, the multi-phase buck converter could be an attractive choice to investigate.

References

- 1- Chang, T.F., Huang, C.F., Yang, T.Y., Chiu, C.W., Huang, T.Y., Lee, K.Y. and Zhao, F., 2015. Low turn-on voltage dual metal AlGaN/GaN Schottky barrier diode. *Solid-State Electronics*, 105, pp.12-15.