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Novel Control Strategies for High Speed Permanent Magnet Brushless Motor Drives

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ABSTRACT

Permanent magnet (PM) brushless motors are eminently suitable for high speed drive systems due to high power density and high efficiency. This thesis presents a thorough investigation into control strategies for high speed PM brushless motor drives, considering both brushless AC (BLAC) operation and brushless DC (BLDC) operation.

In order to solve the current harmonic issues which are common to BLAC drives, the effect of inverter nonlinearity is firstly investigated. It is shown that the nonlinearity effect will generate the $6n\pm1^{th}$ order phase current harmonics. Based on the analysis of current harmonics, an inverter nonlinearity compensation method is presented utilizing simple signal processing algorithms. The effect of non-sinusoidal back-electromotive force (EMF) on phase current is also analysed. Based on this analysis, an adaptive current harmonics suppression method that can compensate any periodic non-ideal factors is proposed. The feedforward self-tuning compensation voltages are generated without requiring any knowledge of back-EMF harmonic components, inverter parameters or motor parameters. With the proposed method, the current harmonic distortion of BLAC drives is reduced by 86%.

The position detection errors of BLDC drives are comprehensively investigated. The effects of both misaligned and uneven Hall signal errors are analysed, and a Hall signal balancing strategy is developed so that the peak current ripples can be suppressed by 80%. A new pulse-width modulation (PWM) generation scheme is also proposed to eliminate the PWM update delay of BLDC drives.

In addition, the cause of phase delay error and its effect on BLDC drives are analysed, while a compensation strategy based on the d-axis current is proposed. The optimal phase advance angle can be generated by reducing the d-axis current to zero so that the phase current is in phase with the corresponding back-EMF. Thus, the phase delay can be successfully eliminated, and the peak-to-peak current can be reduced by as much as 20% without the knowledge of the motor parameters or the need for any additional hardware.

Finally, wide angle twelve-step BLDC drives are investigated to reduce the current harmonics typically found in traditional six-step BLDC control strategies. A phase delay error compensation strategy based on the stator current is also proposed so that the continuous absolute position signal is no longer needed. By reducing the stator current to the minimum value, the phase delay error can still be compensated. Results show that when the phase delay error is compensated in the wide angle twelve-step BLDC drives, a quasi-sinusoidal current waveform can be generated.

All theoretical analyses are validated experimentally on a prototype high speed motor drive.

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NOMENCLATURES

Variables

B	Air-gap flux density (T)
B_H	Threshold flux density of Hall sensor (T)
E	Fundamental component of back-EMF in synchronous reference frame (V)
e_a, e_b, e_c	Phase back-EMFs a, b, c (V)
f_e	Electric frequency (Hz)
H_a, H_b, H_c	Detected Hall signals a, b, c
H'_a, H'_b, H'_c	Rebuilt Hall sensor signals a, b, c
I_s	Stator current (A)
I_a, I_b, I_c,	Currents of phases a, b, c (A)
I_d, I_q	*D*- and q-axis currents (A)
I_{rated}	Rated current (A)
L	Self winding inductance (H)
L_s	Stator winding inductance (H)
L_d, L_q	*D*- and q-axis inductances (H)
M	Mutual winding inductance(H)
R	Stator resistance (Ω)
R_{se}	Equivalent resistance of switch (Ω)
R_{de}	Equivalent resistance of diode (Ω)
T_{dt}	Inserted dead time (s)
T_{pwm}	PWM switch period (s)
T_s	Sample period (s)

$T_{on/off}$	Overall delay between turn-on/off drive signal to effectively fulfil switch-on state (s)
U_{an}, U_{bn}, U_{cn},	Phase supply voltages a, b, c (V)
V_{dc}	DC supply voltage (V)
V_{se_th}	Threshold voltage of switch (V)
V_{de_th}	Threshold voltage of diode (V)
ω_e	Electrical angular frequency (rad/s)
k_1	Coefficient of fundamental back-EMF component
k_n	Coefficient of n^{th} harmonic back-EMF component
θ	Absolute electrical angle (rad)
θ_1	Initial phase angle of fundamental back-EMF component (rad)
θ_n	Initial phase angle of n^{th} order harmonic back-EMF component (rad)
ε_a, ε_b, ε_c	Hall sensor misplacements a, b, c (rad)

Abbreviations

AC	Alternating current
Adaline	Adaptive linear neuron
Back-EMF	Back-electromotive force
BLAC	Brushless alternating current
BLDC	Brushless direct current
BPF	Band pass filter
CSI	Current source inverter
DC	Direct current
EMI	Electromagnetic interference
GaN	Gallium nitride
HPF	High-order filter
IM	Induction machine

IPF	Internal power factor
IPM	Interior permanent magnet
LUT	Look-up-table
LPF	Low pass filter
LMS	Least-mean-square
MLI	Multilevel inverter
MRFT	Multiple-synchronous rotating frame transformations
NdFeB	Neodymium-iron-boron
PI	Proportional–Integral
PLL	Phase locked loop
PM	Permanent magnet
PAM	Pulse-amplitude modulation
PWM	Pulse width modulation
QCSI	Quasi-current source inverter
RLS	Recursive least-square
SFE	Synchronous frequency extractor
SFFR	Switching-to-fundamental frequency ratio
SiC	Silicon carbide
SmCo	Samarium-cobalt
SPM	Surface mounted permanent magnet
SRM	Switched reluctance machine
VSI	Voltage source inverter
WBG	Wide-bandgap
ZCP	Zero-crossing point

CHAPTER 1

GENERAL INTRODUCTION

In the last few decades, thanks to the development of new materials, novel electrical machine topologies, power electronics, microprocessors and bearing technologies, high speed machine drive systems have been gaining popularities in both academia and industry, due to high power density and high efficiency. A high speed drive system mainly consists of a high speed machine, an inverter and the corresponding control strategies as shown in Fig. 1.1.

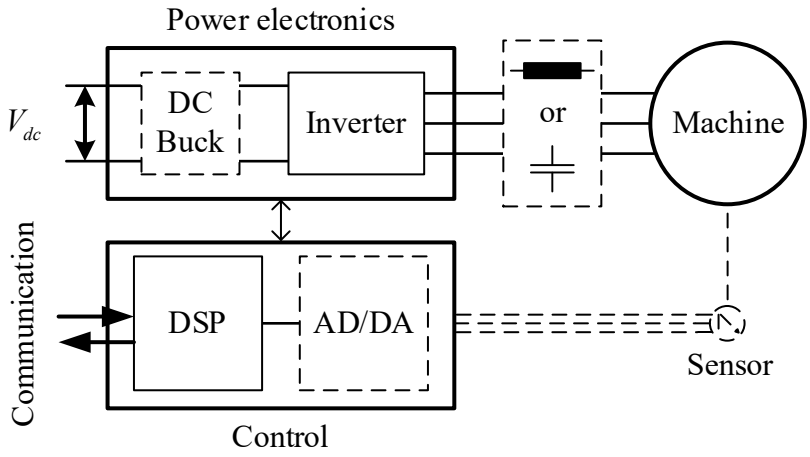


Fig. 1.1 Block diagram of high speed machine drive system. Necessary parts are marked in solid lines, while dependent parts are marked in dash lines.

High speed machines can be defined from different aspects. In terms of speed, the rotor angular velocity is used as criterion in [GER14] where high speed is defined to be in excess of 10 000 r/min. Considering the mechanical constrain, the rotor circumferential velocity is chosen as the definition in [BIN07], where high speed is defined to be in excess of 100 m/s. The relationship between the output power and the rotor angular velocity is used as criterion in [BOR10A]. It should be noticed that all the definitions have their own merits. In terms of machine topologies, different types of machines, e.g. permanent magnet (PM) machines [BIA04], induction machines (IMs) [BAR19], and switched reluctance machines (SRMs) [BAR17], can all be applied to high speed applications [GER14].

Considering high fundamental frequency and low stator inductance of high speed machines, the traditional voltage source inverters (VSIs), is no longer a default choice for high speed

machine drive systems. Various inverter topologies such as VSIs with front-end buck-converter [CUI15A], current source inverters (CSIs) [CHE13], quasi-current source inverters (QCSIs) [SIB14], Z-source inverters (ZSIs) [WUH20] and multilevel inverters (MLIs) [LIC20] etc., have been proposed. As stated in [ZWY08], the selection of optimal inverter topologies mainly depends on practical applications.

The control strategies, which determine the inverter switching status, can be mainly classified as brushless AC (BLAC) drives and brushless DC (BLDC) drives where sinusoidal currents and rectangular currents are generated accordingly. For the high speed drive system, the choice of control strategies also relates closely with inverter topologies. Although BLDC control strategies are widely employed [CUI15A] for high speed drives due to simple and robust structure, BLAC control strategies still have their advantages and should not be neglected.

This thesis will investigate both BLAC and BLDC control strategies for high speed PM motor drives.

In this chapter, the high speed machine drive systems will be reviewed comprehensively. Firstly, different high speed machine topologies will be briefly introduced and compared. Secondly, existing inverter topologies will be reviewed systematically. Then, key issues of high speed control strategies will be introduced while existing challenges for both high speed BLAC and BLDC drives will be emphasized. Finally, the outline and main contributions of this PhD thesis will be detailed.

1.1 High Speed Machines

High speed machines have been used in many applications, e.g. blowers, centrifugal compressors, flywheel systems, micro-turbines, pumps, spindles and turbochargers etc. One of the main advantages of high speed machines is the reduction of system size and weight for a given power [LIS16], since output power of an electrical machine is proportional to rotating speed and volume. Another reason in utilizing high speed machines is improved reliability due to elimination of intermediate gears, belts and other transmission arrangements [TEN14].

Different types of machines can all be applied to different high speed applications. The PM machines have the merits of high control performance while IMs and SRMs have the merits of simple structure, low maintenance requirement, and high fault tolerance. In this thesis, different types of IMs and SRMs are also reviewed to compared with the high speed PM machines.

Various high speed machine topologies are briefly summarised in Fig. 1.2 based on current research and relevant papers.

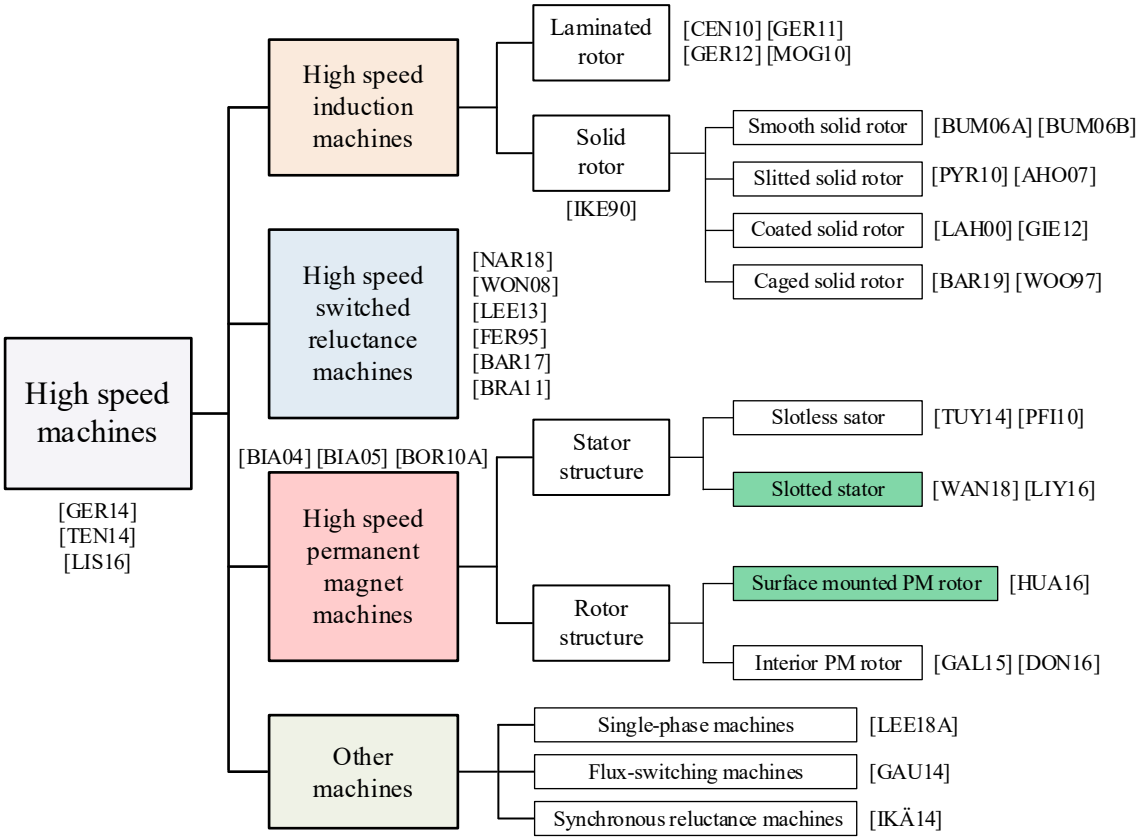


Fig. 1.2 Development of high speed machines and relevant references.

1.1.1 High Speed IMs

Various high speed IMs with different types of solid rotors, including smooth solid rotor [BUM06A], slitted solid rotor [PYR10], coated solid rotor [LAH00], caged solid rotor [BAR19], have been designed and investigated in literature. They are compared in terms of electromagnetic and mechanical performances such as power density, efficiency, mechanical strength, and circumferential velocity [IKE90]. The smooth solid rotor has the simplest and most robust structure [BUM06B] while the coated solid rotor can achieve the highest peripheral speed [GIE12]. The slitted solid rotor has a good torque generation capability at the cost of reduced mechanical strength [AHO07]. The caged solid rotor, on the other hand, combines the advantages of the solid rotor and the squirrel cage rotor so that both a high mechanical strength and a good electromagnetic performance is achieved [WOO97]. The cross-section of an IM with a caged solid rotor is shown in Fig. 1.3.

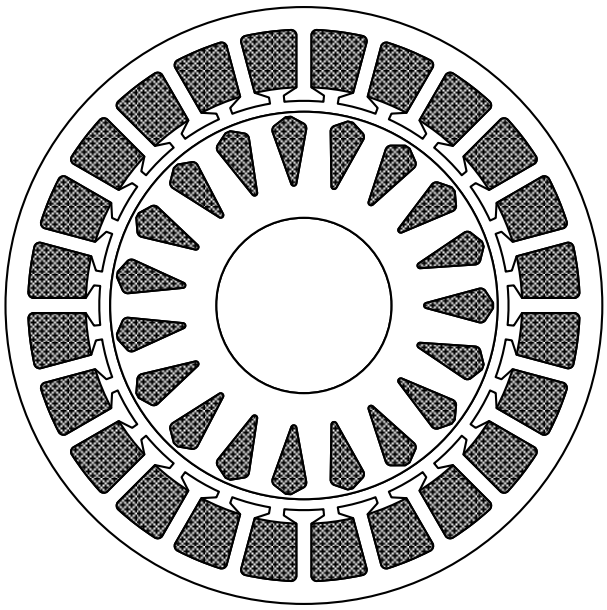


Fig. 1.3 Cross-section of IM with a caged solid rotor. [BAR19]

Several other papers have also investigated the optimization of high speed IMs with the laminated rotors. The laminated rotor topology is optimized in [GER11] and [GER12]. The lamination stack properties are investigated in [MOG10] while the selection of rotor lamination material is studied in [CEN10].

It is shown in the previous research that IMs are popular in high speed applications due to robust structure and low maintenance requirement. Since no PM materials are used, IMs can eliminate the risk of demagnetisation and have high temperature withstand. There are also some remarkable disadvantages of high speed IMs, namely, low power factor, low efficiency and high control complexity.

1.1.2 High Speed SRMs

Apart from IMs, SRMs are also applied to several high speed applications due to advantages of simplest rotor structure, high working temperature, high fault tolerance and low cost [NAR18] [BAR17]. However, some obvious drawbacks of SRMs exist, e.g. low power density, high torque ripple, high level of noise and vibration, and high mechanical loss [WON08] [LEE13]. Thus, high speed SRMs are usually operated in some harsh operational environments [FER95] and low-cost mass-production markets [BRA11]. The cross-section of a SRM is shown in Fig. 1.4.

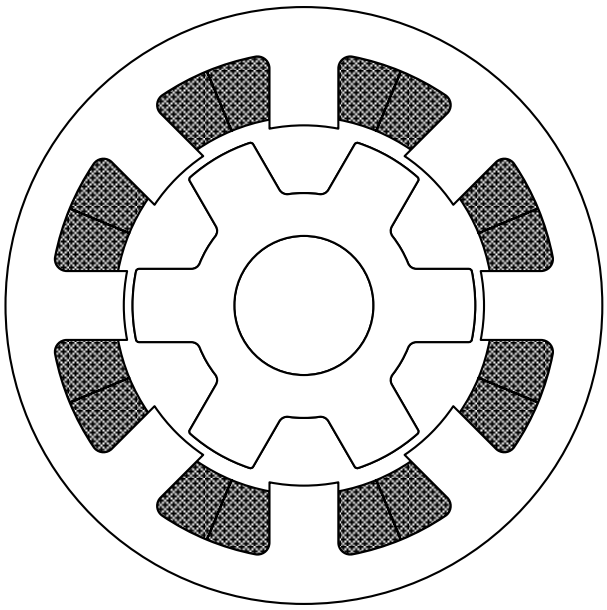


Fig. 1.4 Cross-section of SRM. [ZHU07]

1.1.3 High Speed PM Machines

Thanks to high energy density characteristic of rare-earth PM materials such as neodymium-iron-boron (NdFeB) and samarium-cobalt (SmCo), high speed PM machines have advantages of high power density as well as high efficiency compared with other types of high speed machines [BIA04]. Thus, they are most widely utilized in the applications where high control performances are required [BIA05] [BOR10A].

In terms of stator structures, high speed PM machines can be mainly divided into two different types, i.e. slotless [LOV04] [PFI10] and slotted stator PM machines [WAN18A]. Compared with slotted high speed machines, slotless machines have high demagnetization performance, low rotor loss and low torque ripple at the cost of lower torque density [TUY14]. On the other hand, slotted high speed machines have higher motor inductances which can help attenuate the current distortion under specific drive conditions [LIY16].

In terms of rotor structure, high speed PM machines can also be mainly divided into surface mounted permanent magnet (SPM) [HUA16] and interior permanent magnet (IPM) machines [GAL15]. For high speed SPM machines, retaining sleeves are usually required to keep the rotor mechanical integrity [ZHA15]. Although high speed IPM machines require lower magnet usage and no retaining sleeves, they usually have relative worse mechanical performance since the rotating related force focuses on the magnetic bridge. Besides, high speed IPM machines

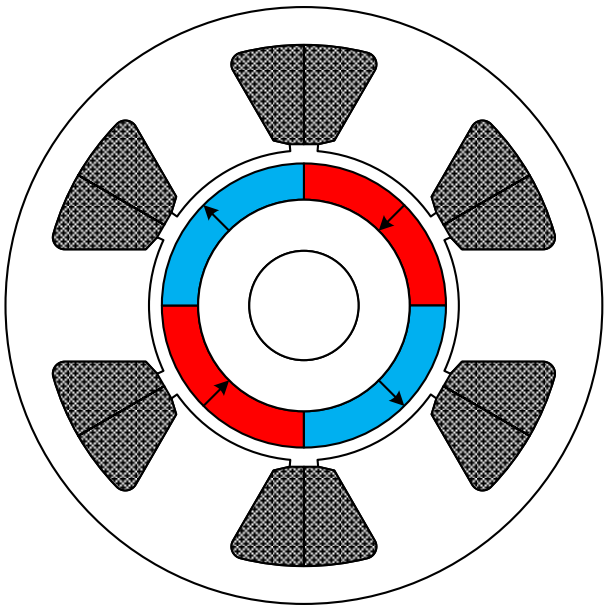


Fig. 1.5 Cross-section of SPM slotted motor. [BIA04]

suffer from noise and vibration problems due to their relatively low nature frequency [DON16]. The cross-section of a SPM slotted motor is shown in Fig. 1.5.

Other high speed machines such as high speed flux-switching machines [GAU14] and high speed synchronous reluctance machines [IKÄ14] are also presented in literature. Besides, all the aforementioned research focuses on three phase machines, single phase machines can also be used for the high speed drive system [LEE18A].

1.1.4 Comparison of High Speed Machines

The comparison of high speed machines is given in Table. 1.1. In this thesis, a high speed SPM slotted motor is used for investigation as shown in the Appendix.

Table 1.1 COMPARISON OF HIGH SPEED MACHINES

Machine topology	Advantages and disadvantages
1. IMs	a. Robust structure b. Low maintenance requirement c. High temperature withstand d. Low cost *e. Low power factor* *f. High control complexity*

2. SRMs	a. Simplest rotor structure b. High temperature withstand c. High fault tolerance d. Lowest cost *e. Low power density* *f. High torque ripple, noise and vibration*
3. PM machines	a. High power density b. High efficiency *c. Low temperature withstand* *d. Low rotor strength* *e. High cost*

1.2 Inverter Topologies

In order to achieve overall high performance of the control systems, the inverter topologies of high speed drive systems should also be considered. Since the high speed machine has a high fundamental frequency and a low stator inductance, the VSI is no longer a default choice. Besides, unlike the high speed machine whose size and weight reduce with speed, the size of power electronics is irrelevant with the machine speed and mainly depends on the power rating, passive components and topologies [ZWY06]. For a high speed drive system, the size and weight of the inverter and corresponding passive components may be even larger than the machine [ZWY08]. Thus, it is important to consider different inverter topologies for high speed drive systems.

Various inverter topologies are briefly summarised in Fig. 1.6 based on current research and relevant papers.

1.2.1 VSIs

The block diagram of a traditional VSI with a fixed DC voltage supply is shown in Fig. 1.7. Both BLAC [SON16A] and BLDC [YAN20A] drives can be realized by the traditional VSI through pulse-width modulation (PWM) techniques. Although this kind of inverter is widely employed for high speed drives [FAN14], the adaption of the traditional VSI still faces some challenges.

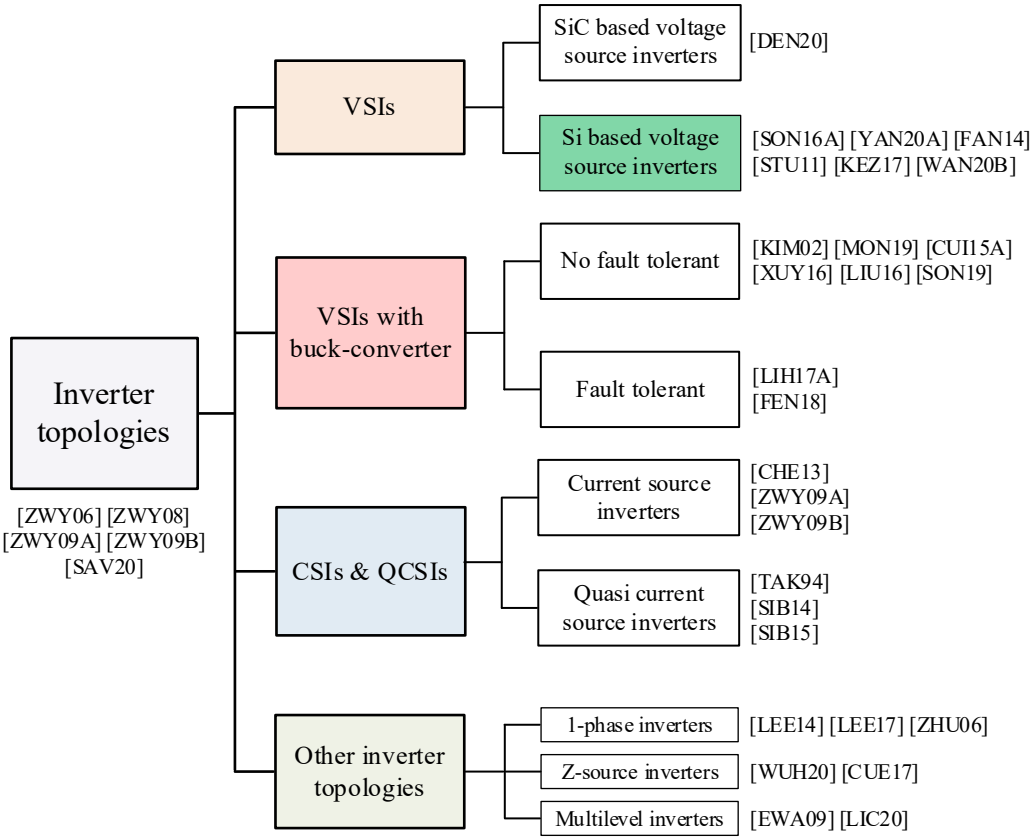


Fig. 1.6 Development of inverter topologies for high speed drive and relevant references.

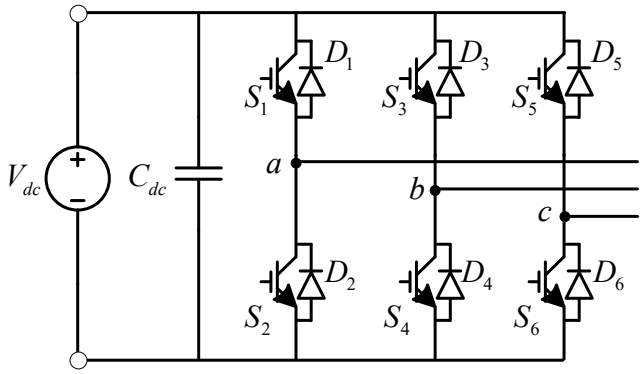


Fig. 1.7 Block diagram of VSI. [WAN20B]

Firstly, it is known that the switching frequency of the traditional VSI cannot be pushed too high and is usually restricted by the physical limit of power electronics. The typical switching frequency of IGBT devices is no higher than 20-30k Hz while the fundamental frequencies of high speed machines are usually several hundreds or even thousands Hz [ZWY06]. In recent years, the wide-bandgap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN), have been considered [DEN20]. Compared with the traditional Si-based VIS, the WBG device-based VSI has higher switching frequency, higher thermal conductivity, higher current

density and wider voltage range. However, the use of high switching frequency WBG devices will also cause an increased electromagnetic interference (EMI) [SAV20]. Besides, the high cost of the WBG devices limits their application.

Another drawback of the traditional VSI is the large current harmonics in high speed drives. For high speed machines, especially the ones with slotless stators, the low stator inductance along with the low switching-to-fundamental frequency ratio (SFFR) will cause severe subharmonics [STU11] and low-frequency current oscillations [KEZ17]. In order to solve the low stator inductance problem, additional external inductances might also be required under some conditions.

1.2.2 VSIs with Front-End Buck-Converter

As shown in the previous section, with the increase of motor speed, the increase of inverter switching frequency and the current control bandwidth requirement make traditional VSI less favourable. Another widely used inverter topology, i.e., VSI with front-end buck-converter, is shown in Fig. 1.8.

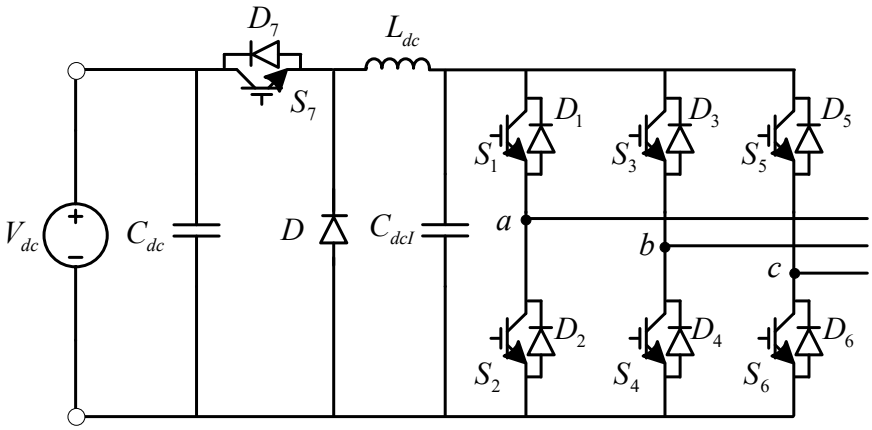


Fig. 1.8 Block diagram of VSI with front-end buck-converter. [SON19]

This concept of this kind of inverters is firstly proposed in [KIM02] for high speed drives, where the authors propose a variable DC link voltage inverter. In [ZWY06], the VSI with front-end buck-converter is proposed for high speed drives. The DC link voltage is modulated through the front-end switch S_7 along with the passive components L_{dc} and C_{dcI}, while the three phase inverter switches S_{1-6} work at the fundamental frequency of the machine [MON19]. The switching frequency of the three phase inverter is thus largely reduced. The pulse-amplitude modulation (PAM) techniques are usually used for BLDC drives [LIU16].

When this inverter topology is used for high speed machine drives, the low stator inductance becomes an advantage since the commutation time will be reduced [XUY16] and no external inductances are required. The control complexity of the system will also be reduced since the PWM delay will be eliminated [CUI15A].

In some applications where high reliability and safety are required, the fault-tolerant VSI with front-end buck-converter is also proposed. The key idea is to provide redundant topologies to ensure safety operation. In [LIH17A], a fault-tolerant VSI with front-end buck-converter is proposed for an aerospace application. An additional leg, a fault protective circuit and redundant front-end switches are also added. A similar method is also employed in [FEN18].

The main drawback of this inverter topology is the use of an additional buck-converter and passive components which will inevitably increase both system cost and size. Besides, the phase currents cannot be controlled directly since they are related with stator resistance, stator inductance, back-electromotive force (back-EMF) and supplied voltage. For some high speed machines, the stator inductance may be just several μH, this kind of inverter will then cause large current ripple [SIB15].

1.2.3 CSIs and QCSIs

Another inverter topology that can make the three phase inverter switching at the fundamental frequency is the CSI with front-end converter [CHE13]. The block diagram is shown in Fig. 1.9.

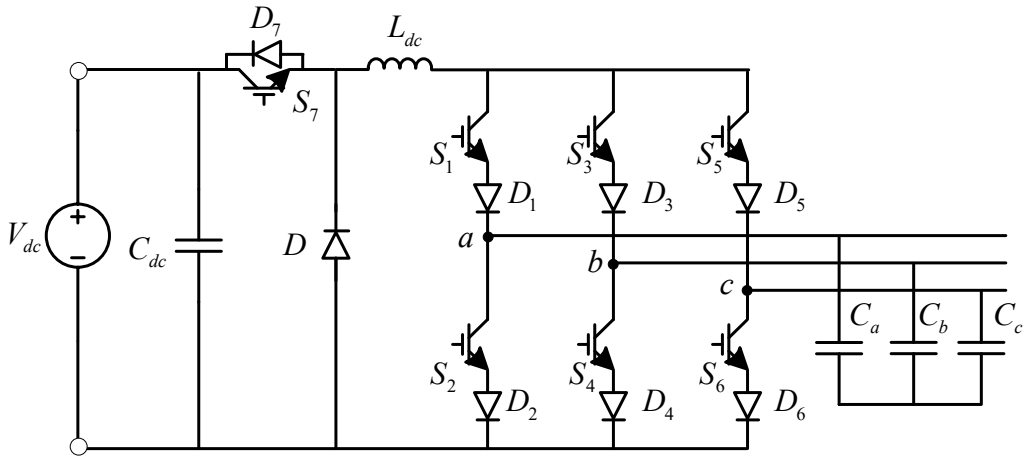


Fig. 1.9 Block diagram of CSI with front-end converter. [ZWY09A]

Similar to VSIs with front-end buck-converter, the front-end switch S_7 is used. Rather than modulating the DC voltage, this inverter directly controls the DC current through S_7 along with a large DC inductor L_{dc}. The phase current can be directly controlled by this kind of inverter [ZWY09A]. Besides, CSIs have an inherent advantage of circuit shoot-through protection.

Apart from L_{dc} that is used in the front-end converter, this inverter topology also requires three decoupling capacitors $C_{a,b,c}$ on the three phase outputs. The low stator inductance still helps to reduce the commutation time. However, the stator inductance together with decoupling capacitors might cause current oscillations [ZWY09B]. Besides, a large L_{dc} is required to suppress the current ripple. The use of DC inductor and decoupling capacitors will increase the size of the inverter. The reliability of the drive system may also be influenced by the passive components. Thus, the employment of this kind of inverter in high speed drive is limited.

In order to both keep the advantages of CSIs and reduce the passive components, QCSIs are proposed as shown in Fig. 1.10. The QCSI consists a front-end converter, an inductor L_{dc}, a diode D_p for bypassing the power regenerated from the machine and a three phase inverter [TAK94]. The key concept is to use the diode D_p as the current path during the free-wheeling period, so that the DC capacitor C_{dcI} can be eliminated. During the operation, the DC current is controlled by S_7 while the three phase inverter switches S_{1-6} work at the fundamental frequency of the machine [SIB15].

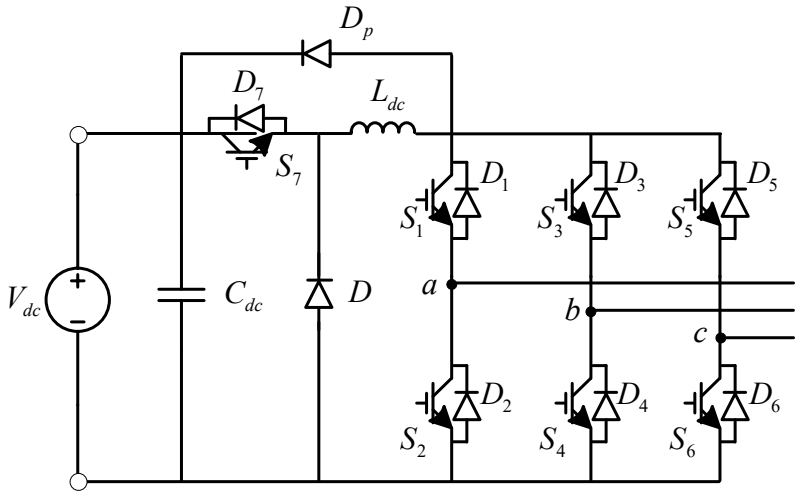


Fig. 1.10 Block diagram of QCSI. [SIB14]

This inverter topology shows superior control performance, especially low current ripple compared with VSIs with front-end buck-converter when the stator inductance is low [SIB14].

Besides, compared with CSIs with front-end converter, a more common three phase voltage inverter is used and the decoupling capacitors can be eliminated.

Some other inverter topologies have also been proposed in the previous researches. The concept of ZSIs is firstly proposed in [PEN03]. The unique feature of ZSIs is that the impedance network rather than power electronics is used to adjust the DC voltage. In [WUH20] and [CUE17], ZSIs are used for the high speed machine drives. MLIs are also used in the high speed machine drive systems. In [EWA09], a three-level inverter is presented to reduce the switching losses. In [LIC20], a hybrid active neutral-point-clamped inverter is proposed for high speed drives with high power rating. Besides, all the aforementioned research focuses on the inverter topologies of the three phase machine, in [LEE14], [LEE17] and [ZHU06], single phase inverter topologies are also proposed for high speed drive systems.

1.2.4 Comparison of Inverter Topologies

VSIs and VSIs with front-end buck-converter are the two most commonly used inverter topologies in high speed drives. QCSIs can also be used in some certain applications. Thus, the comparison of these inverter topologies for high speed drive systems is given in Table 1.2.

VSIs and VSIs with front-end buck-converter have been compared in terms of size, cost, and control complexity in [ZWY06]. It is shown that VSIs can achieve smaller size and lower cost at the expense of more complex control. Besides, only PWM techniques can be used in VSIs while VSIs with front-end buck-converter can also use PAM techniques [CUI15A]. It should also be noticed that the control techniques and the machine topologies will also have an influence on the losses in both machines and inverters [SCH14]. For the slotless high speed machine, a higher system efficiency can be achieved through PAM techniques by choosing the VSI with front-end buck-converter. However, for the high speed machine with a slotted stator, the efficiency is almost the same when driven by two different inverter topologies.

If the high speed machine has an extremely small stator inductance, both VSIs and VSIs with front-end buck-converter will suffer from current harmonic problem. QCSIs, on the other hand, can directly control the current and is thus an attractive option under this condition [SIB14]. However, the use of diode D_p for bypassing the power limits the application of QCSIs in high power rating and high current conditions.

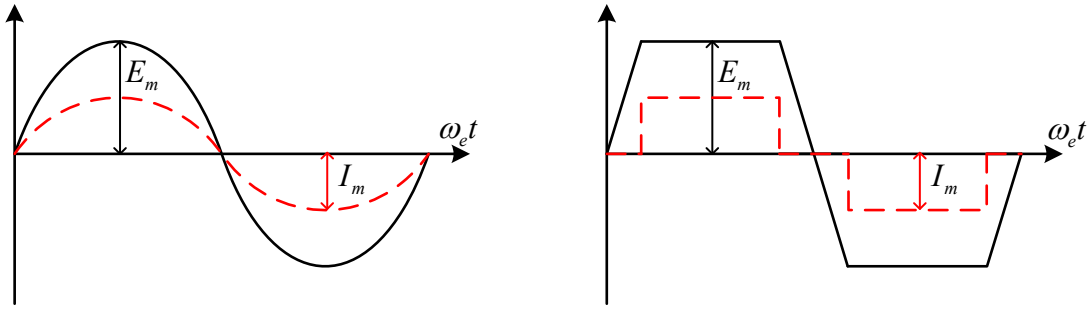
Overall, there is no consensus on which inverter topology is superior and the optimal inverter should be chosen according to the application [ZWY09A]. Considering the machine topology and practical requirements, in this thesis, a VSI is used for investigation as shown in the Appendix.

Table 1.2 COMPARISON OF INVERTER TOPOLOGIES

Inverter topology	Advantages and *disadvantages*
1. VSIs	a. Low cost b. Compact size c. Wide operation range *d. High current harmonics when stator inductance is small* *e. High control complexity*
2. VSIs with front-end buck-converter	a. Low control complexity b. Wide operation range *c. High cost* *e. High current harmonics when stator inductance is small* *f. Size determined by passive components*
3. QCSIs	a. Low PWM current harmonics b. Low control complexity *c. High cost* *d. Size determined by passive components* *e. Limited operation range*

1.3 High Speed Control Strategies

For a VSI fed high speed drive system, both BLAC control strategies and BLDC control strategies can be used. Under BLAC drives, the inverter ideally supplies sinusoidal currents, while rectangular currents are usually generated in BLDC drives. The ideal BLAC drives require a sinusoidal back-EMF, while the ideal BLDC drives require a trapezoidal back-EMF as shown in Fig. 1.11. It should be noticed that for a practical high speed motor, the back-EMF waveform may be neither ideal sinusoidal or trapezoidal.



(a) Ideal BLAC drive (b) Ideal BLDC drive

Fig. 1.11 Back-EMF and phase current waveforms of ideal brushless motor control strategies.

For both BLAC and BLDC control strategies, the rotor position signals are important to achieve a high performance control. Nevertheless, the position signal requirements are different. For BLAC drives, a continuous absolute position signal is needed. For BLDC drives, only discrete commutation points are needed so that the control complexity is reduced. Both these two control strategies have been considered for high speed drives as summarised in Fig. 1.12 based on current research and relevant papers.

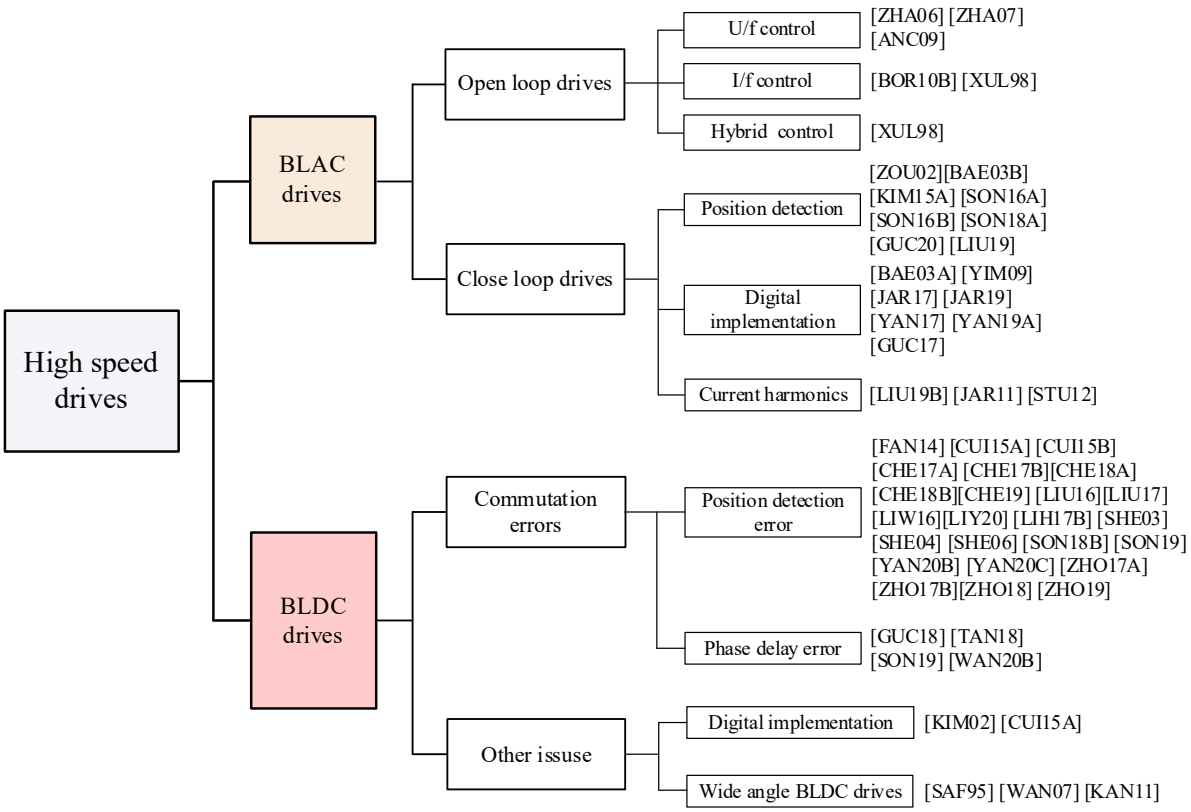


Fig. 1.12 Development of high speed control strategies and relevant references.

1.3.1 BLAC Control Strategies

1.3.1.1 Open Loop Control Strategies

In the early years, the open loop control strategies are usually used for high speed drives considering the limitation of digital controllers and power electronics at that time [XUL98]. In principle, the open loop V/f control can be treated as the simplest sensorless control strategies where the reference voltage V^* is pre-set with respect to the command speed ω_e^*. The block diagram of the open loop V/f control strategy is shown in Fig. 1.13.

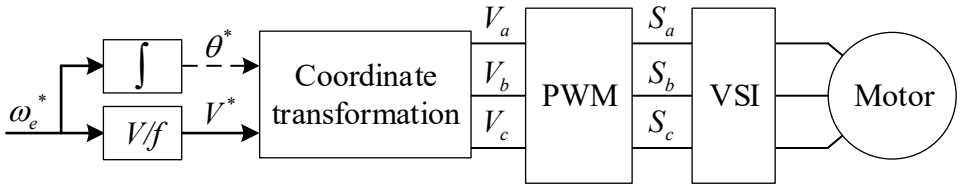


Fig. 1.13 Block diagram of high speed open loop V/f control strategy. [XUL98]

It should be noticed that the reference voltage V^* is critical for performance of the V/f control strategy. An improperly defined reference voltage may even cause instability problems. The machine parameters have a significant influence on the optimal reference voltage. In [ZHA06], the authors point out that a larger stator resistance is favourable for the stable operation of open loop V/f control. In [ZHA07], after considering the effects of stator resistance, an optimal V/f control strategy is proposed for the high speed drive. However, the stator parameters change with temperature and are hard to be considered accurately. In [ANC09], two stabilising loops are added in the open loop V/f control to correct the amplitude and phase of the reference voltage and to improve the dynamic response of high speed motor drives. Nevertheless, the large starting current problem still exists.

In order to solve the over-current problem of the V/f control, the open loop I/f control strategy is also proposed for high speed BLAC drives, as shown in Fig. 1.14.

Under I/f control, the reference voltage V^* is generated through a current regulator while the reference current I^* is pre-set with respect to the command speed ω_e^*. Compared with the V/f control, the reference current I^* can be easily set since it depends only on motor speed and load. The motor parameters have no influence on the open loop I/f control strategy [BOR10B].

Hybrid open loop control strategy that employs U/f control and I/f control under different speed ranges is also proposed in [XUL98]. Although open loop control strategies can be used in the

high speed motor drive system, they all need pre-set reference signals which significant influence the control performance. For application with high efficiency and safety standards, the open loop control strategies can no longer meet the requirement. Besides, with the development of digital controllers, the computation burden of close loop control is no longer a predominant problem. Thus, the use of open loop control strategies becomes less popular nowadays.

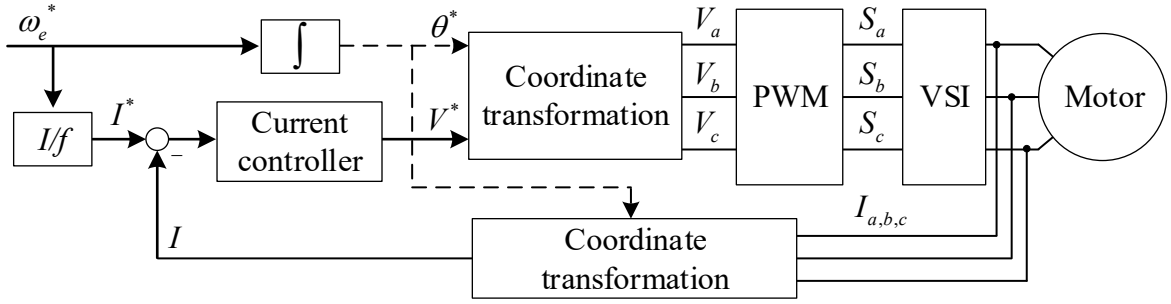


Fig. 1.14 Block diagram of high speed open loop I/f control strategy. [BOR10B]

1.3.1.2 Close Loop Control Strategies

Although modern control strategies such as predictive control [TAN16] have been proposed for high speed BLAC drives, field-oriented control (FOC) is still the most popular choice among close loop control strategies considering the control complexity. The block diagram of high speed close loop BLAC FOC strategy is shown in Fig. 1.15.

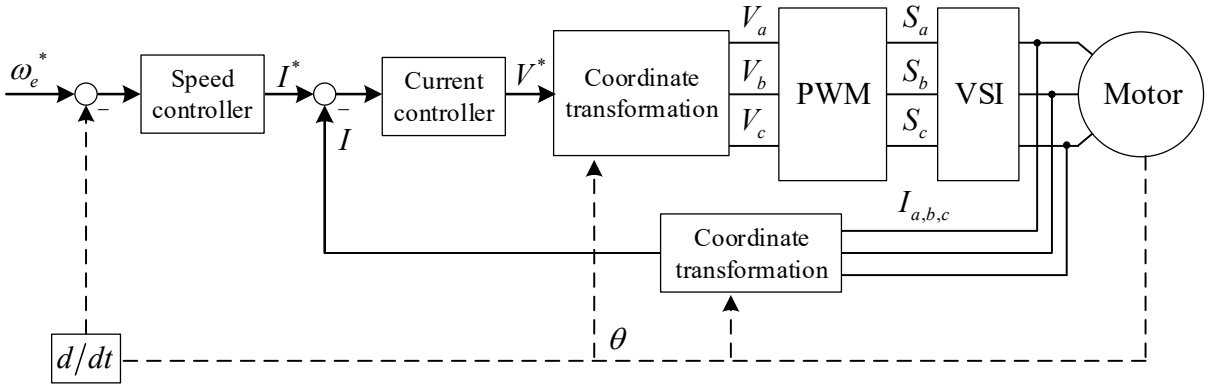


Fig. 1.15 Block diagram of the high speed close loop BLAC FOC strategy.

In order to achieve a high performance close loop high speed BLAC drive, several factors should be considered. Firstly, the rotor position signal must be accurate and able to deal with the changes of motor parameters and operation conditions, such as motor speed, load and temperature. Additionally, the digital implementation issues such as time delay, discretization

method and current linear approximation error should also be considered. Besides, the current harmonic problem becomes more severe for high speed drive considering low motor inductance and low SFFR. Thus, it is important to consider current harmonic issues. The relevant research is summarized as follows.

A. Position Detection Issues

The accurate rotor position signal is essential for high speed BLAC drives since the position detection error will cause large current ripple, large copper loss and low efficiency. Existing methods to detect the continuous absolute position signal can be classified into two groups: sensorless methods and position sensor based methods.

For sensorless methods, back-EMF based methods are more suitable for high speed BLAC drives compared with high frequency signal injection based methods [SON18A]. In [BAE03A] and [GUC20], the position signal is directly calculated from the EMF voltage. In [SON16A], the back-EMF estimator based on sliding-mode observer (SMO) is proposed. The SMO has the features of high precision and anti-disturbance. In [BAE03B], a simplified model reference adaptive observer is also designed. All the aforementioned sensorless control methods neglect the iron loss. However, since the iron loss increases with the square of motor speed, it should be considered in high speed range. The effect of iron loss on high speed sensorless drives is investigated in [KIM15A]. Although various sensorless methods are employed in high speed applications, they still have some limitations. Firstly, during the zero and low speed range, the back-EMF voltage is not high enough and the estimation is usually not accurate. Thus, the current is usually controlled by I/f control method during the initial alignment and starting process [GUC20]. Besides, the sensorless methods may also be influenced by the motor parameters, operation conditions and inverter nonlinearity.

The position sensor based methods are also widely used in many applications. The use of resolvers and encoders in high speed drives are limited due to their complex mechanical coupling structure. The Hall-effect sensors, on the other hand, do not require extra mechanical coupling and are popular in high speed drives. In [ZOU02], the continuous absolute position signal is detected through one discrete Hall sensor. The phase locked loop (PLL) is used to compensate the error between the discrete Hall signal and the continuous absolute position signal. In [LIU19A], three discrete Hall sensors are used to obtain the position signal. The coordinate transformation is used to obtain the Hall rotary vector. Then, the synchronous frequency extractors (SFEs) are used to extract the fundamental component of the Hall rotary

vector. The continuous absolute position signal is then calculated through the fundamental Hall vector. Linear Hall sensors that generate sinusoidal waveforms can also be used as the position sensor and achieve better performance than the discrete ones [ZOU02]. Two linear Hall sensors that are placed 90 electrical degrees apart are usually used. It is known that there are harmonics in the output of the linear Hall sensors. In [SON16B], the SFEs are used to filter out these harmonics and achieve high performance high speed BLAC control.

B. Digital Implementation Issues

In order to achieve the BLAC control strategy, all the signal processing including the speed loop control, the current loop control and the PWM generation are implemented in the digital discrete domain [GUC17]. When the motor speed is low, the difference between the continuous domain and the discrete domain can be neglected. However, for high speed drives, there are several digital implementation issues that should be carefully considered.

Firstly, the digital implementation will cause an inevitable time delay. In [BAE03A], the authors point out that there is commonly a one-sample-period time delay in order to achieve a full digital implementation. The time delay caused by the FOC algorithm is also approximated by half-sample-period. Thus, a total of 1.5 sample periods time delay is generated, assuming that the PWM signals are updated at each sampling point. Under high speed operation, the SFFR is low and the time delay becomes significant. The control performance will be deteriorated and the system may even be unstable [YIM09].

The control system is analysed in discrete domain in [YAN19A]. The effects of various discretization methods including forward difference method, backward difference method and centre difference method are compared in terms of their ability to maintain the system stability. The authors conclude that forward difference and the centre difference discretization methods can keep the system stable supposed that the time delay is compensated. In [YAN17], the position estimation model is considered in the discrete time domain and the error caused by the discrete time estimation is considered and compensated.

In order to achieve BLAC drives, the phase currents are needed to be sampled. The current linear approximation technique is usually used. This technique assumes that current changes linearly with supplying voltage so that the current sampled at the midpoint is the same as the mean current in one sample period [JAR19]. It is known that under practical digital implementation conditions, the sampling frequency is usually related with the PWM frequency. For high speed drives, the rotor covers substantial angular distance during one sample period

since the SFFR is low [JAR17]. The relationships between the sampled current and the supplying voltage are no longer linear due to the rotor movement. The linear approximation technique will thus cause current sampling error.

C. Current Harmonic Issues

The current harmonic problem will also become more severe for high speed drives considering the low SFFR and low motor inductance. There are mainly two types of current harmonics, i.e., the PWM related harmonics and the low order harmonics. The PWM related harmonics are generated due to the non-ideal PWM pattern [JAR11]. In high speed drives, the SFFR becomes small and may not even be an integer. The supplying voltages generated by traditional PWM techniques will become distorted and the currents will thus consist notable PWM related harmonics. Several different PWM techniques are presented and compared to solve the PWM related harmonics problem [STU12]. The low order harmonics are caused by several factors such as inverter nonlinearity and non-sinusoidal back-EMF. For a high speed motor, even a small distortion voltage will cause large current harmonics due to the low motor inductance [LIU19B]. A closed-loop current harmonic detection system and the corresponding harmonic compensation method is proposed in [LIU19B]. Since different non-ideal factors are coupled and hard to separate, in this thesis, an adaptive current harmonic suppression method will be proposed.

1.3.2 BLDC Control Strategies

Apart from BLAC drives, BLDC control strategies are also widely used in high speed drive systems. The block diagram of the high speed close loop BLDC control strategy is shown in Fig. 1.16.

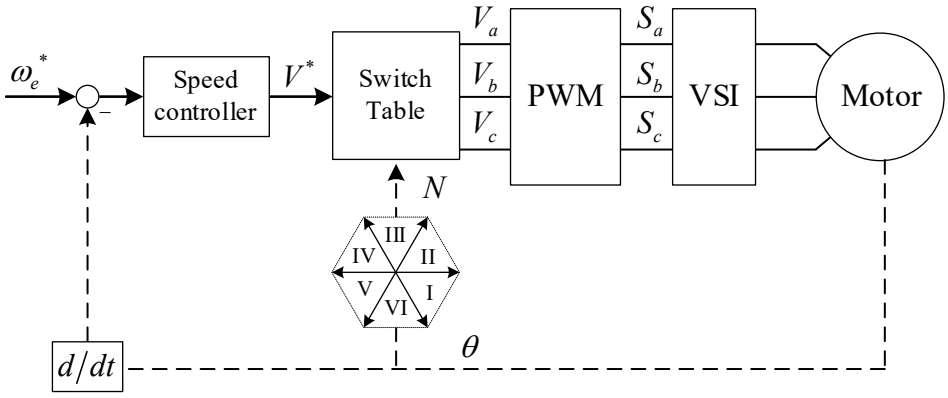


Fig. 1.16 Block diagram of the high speed close loop BLDC control strategy.

Unlike BLAC drives which need a continuous absolute position signal, only discrete commutation points are required to determine the sector number N and the corresponding switch table under BLDC drives so that the control complexity can be largely reduced.

1.3.2.1 Commutation Errors

The commutation errors are caused by mainly two factors, i.e. inaccuracy of detected position signals and phase delay effect.

A. Position Detection Errors

The accurate position signals are essential for high speed BLDC drives since the inaccurate commutation will cause unbalance operation, large current ripple, and low efficiency. The existing methods to detect the commutation points can be classified into two groups: sensorless methods and position sensor based methods.

Like BLAC drives, the back-EMF based sensorless methods are also suitable for high speed BLDC drives. The zero-crossing points (ZCPs) of the phase back-EMFs are usually used to obtain the commutation points. Ideally, the neutral point "n" of the motor is needed to obtain the phase voltage [LIU17] [CHE17A]. However, the access to the neutral point might be unavailable under some conditions. Thus, three Y-connected resistors are usually used to obtain the virtual neutral point "s" [LIH17B] as shown in Fig. 1.17.

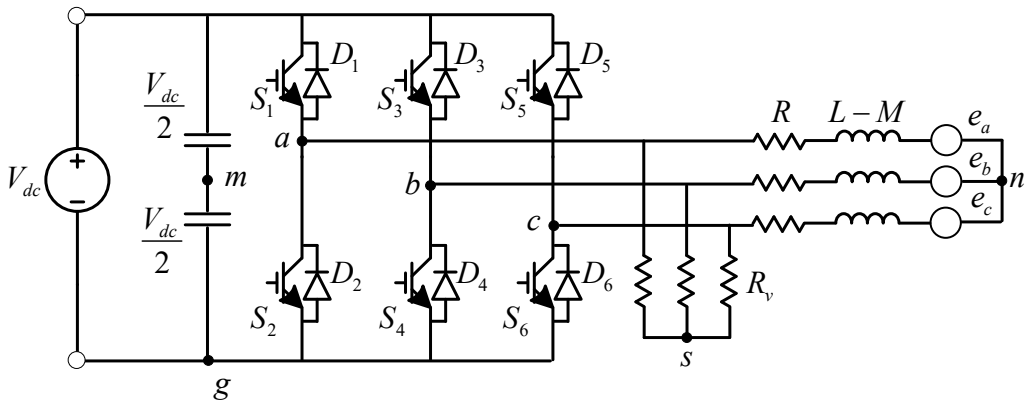


Fig. 1.17 Block diagram of VSI fed BLDC sensorless drive system. "n" is the neutral point, "s" is the virtual neutral point, "m" is the midpoint of the DC bus, "g" is the ground.

The midpoint of the DC bus "m" is also used for phase voltage detection in [ZHO19]. Besides, the ZCPs of the 3rd order back-EMFs can also be utilized for detecting the commutation points [YAN20B]. They can be obtained through the voltage difference between "n" and "s" [SHE04] [SHE06]. Similarly, the concept of virtual 3rd order back-EMFs is proposed in [CUI15B]

[SON18B] so that the neutral point is no longer needed. The virtual 3rd order back-EMFs are detected through the voltage difference between "s" and "m". Apart from the phase back-EMF, the line-to-line back EMF might also be used to obtain the commutation points since the amplitude of the line-to-line back EMF is larger than that of the phase back EMF [CHE18A] [LIU16]. The composition between different high speed back-EMF based sensorless methods is presented in [ZHO19].

However, one obvious drawback of the back-EMF based sensorless methods is the limitation of their use during start-up when the speed is low. Besides, when PWM techniques are used, the detected EMF signals must be filtered by low-pass filters (LPFs) in order to avoid false commutation. The use of LPFs will cause inevitable commutation delay error [LIW16]. The asymmetric machine parameters [YAN20B], PWM patterns [YAN20C], EMF shapes [CHE19] and armature reaction [SHE03] also have a negative influence on the accuracy of position signals. In order to eliminate the position detection errors during sensorless operation, various compensation methods based on DC current, phase current, phase back-EMF, 3rd order phase back-EMF and virtual 3rd order phase back-EMF have been proposed as summarized in Table 1.3.

Table 1.3 POSITION DETECTION ERROR COMPENSATION METHOD

Compensation method based on	*References*
DC current	*[ZHO17A]*
Phase current	*[CHE18A] [LIY20]*
Phase back-EMF	*[CHE17A] [CHE18B] [LIH17B] [LIW16] [ZHO17B] [ZHO18]*
3rd order phase back-EMF	*[SHE06]*
Virtual 3rd order phase back-EMF	*[LIU16] [SON18B]*

Discrete Hall sensors are also widely used to detect the commutation points in high speed BLDC drives. The Hall sensors have the advantages of simplicity and robustness in wide speed and load range [FAN14]. They are also insensitive to the motor parameter variation. Besides, the PWM signals introduces no high frequency noises on the Hall signals [CUI15A]. The Hall sensors will also not be influenced by the armature reaction since Hall sensors are usually

mounted on the end of windings [ZOU02]. The position detection errors are usually caused by the misplacement of Hall sensors in practical conditions [ALA08] and the uneven Hall signal effect [SEO17] which is caused by several reasons, such as the threshold effect of Hall sensor and the reduction of magnetic flux density. In this thesis, the commutation balancing strategy will be analysed and proposed for the Hall sensor based high speed BLDC drive.

B. Phase Delay Error

Apart from the position detection errors, the phase delay error has also been considered for high speed BLDC drives, especially in recent three years. The phase delay error is caused by the free-wheeling period of BLDC drive which leads to the phase current lagging behind the corresponding back-EMF [SHI17]. Under high speed drives, the long free-wheeling period will cause severe phase deviation which will undermine the control performance. In order to compensate the phase delay error, the commutation points should be shifted so that the current and the back-EMF are in phase. The phase delay problem in high speed BLDC drives is only addressed in limited research such as [GUC18], [TAN19] and [SON19]. In this thesis, this problem will be comprehensively analysed and compensated.

1.3.2.2 Other Issues

A. Digital Implementation Issues

Like BLAC drives, BLDC drives also face practical digital implementation issues during high speed operation. For a full digital implementation BLDC drive system, the voltage command generated by the speed controller is usually updated once in each PWM period. Thus, the practical commutation points are delayed from the detected ones. When the SFFR is low, this phenomenon becomes more severe. However, unlike BLAC drives where the PWM update delay can be approximated by 1.5 sample periods, the time delay of BLDC drives is not constant since the commutation signal may occur at any time during one PWM period [KIM02]. In [CUI15A], the time delay of high speed BLDC drives is analysed. Nevertheless, no compensation method is proposed. The authors, on the other hand, choose to utilize the PAM technique so that time delay caused by the digital implementation could be eliminated since the PWM chopper signals are no longer needed. In this thesis, a new PWM generation scheme will be proposed to eliminate the PWM update delay.

B. Wide Angle BLDC Drives

It should be noticed that for most BLDC drive systems, the 120° mode six-step control (120-SSC) strategy is usually used where inverter commutates every 60 electrical degrees. However,

this traditional BLDC control strategy will generate rectangular phase currents with large harmonic components. Thus, the concept of wide angle BLDC controls, which extends the conducting angle in order to generate quasi-sinusoidal currents, is considered [WAN07] as shown in Fig. 1.18.

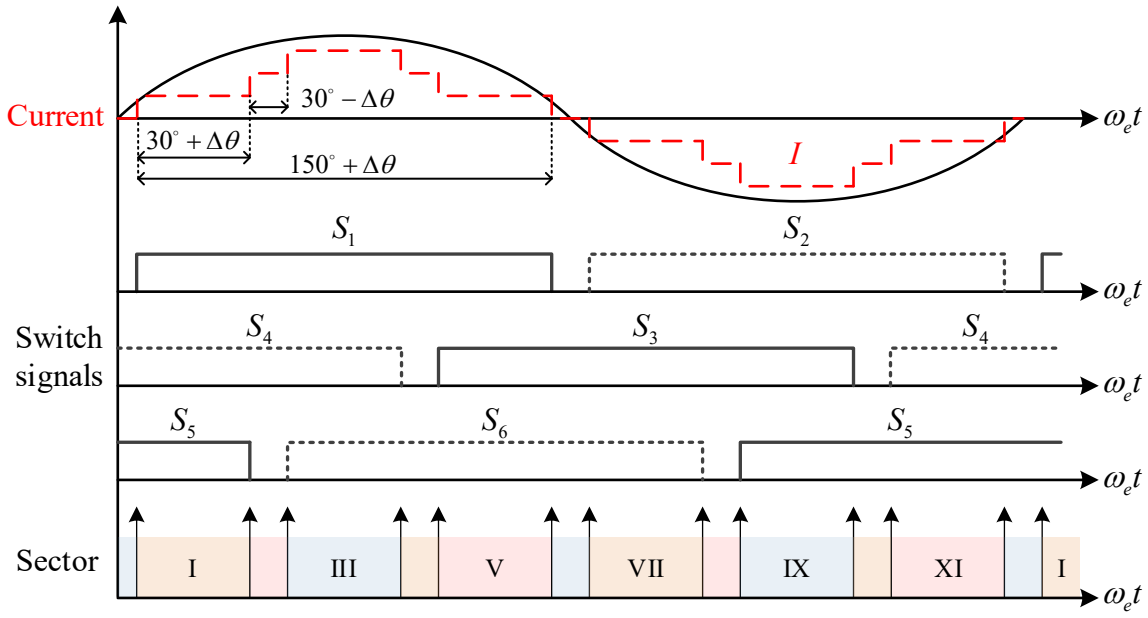


Fig. 1.18 Wide angle BLDC drive. [WAN07]

The wide angle BLDC drives are twelve-step control (TSC) strategies. The intervals of two continuous sectors are $30^\circ + \Delta\theta$ and $30^\circ - \Delta\theta$ respectively while the total commutation interval of each switch is $150^\circ + \Delta\theta$. $\Delta\theta$ can vary from -30° to 30°. When $\Delta\theta$ is zero, a symmetrical wide angle BLDC control is achieved. It is referred as the 150° mode TSC (150-TSC) in the [KAN11]. It is shown in [SAF95] that the control performance of the BLDC drive system can be improved by using wide angle BLDC control strategies. However, the use of wide angle BLDC control in high speed application can be rarely found in the previous research. In this thesis, the high speed wide angle BLDC control strategy will be analysed and exploited.

1.3.3 Comparison of High Speed Control Strategies

The comparison between high speed control strategies is given in Table 1.4.

Table 1.4 COMPARISON BETWEEN HIGH SPEED CONTROL STRATEGIES

Control strategies	Advantages and *disadvantages*
1. BLAC drives	a. Low current harmonics and torque ripple b. Reliable dynamic performance *c. High position signal requirement* *d. High control complexity*
2. BLDC drives	a. Low control complexity b. Low position signal requirement *c. Large current harmonics and torque ripple*

1.4 Scope of Research and Contributions of Thesis

1.4.1 Scope of Research

This thesis investigates and analyses both BLAC and BLDC control strategies of a high speed SPM slotted machine, with a particular focus on suppression of current harmonics and compensation of commutation errors. For BLAC drives, several non-ideal factors that could lead to current harmonics, including inverter nonlinearity and back-EMF harmonics, are investigated. For BLDC drives, both the position detection errors and the phase delay errors are considered so that the high speed drive system can achieve a balanced operation without commutation errors. The conclusions and findings of this thesis are validated by both simulation and experiments.

The research scope of this thesis and arrangement of chapters are shown in Fig. 1.19. The aims and contents of each chapter are summarised as follows:

Chapter 1

Aims: Literature review to identify the significances and necessities of this thesis.

This chapter reviews the relevant backgrounds and developments of high speed machine drive systems. Based on the controlled machine topology and practical conditions, the VSI is chosen for this thesis. The literature review on high speed drives shows that the current harmonic problems and the commutation errors are critical for BLAC and BLDC drives, while the

existing researches all have their limits. Various aspects for improving both BLAC and BLDC control performance still need to be systematically investigated.

Chapter 2

Aims: to investigate and suppress the current harmonics caused by the inverter nonlinearity of BLAC drive.

In this chapter, the inverter nonlinearity effect of BLAC drives will be comprehensively analysed. Based on the current harmonics analysis, an inverter nonlinearity compensation method is presented with simple signal processing algorithms. The proposed method uses currents in the synchronous reference frame to generate compensation voltages. The effectiveness of the proposed method is verified by experimental results.

Chapter 3

Aims: to suppress the current harmonics caused by the non-sinusoidal back-EMF of BLAC drive, with due account for inverter nonlinearity.

Following the analysis in the previous chapter, an adaptive linear neuron based current harmonics suppression method for BLAC drives considering non-sinusoidal back-EMF is presented, with due account for inverter nonlinearity. The feedforwarding compensation voltages can be adaptively generated without the knowledge of back-EMF components, inverter parameters and machine parameters. The analysis of current harmonics is also no longer needed. The proposed method has the ability to compensate the current harmonics caused by any periodic non-ideal factors. The effectiveness of the proposed method is verified by both simulation and experimental results.

Chapter 4

Aims: to develop a position signal error compensation method of BLDC drives.

In this chapter, the position detection errors of BLDC drives will be comprehensively investigated. Two types of Hall signal errors, i.e. misaligned and uneven Hall signal errors, are analysed and a Hall signal balancing strategy is developed to detect Hall signal errors and regenerate balanced Hall signals. In order to solve the PWM delay problem during high speed operation, a new PWM generation scheme is also proposed to eliminate the PWM update delay. Both simulation and experiment results have verified the effectiveness of the proposed strategy.

Chapter 5

Aims: to develop a phase delay error compensation method of BLDC drives using the d-axis current.

In this chapter, phase delay error of the BLDC drives is systematically investigated following the analysis of position detection errors in the previous chapter. The cause of the phase delay error is analysed, and a compensation strategy based on the d-axis current is proposed. A least mean square algorithm based filter is proposed to extract the d-axis current. The optimal phase advance angle is adaptively generated by reducing the filtered d-axis current to zero. The proposed method does not need the motor parameter information or additional hardware, and can be implemented in the general VSI. The effectiveness of the proposed strategy is verified by both simulation and experimental results.

Chapter 6

Aims: to develop a phase delay error compensation method of BLDC 150-TSC strategies using the stator current.

In this chapter, the 150-TSC strategy is utilized to reduce the current harmonics of BLDC drives. The phase delay error problem is further investigated and a compensation method without using the absolute position signal is proposed. The stator current is utilized as the criterion to determine the commutation errors in this chapter. The optimal phase advance angle is generated when the stator current magnitude is reduced to the minimum value with the help of the gradient descent optimization algorithm. The effectiveness of the proposed strategy is verified by simulation results.

Chapter 7

The general conclusions of this thesis and potential future work are summarised in this chapter.

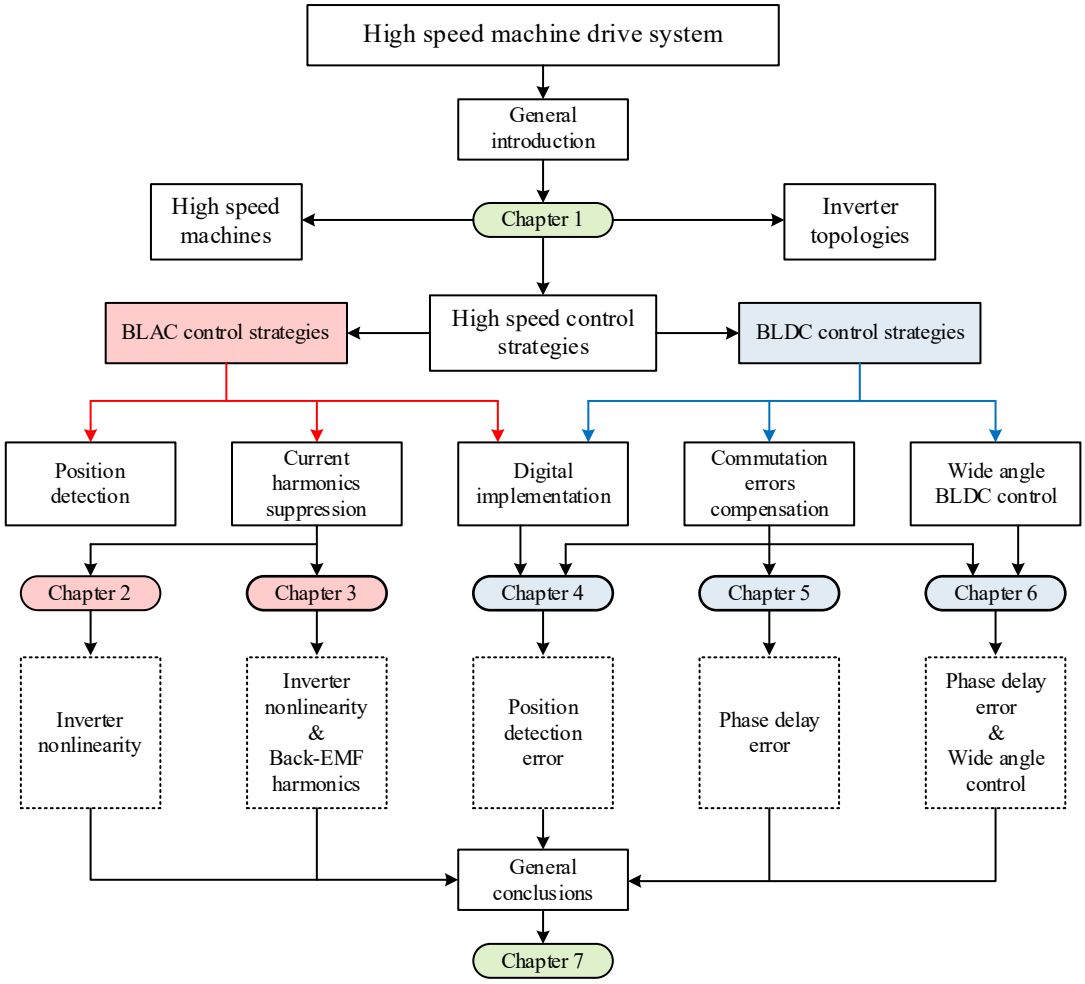


Fig. 1.19 Research scope and arrangement of chapters.

1.4.2 Main Contributions of Thesis

The contributions of this thesis are summarised as follows:

- The issues of current harmonics in BLAC drives are comprehensively analyzed considering the effects of different non-ideal factors. The inverter nonlinearity effect is compensated. An adaptive current harmonics suppression method that could suppress current harmonics caused by any periodic factors is also developed.
- The position signal caused commutation error in BLDC drives is investigated considering effects of both misaligned and uneven Hall signal errors. A position signal balancing strategy and a new PWM generation scheme is developed.
- The phase delay caused commutation error in BLDC drives is investigated. Two compensation strategies are proposed to generate the optimal phase advance angle without the use of the motor parameter information. The first one utilizes the d-axis

current while the second one chooses the stator current as criterion. The wide angle BLDC control strategy is also investigated for high speed drives.

1.4.3 List of Publications

Journal Publications:

[1] **L. Wang**, Z. Q. Zhu, B. Hong, and L. M. Gong, "Current harmonics suppression strategy for PMSM with non-sinusoidal back-EMF based on adaptive linear neuron method," *IEEE Trans. Ind. Electron*., DOI: 10.1109/TIE.2019.2955414.

[2] **L. Wang**, Z. Q. Zhu, B. Hong and L. M. Gong, "A commutation error compensation strategy for high speed BLDC drive based on Adaline filter," *IEEE Trans. Ind. Electron*., DOI: 10.1109/TIE.2020.2984445.

[3] **L. Wang**, Z. Q. Zhu, B. Hong and L. M. Gong, "A commutation optimization strategy for high speed brushless DC drives with inaccurate rotor position signals," *IET Electr. Power Appl.*, under review.

Conference Publication:

[4] **L. Wang**, Z. Q. Zhu, B. Hong and L. M. Gong, "A simple current harmonic analysis based dead time compensation method for permanent magnet synchronous machine drives," *in 10th Int. Conf. Power Electr. Mach. Drives*, Nottingham, UK, 2020.

CHAPTER 2

INVERTER NONLINEARITY COMPENSATION STRATEGY FOR BLAC DRIVES BASED ON CURRENT HARMONIC ANALYSIS

Both brushless alternating current (BLAC) drives and brushless direct current (BLDC) drives are widely used for permanent magnet (PM) brushless motors. The BLDC drives have the advantages of simple and robust structures at the cost of large torque ripples. The BLAC drives, on the other hand, have the advantages of low torque ripples and reliable dynamic performances with more complex control algorithms. In this thesis, the BLAC drives are used in low and medium speed range while the BLDC drives are used in high speed range.

For the voltage source inverters (VSIs) fed BLAC drives, the pulse width modulation (PWM) technique is commonly employed to adjust the motor speed. However, the inverter nonlinearity effect will cause voltage distortions which may deteriorate the control performance, especially in the low speed range. In this chapter, based on the analysis and minimization of current harmonics in the synchronous reference frame, an inverter nonlinearity compensation method is presented. The proposed method has the advantage of simple signal processing algorithms. It can use either the d-axis or the q-axis current to generate the compensation voltages. It should be noticed that the other non-ideal factors that cause current harmonics are not considered in this chapter since they will be analysed and compensated in Chapter 3. The proposed method is utilized in the low speed range where the inverter nonlinearity effect is dominant compared with other non-ideal factors. The effectiveness of the proposed method is verified by experimental results.

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2.1 Introduction

The BLAC drives are widely employed due to the advantages of low torque ripples and reliable dynamic performances. For the VSIs fed BLAC drives, the PWM technique is commonly employed to adjust the motor speed. However, the inverter nonlinearity effect will cause

voltage distortions which may result in the deterioration of control performance [PAR14A]. The inverter nonlinearity effect is caused by several practical characteristics of the power electronics devices. Firstly, a dead time should always be inserted in gate drive signals to prevent the shoot-through in DC link caused by the simultaneous conduction of both upper and lower switches. When the current flows through the power electronics devices, it will also cause voltage drops on both the switches and the diodes. Besides, for a practical power electronics device, there exists a turn-on/off delay between the instant when the device is commanded to switch and the instant when it is effectively fulfilled. It should also be noted that the inverter nonlinearity is also related with other, parasitic capacitance effect [GUE05], zero-current clamping effect [CHO95] and so on. Due to the inverter nonlinearity effect, the actual voltage outputs are distorted from the reference voltages [TAN17] [CHE08] [LIN09]. In recent years, various inverter nonlinearity compensation methods have been studied. These attempts could be categorized as follows.

Methods based on the average value theory reconstruct the PWM signals according to the error between the actual voltage outputs and the reference voltages with fixed compensation voltages. The first attempt of these methods is proposed in [SUK91], where an open-loop feedforward approach is used to produce the compensation signals. Another early attempt is presented in [CHO96], where an offline compensation method is proposed based on the characteristics of the inverter. However, this kind of compensation methods exhibits two challenges. Firstly, the physical characteristics of the inverters are not precisely known and may change with the operating conditions [PAR14B]. Many researches that consider different distortion factors of the inverters have been done. In [ZHA14] and [MAN15], the parasitic capacitance is considered and compensated. Nevertheless, these compensation methods are based on the limited sampling data and hard to achieve a precise compensation. In [WAN18B], a graphical solution of compensating voltage error is proposed in which all the voltage distortion factors are considered. However, it needs a current observer which depends on the accuracy of motor parameters. Secondly, for methods based on the average value theory, the accuracy of current direction information is vital. Nevertheless, the detected current is far from precise especially around zero current crossing area. Although many phase current reconstruction methods have been proposed [MUN99][WAN14][LIU17], they suffer from additional detection circuits and complex algorithm designs.

Methods based on the model observer estimate the voltage distortions caused by inverter nonlinearity. Rather than determining each voltage distortion factors and compensating them

separately, these methods are designed to obtain the total voltage errors and mitigate them together. Thus, these methods do not rely on the inverter characteristic information or operating conditions [KIM03A][KIM03B][BRA04][LIN02]. In [URA07], the q-axis disturbance voltage caused by the inverter nonlinearity is estimated, and the magnitude of inverter nonlinearity compensation voltage is adaptively determined. In [KIM10], an online inverter nonlinearity compensation method is proposed, and the disturbance voltage can be estimated without the use of tuneable parameters. In [LIA18], an adaptive second-order sliding-mode observer is proposed. Nevertheless, the feasibility of these methods heavily depends on the accuracy of motor parameters.

Methods based on the current harmonic analysis are also proposed in recent years. The inverter nonlinearity effect causes the 6^{th} order and its multiple current harmonics in the synchronous reference frame. By analysing the current harmonics, the compensation voltage can then be determined. This kind of compensation methods has the advantage of motor parameter independent. In [ZHA04], the current harmonics are minimized by comparing the 6^{th} order harmonic with the average value obtained by a moving average method. Only the steady state results are presented in [ZHA04]. In [HWA10], the integral term of d-axis current proportional-integral (PI) controller output is used to detect the harmonics. The inverter nonlinearity effect could be compensated by reducing and suppressing the integrator output. An additional limiter is used to suppress the excessive components during the transient state. Although this method is easy to implement, only the integrator output of d-axis PI controller output can be used for this method. The q-axis PI controller output cannot be used since it contains a DC component. The difference between the maximum and minimum values of the d-axis current is used in [PAR14B] to obtain the peak-to-peak value of current over 1/6 of the periodicity. An additional PI controller is then used to reduce the peak-to-peak value of current to zero in order to compensate the inverter nonlinearity effect. The peak-to-peak values of current over 1/6 of the periodicity can only be obtained under the steady state in [PAR14B]. However, it should be noted that the precise maximum and minimum values of the d-axis current are hard to obtain.

In this chapter, a motor-parameter-independent inverter nonlinearity compensation method based on the current harmonic analysis is presented. The proposed method compensates the inverter nonlinearity effect by minimizing the current harmonics in the synchronous reference frame. The proposed method is easy to implement since it does not need the complicated signal processing algorithms. It also does not rely on the knowledge of any motor parameters or

inverter characteristic information. The effectiveness of the proposed method is verified by experimental results.

2.2 Inverter Nonlinearity Effect Analysis

The voltage equations of BLAC drive can be expressed as

$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = R \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{2-1}$$

where R is the stator resistance, L and M are the self and mutual winding inductances. $U_{an,bn,cn}$, $I_{a,b,c}$ and $e_{a,b,c}$ are the three phase supply voltages, phase currents and phase back-electromotive forces (EMFs), respectively. A typical three phase half-bridge inverter fed BLAC drive topology is shown in Fig. 2.1.

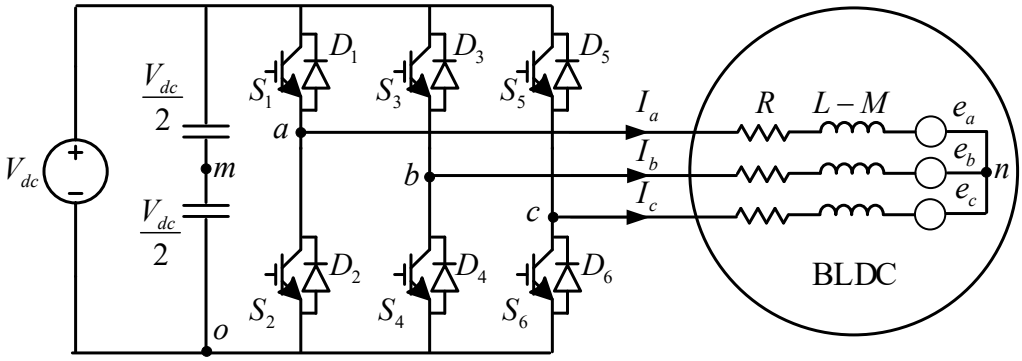


Fig. 2.1. Topology of three phase half-bridge inverter.

Phase A of the inverter is shown in Fig. 2.2 for further analysis.

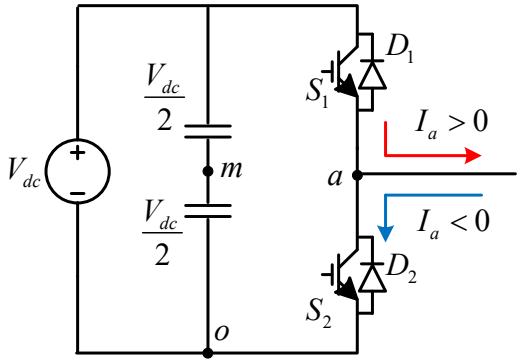


Fig. 2.2. Definition of current direction.

The current direction is defined as follows. When the current flows from the inverter to the motor, the current is defined as positive. Otherwise, it is defined as negative.

2.2.1 Dead Time Effect

In order to prevent shoot-through in the DC link, a dead time T_{dt} is needed for BLAC drive. The purpose of the inserted dead time is to make sure the switches which are demanded to turn off have been switched off effectively. During the dead time, both the upper and lower switches on one leg are turned off and the current flows through the anti-parallel diodes. Take phase A current for example, when the current is positive, it flows through D_2, otherwise, the current flows through D_1 which makes the output voltage distorted from the ideal case.

2.2.2 Turn-On/Off Delay

For a practical power electronics device, there exists a time delay between the instant when the device is commanded to switch and the instant when it is effectively fulfilled. Besides, a gate drive circuit is usually needed to amplify the PWM control signals that drive the power electronics devices. There will also introduce an inevitable time delay. The turn-on delay T_{on} is defined as the overall delay between the turn-on drive signal and effectively fulfilled switch-on state. The turn-off delay T_{off} can be defined accordingly. Together with the dead time effect, a voltage distortion will be generated.

Still taking phase A for example, the switch pattern and the voltage distortion caused by the dead time effect and the turn on/off delay when $I_a > 0$ are presented in Fig. 2.3. The dead time effect and the turn on/off delay when $I_a < 0$ are presented in Fig. 2.4. The terminal voltage V_{ao}, the drive signals $S_{1,2}$ and the terminal voltage distortion ΔV_{ao_dead} are shown accordingly.

As shown in the figures, the voltage distortion varies with the phase current polarity. Taking phase A for example, it could be expressed as

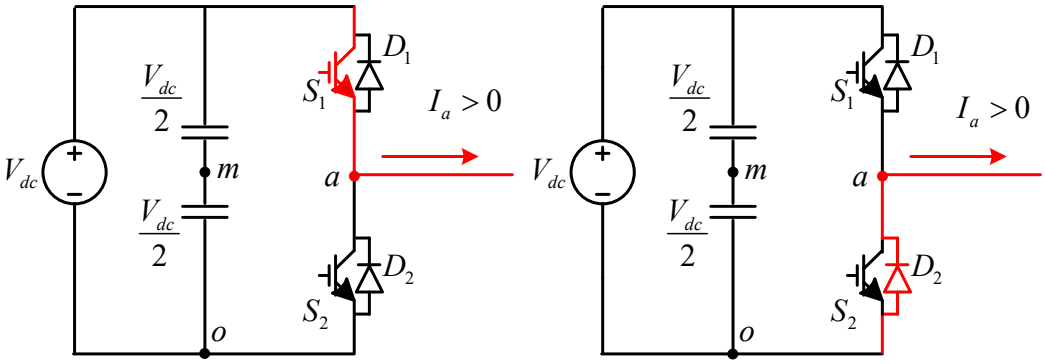
$$\Delta V_{ao\_dead} = -V_{dead} sign(I_a) \tag{2-2}$$

where

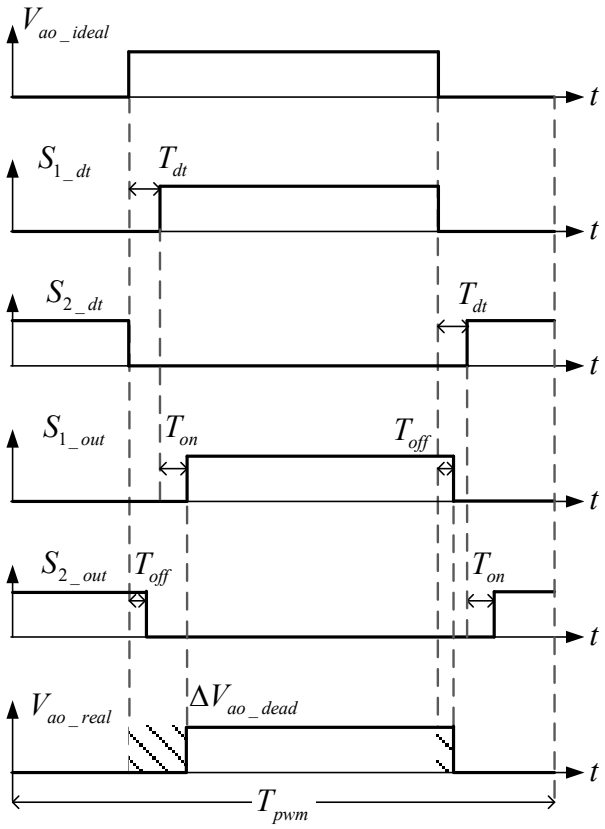
$$V_{dead} = \frac{T_{dead} + T_{on} - T_{off}}{T_{pwm}} V_{dc} \tag{2-3}$$

$$sign(I_a) = \begin{cases} 1 & I_a > 0 \\ -1 & I_a < 0 \end{cases} \tag{2-4}$$

T_{pwm}, V_{dc} and I_a are the PWM period, the DC voltage and the phase A current, respectively. Phase B and Phase C terminal voltage distortions can be expressed as ΔV_{bo_dead} and ΔV_{co_dead} accordingly. It is obvious that the terminal voltage distortion is related with the DC supply voltage and the PWM frequency.

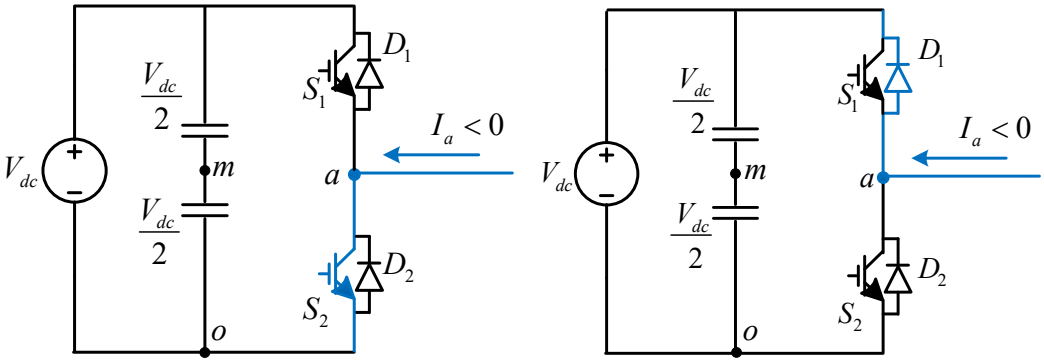


(a) Switching pattern.

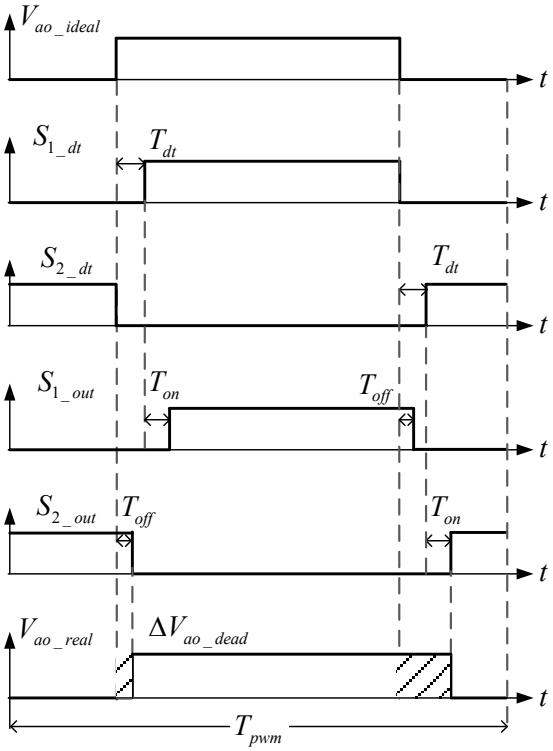


(b) Output voltage.

Fig. 2.3. Dead time effect and turn-on/off delay when $I_a > 0$.



(a) Switching pattern.



(b) Output voltage.

Fig. 2.4. Dead time effect and turn-on/off delay when $I_a < 0$.

2.2.3 Voltage Drops on Power Electronics Devices

When the current flows through a power electronics device, there will be a voltage drop. Taking phase A for example, based on the power electronics device properties, the voltage drops on the switches and the diodes can be expressed as [CHO96]

$$V_{se} = V_{se\_th} + R_{se} I_a \tag{2-5}$$

$$V_{de} = V_{de\_th} + R_{de} I_a \tag{2-6}$$

where V_{se_th}, V_{de_th} R_{se} and R_{de} are the threshold voltages and the equivalent resistances of the switches and the diodes accordingly. Thus, the terminal voltage drop on the power electronics devices can be expressed as

$$\Delta V_{ao\_drop} = -\frac{1}{2}(V_{se\_th} + V_{de\_th}) sign(I_a) - \frac{1}{2}(R_{se} + R_{de}) I_a \tag{2-7}$$

As shown in the equation, the voltage drop error composes of two parts. The first term acts like the voltage distortion caused by the dead time and turn-on/off delay, while the second term has the same property as the stator resistor. Thus, the second term can be combined to the overall stator resistance. Then, the terminal voltage drop can be simplified as

$$\Delta V_{ao\_drop} = -\frac{1}{2}(V_{se\_th} + V_{de\_th}) sign(I_a) \tag{2-8}$$

2.2.4 Parasitic Capacitance Effect

The parasitic capacitance of the power electronics devices is shown in Fig. 2.5.

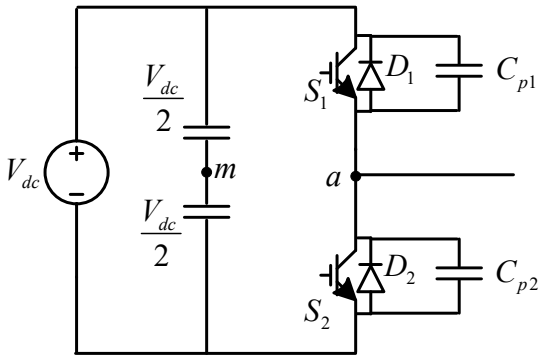
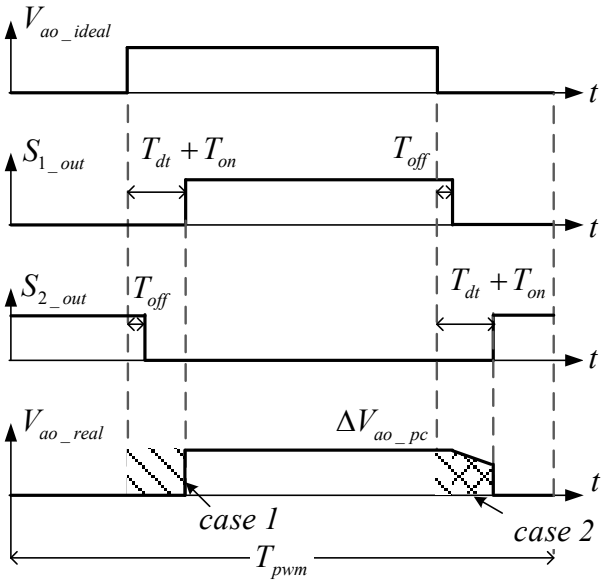
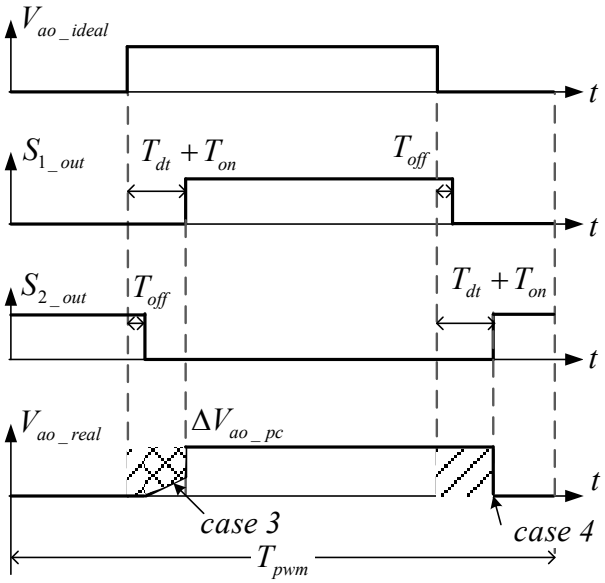


Fig. 2.5. Parasitic capacitance of the power electronics device.

Due to the parasitic capacitance, the phase output voltage cannot change instantly [GUE05]. Considering the phase current polarity and the output voltage, there are four different cases as shown in Fig. 2.6.



(a) Parasitic capacitance effect when $I_a > 0$.



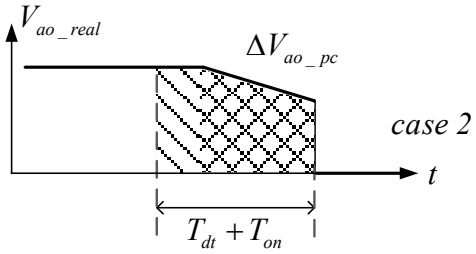
(b) Parasitic capacitance effect when $I_a < 0$.

Fig. 2.6. Voltage distortion caused by the parasitic capacitance effect.

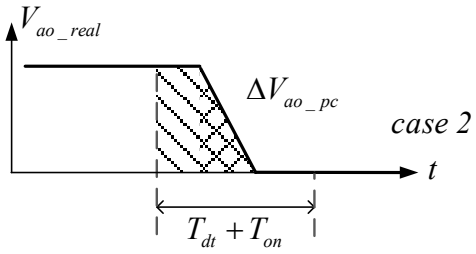
The terminal voltage distortion ΔV_{ao_pc} caused by the parasitic capacitance effect is shown in Fig. 2.6. Under case 1 and case 4, the current transfers from the diodes to the switches. The phase current is positive under case 1 and is negative under case 4. Since the switches provide a low resistance path, the charging and discharging of the parasitic capacitance can be relatively fast. Thus, the phase voltage slope is very sharp.

However, under the condition of case 2 and case 3, the current transfers from the switches to the diodes. Taking case 2 for example, after S_1 is turned off, the phase current starts to charge the parasitic capacitance C_{p1}. Thus, the phase voltage cannot reduce to zero instantly. The falling slope of the phase voltage is significantly dependent on the current level. The case 3 can be analysed accordingly.

It should be noticed that there might be two different output voltage profiles based on the different voltage falling slopes as shown in Fig. 2.7. Still taking case 2 for example, at the end of dead time, the phase voltage might be higher than zero as shown in Fig. 2.7(a). Under this circumstance, the voltage is then forced to zero. If the phase output voltage has already fallen down to zero before the dead time, then the lower diode D_2 provide the current flow path so that the phase output voltage is kept as zero until the end of dead time as shown in Fig. 2.7(b). The case 3 can then be analysed accordingly.



(a) Phase voltage is higher than zero at the end of dead time.



(b) Phase voltage reaches zero before the end of dead time.

Fig. 2.7. Different voltage profiles of case 2.

It is known that the voltage distortion caused by the parasitic capacitance effect will increase with the increase of phase current and will be saturated at high current [XUL14]. The saturation value V_{pc} is related with the inverter property, the DC voltage and PWM frequency. The parasitic capacitance effect error under saturation condition can be expressed as

$$\Delta V_{ao\_pc} = -V_{pc} sign(I_a) \tag{2-9}$$

At lower current condition, however, the current value and parasitic capacitance will have significant influence on the parasitic capacitance effect error.

2.2.5 Voltage Distortion Analysis in Synchronous Reference Frame

The total voltage distortion caused by the inverter nonlinearity effect is the sum of all the aforementioned factors. Taking phase A for example, the total phase A terminal voltage distortion ΔV_{ao} can be expressed as

$$\Delta V_{ao} = \Delta V_{ao\_dead} + \Delta V_{ao\_drop} + \Delta V_{ao\_pc} = -V_{inv\_non} sign(I_a) \tag{2-10}$$

where V_{inv_non} is determined by the inverter properties. Then, the phase voltage distortions caused by the inverter nonlinearity effect can be derived from the terminal voltage distortions and can be expressed as [KIM07].

$$\begin{bmatrix} \Delta V_{an} \\ \Delta V_{bn} \\ \Delta V_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} \Delta V_{ao} \\ \Delta V_{bo} \\ \Delta V_{co} \end{bmatrix} \tag{2-11}$$

Taking phase A for example, the relationship between the phase voltage distortion and the phase current is shown in Fig. 2.8.

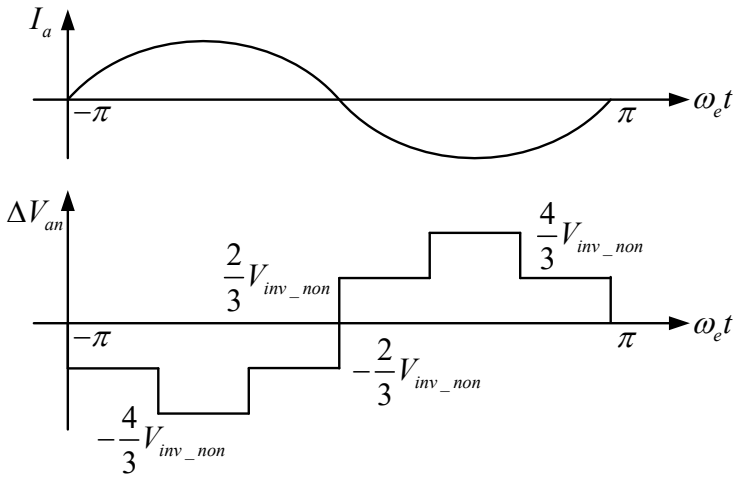


Fig. 2.8. Relationship between phase current and phase voltage distortion.

Employing the Fourier series analysis, the phase voltage distortion can be derived as

$$\Delta V_{an} = -\frac{4V_{inv\_non}}{\pi}\left[\begin{matrix}cos(\delta)\\ +\sum_{n=6k}\left\{\frac{cos[(n-1)\delta]}{n-1} - \frac{cos[(n+1)\delta]}{n+1}\right\}\end{matrix}\right] \tag{2-12}$$

where δ is the angle between the current vector and the a-axis. The coordination transformation function from the a-b-c axis frame to the d-q axis frame can be expressed as

$$C_{abc}^{dq} = \frac{2}{3}\begin{bmatrix} cos\,\omega_e t & cos(\omega_e t - \frac{2}{3}\pi) & cos(\omega_e t + \frac{2}{3}\pi) \\ -sin\,\omega_e t & -sin(\omega_e t - \frac{2}{3}\pi) & -sin(\omega_e t + \frac{2}{3}\pi) \end{bmatrix} \tag{2-13}$$

Assuming that

$$\delta = \omega_e t + \frac{1}{2}\pi + \gamma \tag{2-14}$$

where γ is the angle between the current vector and the q-axis. Then, the voltage distortions in d-q reference frame ΔV_d and ΔV_q can be expressed as

$$\begin{aligned}\Delta V_d &= \frac{4V_{inv\_non}}{\pi}\left\{\begin{matrix}sin(\gamma)\\ +\sum_{n=6k}\left\{\frac{sin[n(\omega_e t+\gamma)-\gamma]}{n-1} + \frac{sin[n(\omega_e t+\gamma)+\gamma]}{n+1}\right\}\end{matrix}\right\}\\ \Delta V_q &= \frac{4V_{inv\_non}}{\pi}\left\{\begin{matrix}-cos(\gamma)\\ +\sum_{n=6k}\left\{\frac{cos[n(\omega_e t+\gamma)-\gamma]}{n-1} - \frac{cos[n(\omega_e t+\gamma)+\gamma]}{n+1}\right\}\end{matrix}\right\}\end{aligned} \tag{2-15}$$

After combining the same order harmonic terms, (2-15) can be expressed as

$$\begin{aligned}\Delta V_d &= \frac{4V_{inv\_non}}{\pi}\left\{\begin{matrix}sin(\gamma)\\ +\sum_{n=6k}\left\{\frac{2\sqrt{n^2\,cos^2(\gamma)+sin^2(\gamma)}}{(n-1)\times(n+1)}sin[n(\omega_e t+\gamma)+\delta_d]\right\}\end{matrix}\right\}\\ \Delta V_q &= \frac{4V_{inv\_non}}{\pi}\left\{\begin{matrix}-cos(\gamma)\\ +\sum_{n=6k}\left\{\frac{2\sqrt{n^2\,sin^2(\gamma)+cos^2(\gamma)}}{(n-1)\times(n+1)}cos[n(\omega_e t+\gamma)+\delta_q]\right\}\end{matrix}\right\}\end{aligned} \tag{2-16}$$

where

$$\delta_d = arctan\frac{sin\,(\gamma)}{ncos\,(\gamma)}$$
$$\delta_q = arctan\frac{nsin\,(\gamma)}{cos\,(\gamma)} \tag{2-17}$$

As shown in (2-16), all multiples of the 6th harmonic are considered in the equation. For simplicity, only the 6th order harmonic is further considered since the magnitudes of rest harmonics are negligible compared with the 6th order one. Then, the equations of ΔV_d and ΔV_q can be further simplified as

$$\Delta V_d = \frac{4V_{inv\_non}}{\pi}\left\{\begin{matrix} sin(\gamma) \\ +\frac{2\sqrt{36\,cos^2(\gamma)+sin^2(\gamma)}}{35}sin[6\omega_e t+(6\gamma+\delta_d)] \end{matrix}\right\}$$
$$\Delta V_q = \frac{4V_{inv\_non}}{\pi}\left\{\begin{matrix} -cos(\gamma) \\ +\frac{2\sqrt{36\,sin^2(\gamma)+cos^2(\gamma)}}{35}cos\left[6\omega_e t+\left(6\gamma+\delta_q\right)\right] \end{matrix}\right\} \tag{2-18}$$

The voltage harmonics will then result in phase current harmonics. Based on (2-1) and (2-17), the current harmonics caused by the inverter nonlinearity effect in the d-q reference frame can be expressed as

$$\Delta I_d = \frac{4V_{inv\_non}}{\pi}\left[\frac{sin(\gamma)}{R}+\frac{2\sqrt{36\,cos^2(\gamma)+sin^2(\gamma)}}{35Z_6^d}sin(\,6\omega_e t+(6\gamma+\delta_d))\right]$$
$$\Delta I_q = \frac{4V_{inv\_non}}{\pi}\left[\frac{-cos(\gamma)}{R}+\frac{2\sqrt{cos^2(\gamma)+36\,sin^2(\gamma)}}{35Z_6^q}cos(\,6\omega_e t+\left(6\gamma+\delta_q\right))\right] \tag{2-19}$$

where

$$Z_6^d = \sqrt{R^2+(6\omega_e L_d)^2}$$
$$Z_6^q = \sqrt{R^2+(6\omega_e L_q)^2} \tag{2-20}$$

As shown in (2-19), the inverter nonlinearity effect introduce both the DC component and the 6th order component in the d-q reference frame. Although the DC distortion component will not lead to current harmonics, the 6th order voltage distortion caused by the inverter nonlinearity effect will inevitably cause current harmonics.

2.3 Proposed Inverter Nonlinearity Compensation Method

It is known from [KIM07][HWA10] and (2-19) that the magnitudes of harmonic components of I_d and I_q change simultaneously if the inverter nonlinearity compensation is employed. Thus, by minimizing the harmonic components of either I_d or I_q, the optimal compensating voltages could be obtained, and the inverter nonlinearity effect could then be compensated. In this chapter, an inverter nonlinearity compensation method based on the current harmonic analysis is presented. A simple signal processing algorithm is proposed to obtain the magnitude of the harmonic components. The proposed method could use either the d-axis or the q-axis current to generate the compensation voltages. The proposed method firstly separates the harmonic components from the DC component and then obtain the magnitude information of the harmonic components through the absolute value function. The block diagram of the BLAC drive system considering inverter nonlinearity effect is shown in Fig. 2.9. E stands for the fundamental component of the back-EMF in the synchronous reference frame. I_{dq}^* and V_{dq}^* are the reference currents and voltages respectively. ΔV_{dq} are the voltage distortions as analysed in (2-18).

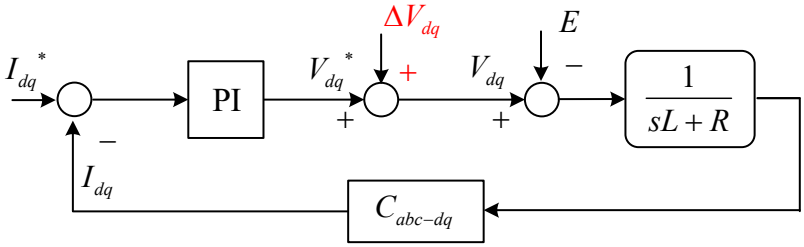


Fig. 2.9. Block diagram of BLAC drive system considering inverter nonlinearity effect.

The q-axis current I_q is used as an example to show the effectiveness of the proposed method. Based on (2-1) and (2-19), the q-axis current considering inverter nonlinearity effect can be expressed as

$$I_q = I_q^* + \Delta I_q = I_{q\_DC} + I_{q\_har} = K_q + K_{q\_har}\, cos\left[6\omega_e t + \left(6\gamma + \delta_q\right)\right] \tag{2-21}$$

where K_q is the DC component of I_q considering the inverter nonlinearity effect. It can be expressed as

$$K_q = I_q^* - \frac{4V_{inv\_non}\, cos(\gamma)}{\pi R} \tag{2-22}$$

K_{q_har} is the magnitude of the 6th order harmonic determined by the inverter nonlinearity effect. It can be obtained from (2-19)

$$K_{q\_har} = \frac{8V_{inv\_non}\sqrt{cos^2(\gamma) + 36\,sin^2(\gamma)}}{35\pi Z_6^q} \tag{2-23}$$

In order to separate the DC component and the harmonic components, the q-axis current I_q is firstly processed through a high-pass-filter (HPF) so that the DC component I_{q_DC} is eliminated, and the resulting output signal contains only the 6th order harmonic I_{q_har}. The HPF is easy to design since it only need to eliminate the DC component.

It is worth noting that only the magnitude of the 6th order harmonic is needed to obtain the compensation voltage. Thus, the output signal of the HPF is further processed. Firstly, an absolute value function is used to convert the negative part of the 6th order harmonic into positive one. After processed by the absolute value function, the 6th order harmonic I_{q_har} will become $I_{q\_har\_abs}$. Then, a low-pass-filter (LPF) is used to obtain the magnitude information Mag_{q_har}. The whole signal processing is expressed as

$$Mag_{q\_har} = LPF\{abs[HPF(I_q)]\} \tag{2-24}$$

where abs stands for the absolute value function. Then, the magnitude information of the current harmonic can be used as the factor to compensate the inverter nonlinearity effect. The block diagram of the proposed current magnitude information extraction method is shown in Fig. 2.10.

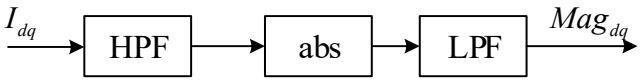


Fig. 2.10. Block diagram of the proposed current magnitude information extraction method.

The current harmonic magnitude information extraction process is simulated in the MATLAB/Simulink as presented in Fig. 2.11. The motor is operating at $\omega_e = 100\pi$ rad/s ($f = 50$ Hz) under the rated load (0.24 Nm). In the simulation model, the PWM switching frequency is set to 20 kHz while the dead time is set to 1.5μs. The cut-off frequency of the HPF and LPF in the proposed method are chosen as 10 Hz and 5 Hz.

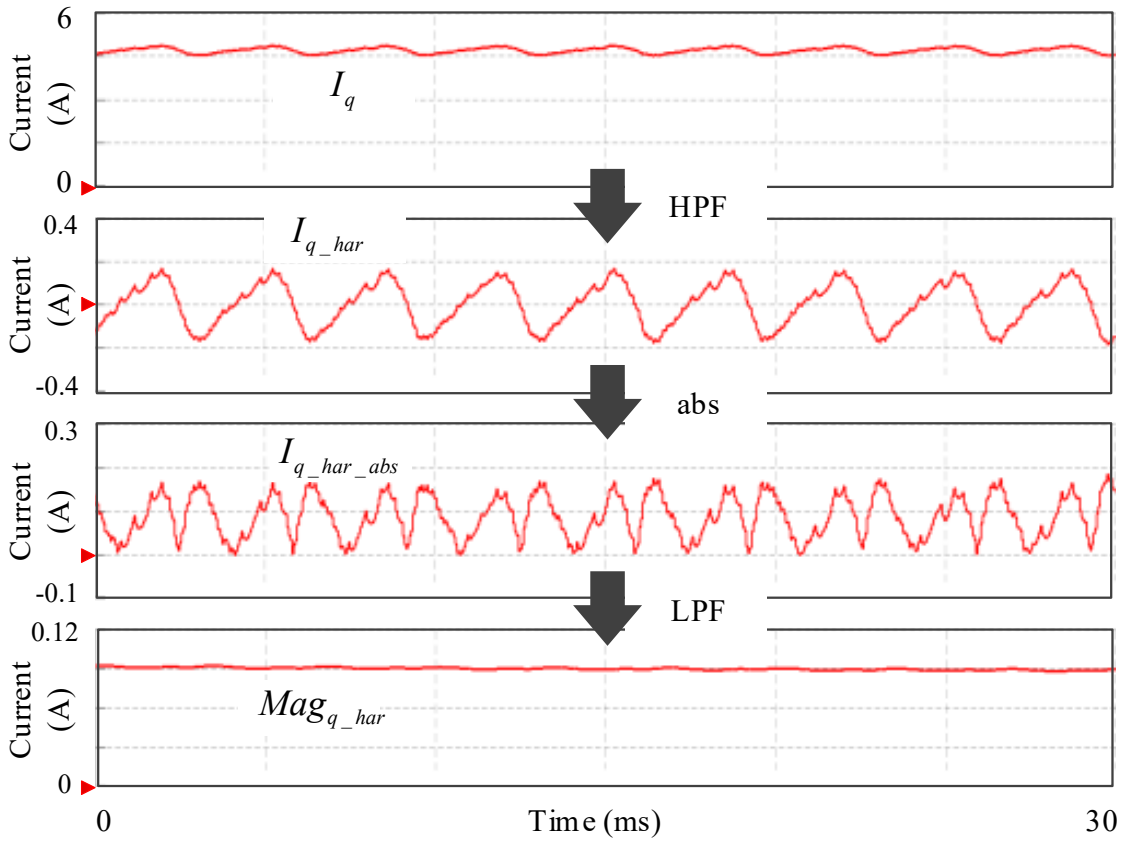


Fig. 2.11. Extraction of current harmonic magnitude information.

As shown in Fig. 2.11, the magnitude information of the 6th order current harmonic introduced by the inverter nonlinearity effect can be obtained while the higher order harmonics are neglected. Then, the compensation voltages can be obtained by reducing the magnitude of current harmonic to zero. In a practical system, it is difficult to completely eliminate the current harmonics, especially when there also exist other non-ideal factors that could lead to current harmonics. Nevertheless, in the low speed range, the inverter nonlinearity effect is dominant compared with other factors. The current harmonics could still be well suppressed with the proposed method. The effects of other non-ideal factors are considered later in Chapter 3. The compensation voltage can be expressed as

$$V_{ff\_q} = \alpha V_{com\_q} \tag{2-25}$$

where V_{com_q} is the fixed compensation voltage and α is the compensation factor. The fixed compensation voltage can be expressed as

$$V_{com\_q} = V_{dead}\, cos(6\omega_e t) \tag{2-26}$$

where V_{dead} can be obtained depending on the inverter characteristics [LIU17] based on (2-3). A PI controller is used to obtain the compensation voltage factor α. The factor can be determined as

$$\alpha = \left(k_{p\_inv} + \frac{1}{s} k_{i\_inv}\right) Mag_{q\_har} \tag{2-27}$$

The compensation factor is calculated in the direction of reducing the current harmonics under steady state. When the condition $Mag(k) \geq Mag(k-1)$ meets, the tuning process is completed, and the compensation factor is determined. The PI tuning factors k_{p_inv} and k_{i_inv} can be experimentally obtained considering the practical system design. The d-axis compensation voltage V_{ff_d} can be obtained in the same way accordingly. The block diagram of the proposed inverter nonlinearity compensation is shown in Fig. 2.12.

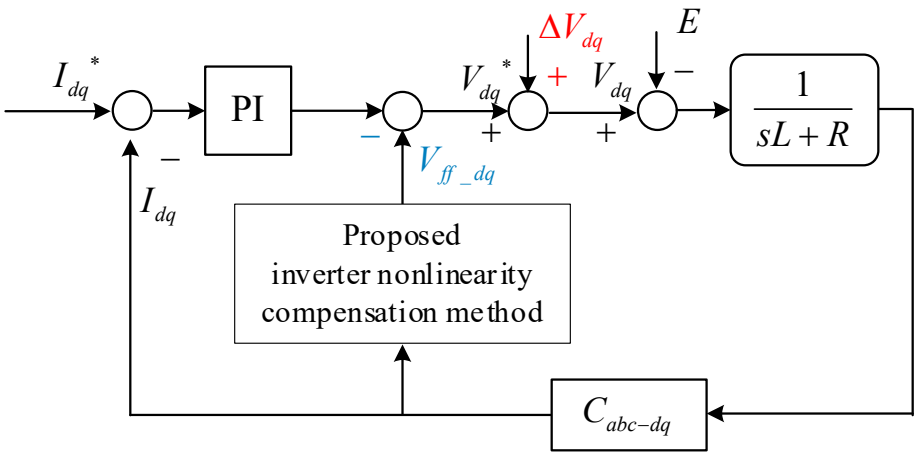


Fig. 2.12 Block diagram of the proposed inverter nonlinearity compensation method.

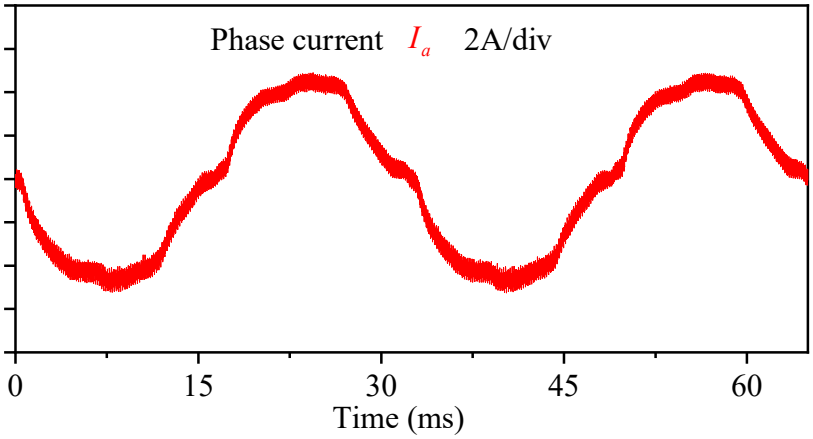
2.4 Experimental Verification

2.4.1 Steady State Experimental Results

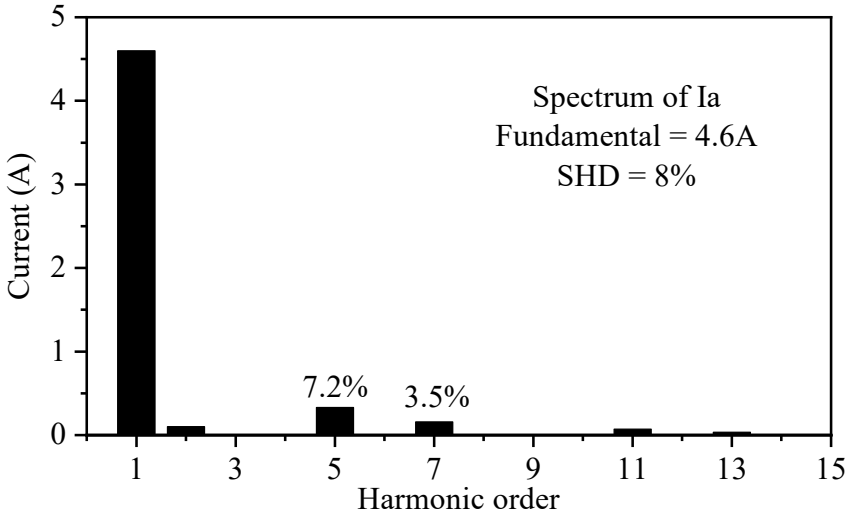
The test rig setup is presented in the Appendix. The DC supply voltage is 100V. A fast Fourier transform is used to analyse the current waveforms and obtain the current spectra. The measured phase current waveforms and corresponding spectra with and without inverter nonlinearity compensation method under different conditions as shown in Fig. 2.13-2.18. The inverter nonlinearity effect mainly introduces the 6th order in the d-q reference frame. Based on the transformation equation, the nth order harmonics in d-q reference frame will become the (n-1)th order and (n+1)th order harmonics in a-b-c reference frame. In this chapter, the 5th and

7th harmonics in a-b-c reference frame are considered and chosen as the factor to verify the effectiveness of the proposed compensation method. The selective harmonic distortion (SHD) is defined as

$$SHD = \frac{\sqrt{I_5^2 + I_7^2}}{I_1} \tag{2-28}$$



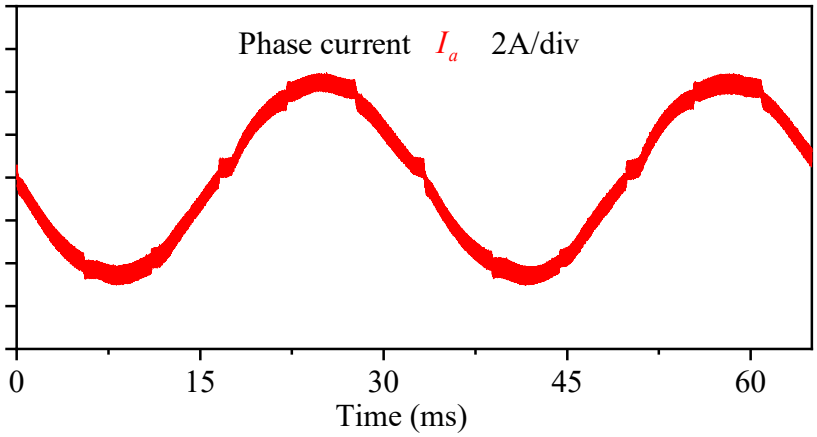
(a) Phase current waveform.



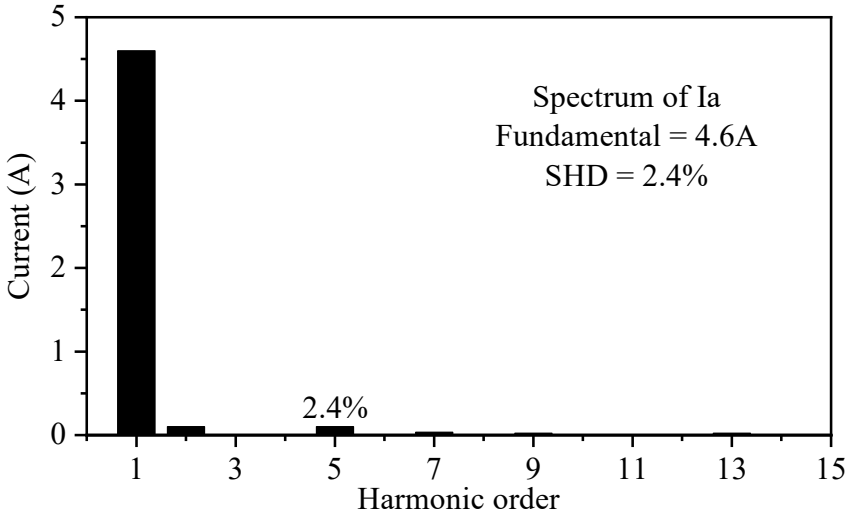
(b) Phase current spectrum.

Fig. 2.13. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 66.7\pi$ rad/s ($f_e = 33.3$ Hz) at rated load without inverter nonlinearity compensation method. The dead time is set to 1.5μs.

Fig. 2.13 and Fig. 2.14 show the experimental results of phase current waveforms and current harmonic spectra without and with the proposed inverter nonlinearity compensation method when the motor is operating at $\omega_e = 66.7\pi$ rad/s ($f_e = 33.3$ Hz) under the rated load. The dead time is set to 1.5μs under this condition.



(a) Phase current waveform.

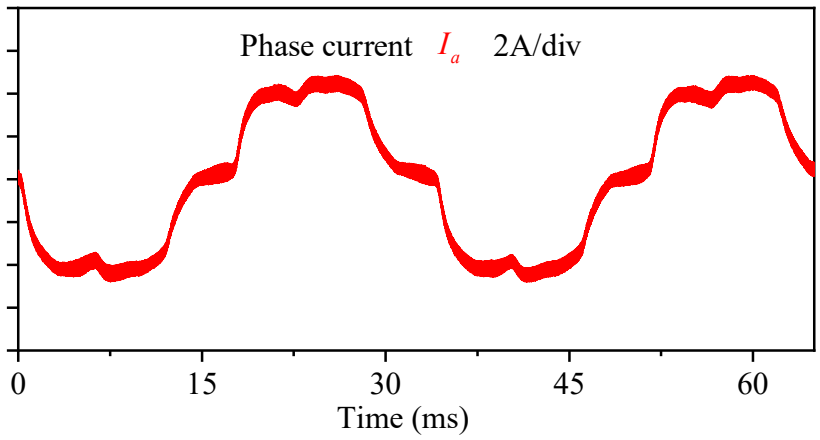


(b) Phase current spectrum.

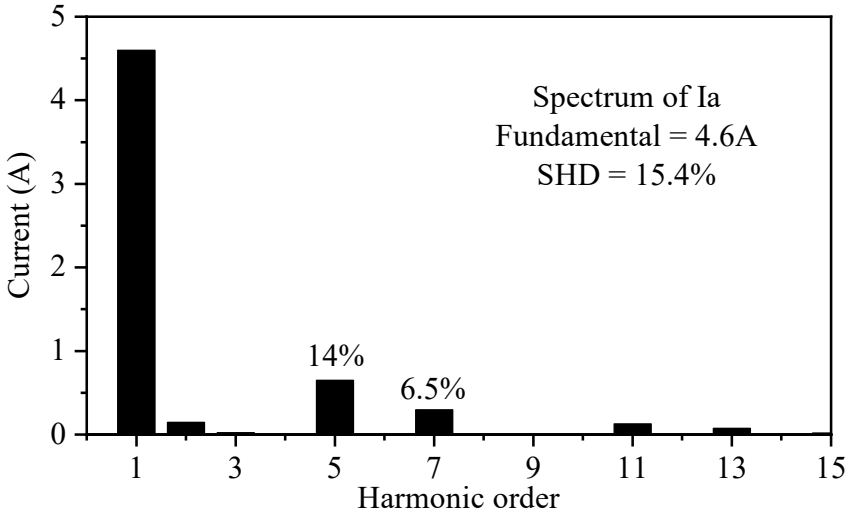
Fig. 2.14. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 66.7\pi$ rad/s ($f_e = 33.3$ Hz) at rated load with the proposed inverter nonlinearity compensation method. The dead time is set to 1.5μs.

Without inverter nonlinearity compensation, the phase current is seriously distorted as shown in Fig. 2.13. The phase current contains the dominant 5th and 7th harmonics. After the proposed compensation method is employed, the inverter nonlinearity effect are well compensated as

shown in Fig. 2.14. It can be seen that. The SHD of without and with inverter nonlinearity effect compensation are 8% and 2.4%, respectively. Compared with no nonlinearity effect compensation, the proposed method can decrease the harmonic distortion by 71%.



(a) Phase current waveform.

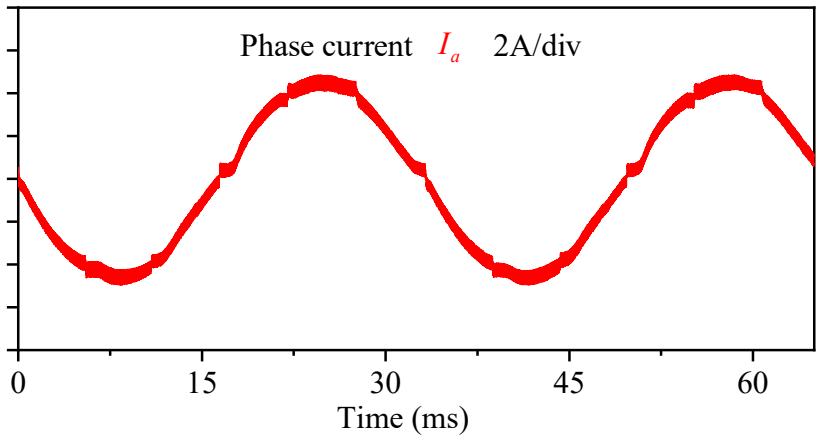


(b) Phase current spectrum.

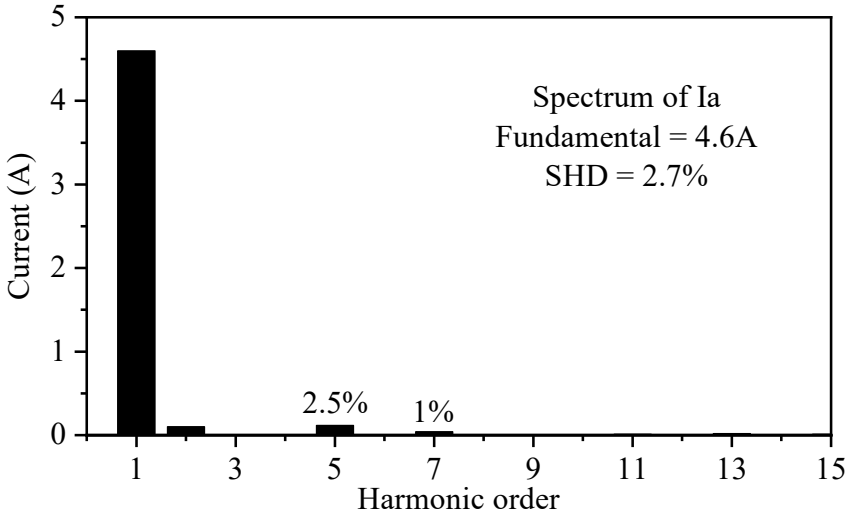
Fig. 2.15. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 66.7\pi$ rad/s ($f_e = 33.3$ Hz) at rated load without inverter nonlinearity compensation method. The dead time is set to 3μs.

Fig. 2.15 and Fig. 2.16 show the current waveforms and spectra when the dead time is set to 3μs. The motor is still operating at $\omega_e = 66.7\pi$ rad/s ($f_e = 33.3$ Hz) at rated load. In Fig. 2.15, the current waveform and spectrum without any inverter nonlinearity compensation is presented. Since the dead time is increased, the inverter nonlinearity effect becomes more

obvious compared with the previous condition. The current SHD increases from 8% to 15.4% while the 5th and 7th order harmonics increase from 7.2% and 3.5% to 14% and 6.5%.



(a) Phase current waveform.

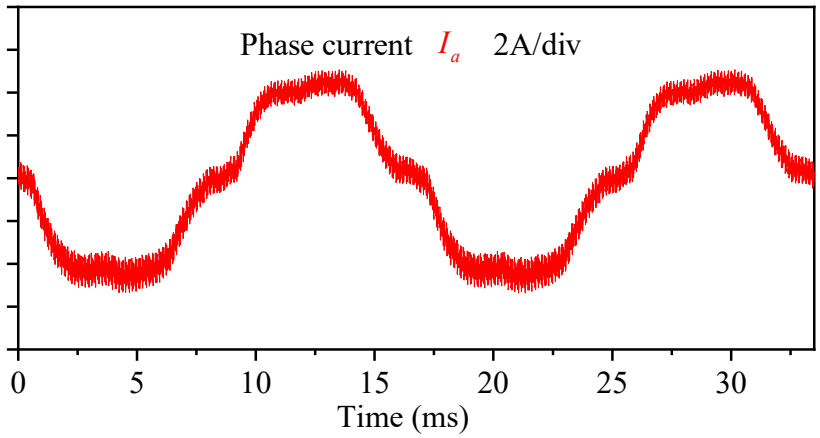


(b) Phase current spectrum.

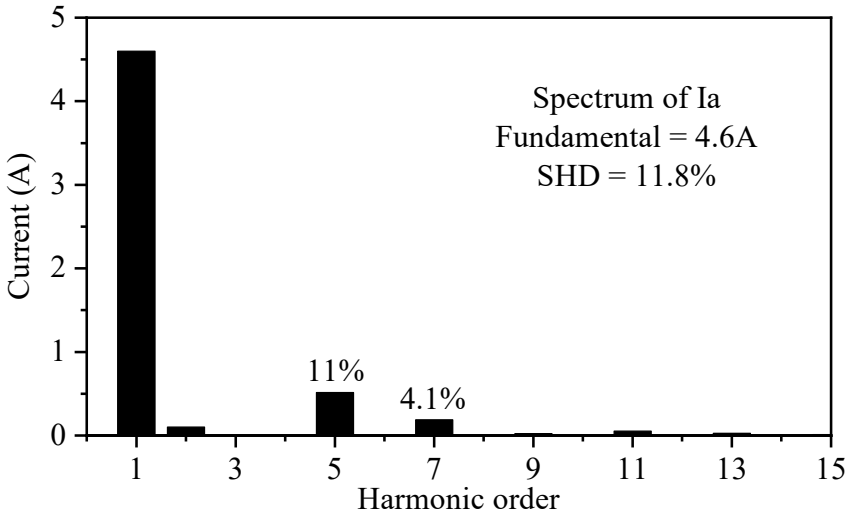
Fig. 2.16. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 66.7\pi$ rad/s ($f_e = 33.3$ Hz) at rated load with the proposed inverter nonlinearity compensation method. The dead time is set to 3μs.

It can be seen from Fig. 2.16 that the proposed compensation method can still effectively mitigate the inverter nonlinearity effect. With the proposed companion method, the SHDs are reduced from 15.4% to 2.7%, so that the harmonic distortion is decreased by 83%. It is thus confirmed that the propose compensation method still has a good performance at a different dead time. It should be noticed that although the proposed method can well compensate the

inverter nonlinearity effect and produce sinusoidal current waveform, the zero-current clamping effect still exists. This is because the voltage distortion caused by the voltage drop in anti-parallel diodes and the parasitic capacitance are compensated by a constant value in one fundamental period, which is the same way as the dead time effect and the turn-on/off delay. However, as analysed in the precious section, the current value and parasitic capacitance have a significant influence on the parasitic capacitance effect. During the current zero-crossing period, the parasitic capacitance effect is hard to be well compensate by the proposed method.

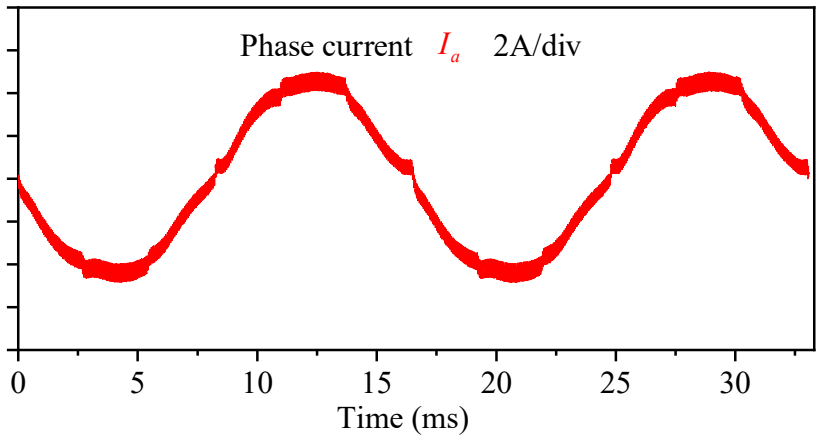


(a) Phase current waveform.

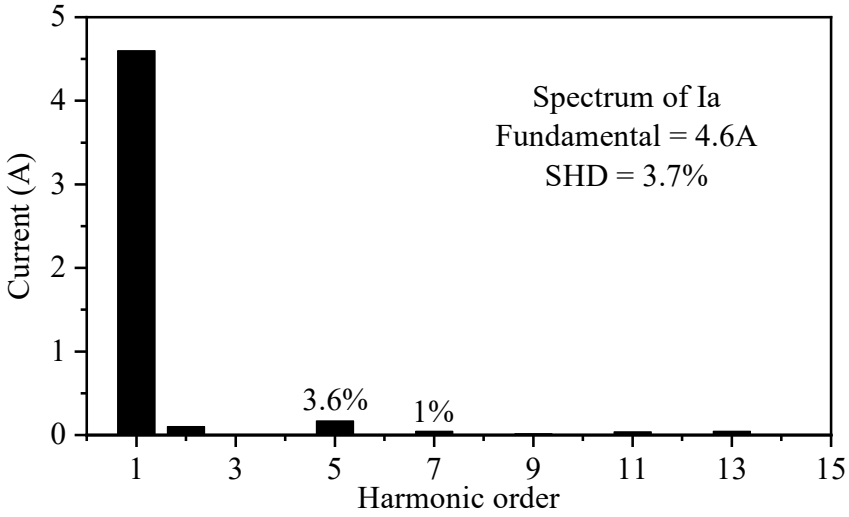


(b) Phase current spectrum.

Fig. 2.17. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 133.3\pi$ rad/s ($f_e = 66.7$ Hz) at rated load without inverter nonlinearity compensation method. The dead time is set to 1.5μs.



(a) Phase current waveform.



(b) Phase current spectrum.

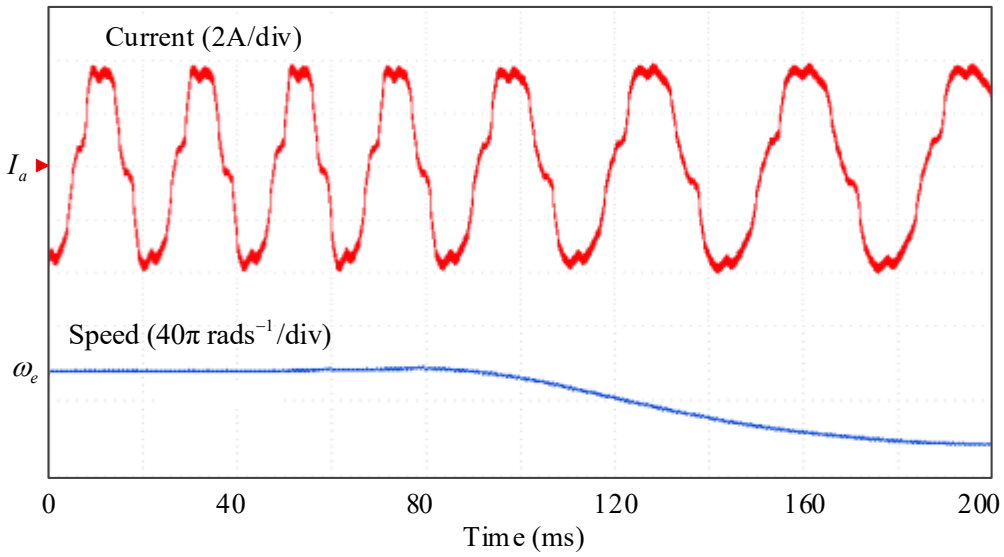
Fig. 2.18. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 133.3\,\pi$ rad/s ($f_e = 66.7$ Hz) at rated load with the proposed inverter nonlinearity compensation method. The dead time is set to 1.5μs.

When the motor speed increases to $\omega_e = 133.3\pi$ rad/s ($f_e = 66.7$ Hz), the experimental results are presented in Fig. 2.17 and Fig. 2.18. The dead time is still set as 1.5μs. As shown in Fig. 2.17 and Fig. 2.18, the proposed inverter nonlinearity compensation method is still effective with the increase of motor speed. The SHDs without and with the proposed inverter nonlinearity compensation method are 11.8% and 3.7% respectively. The proposed compensation method can decrease the harmonic distortion by 67%. It should also be noticed that with the increase of the motor speed, the current distortion becomes more severe even if

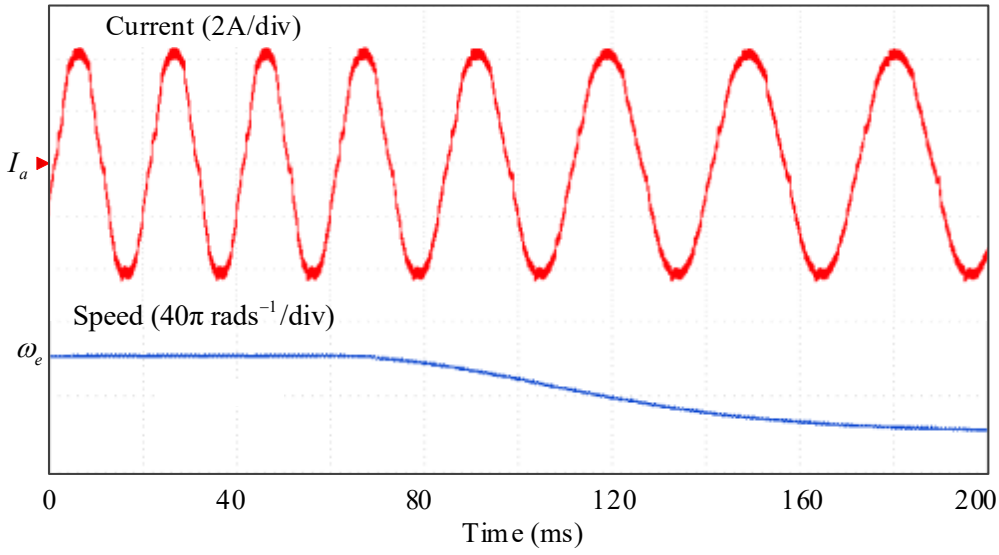
the proposed compensation method is employed. This phenomenon is caused by the other non-ideal factors such as non-sinusoidal back-EMF waveform. With the increase of motor speed, the effect of inverter nonlinearity becomes less dominant. Thus, only employing the inverter nonlinearity compensation method cannot totally suppress the current harmonics. This problem will also be further discussed and solved in the next chapter.

2.4.2 Transient State Experimental Results

Fig. 2.19 shows the phase current and speed waveforms during the transient state without and with the proposed inverter nonlinearity compensation method.



(a) Without compensation.



(b) With the proposed compensation method.

Fig. 2.19. Phase current and speed waveforms during the transient state.

The dead time is still set to 1.5μs. The speed decreases from $\omega_e = 100\,\pi$ rad/s ($f_e = 50$ Hz) to $\omega_e = 60\,\pi$ rad/s ($f_e = 30$ Hz) while the load is kept constant. As shown in the figure, the proposed method can work well for the transient state. Overall, the proposed method shows good performance under both steady and transient states.

2.5 Conclusion

In this chapter, a simple machine-parameter-independent inverter nonlinearity compensation method for BLAC control is proposed based on analysing and minimizing the current harmonics in the synchronous reference frame under steady state. The proposed method is easy to implement since it does not need complicated signal processing algorithms. The proposed method also does not rely on the machine parameters or operating conditions. The proposed method is verified by experimental results.

It should be noticed that since only the inverter nonlinearity effect is considered in this chapter, the proposed method cannot totally eliminate the current harmonics if there exist other non-ideal factors such as back-electromotive force harmonics. In the next chapter, this problem will be investigated and an adaptive current harmonics suppression method considering different non-ideal factors will be proposed.

CHAPTER 3

CURRENT HARMONICS SUPPRESSION STRATEGY FOR BRUSHLESS AC DRIVES CONSIDERING NON-SINUSOIDAL BACK-EMF

In Chapter 2, the inverter nonlinearity effect is considered for brushless alternating current (BLAC) drives. However, if there exist other non-ideal factors, only employing the inverter nonlinearity compensation method cannot totally eliminate the current harmonics. In this chapter, an adaptive linear neuron (Adaline) based current harmonics suppression method for BLAC drives considering non-sinusoidal back-electromotive force (EMF) is presented, with due account for inverter nonlinearity. The current harmonics can be well suppressed by feedforwarding self-tuning compensation voltages. The proposed method does not rely on the knowledge of back-EMF harmonic components, inverter parameters and motor parameters. Moreover, the proposed method is easy to implement since it does not need the process to extract the current harmonics. It should be noticed that although the proposed method focuses on the non-sinusoidal back-EMF, it could also compensate the current harmonics caused by other periodic non-ideal factors. The effectiveness of the proposed method is verified by both simulation and experimental results without requiring additional hardware.

The major part of this chapter is published on Transactions on Industrial Electronics, and is referred as [WAN20B] in the references.

3.1 Introduction

Permanent magnet (PM) brushless motors are widely employed for many applications such as industrial servo drives, electric vehicles and robotics etc. due to high torque density, high efficiency and high reliability. Ideally, it is desirable to have sinusoidal airgap field distribution and back-EMF waveform epically for high speed motors [LUO18]. Although the brushless direct current (BLDC) drive has the advantages of simple and robust structure, it will produce a large torque ripple. In this chapter, the BLAC drive is utilized for the test motor among medium and low speed ranges. For the ideal BLAC drive, the motor should have sinusoidal current waveforms since the current harmonics decrease the lifetime of the motor and

undermine the stability of the operation [FEN17] [LIL18]. In Chapter 2, the inverter nonlinearity effect has been compensated in order to achieve sinusoidal current waveforms. However, apart from the inverter nonlinearity effect, some other non-ideal factors can also cause low order current harmonics [HWA14]. For example, it is widely known that rotor PM configuration varies greatly with different motors which may cause non-sinusoidal back-electromotive force (EMF). Besides, the motor operation condition will also influence the PM state. For a motor with low inductance, the current harmonic problem becomes more severe. Therefore, it is of significant importance to suppress the current harmonics for improving the system performance. The conventional proportional–integral (PI) control strategy has a bandwidth limit and can only work well on DC components. Therefore, the periodic distortion cannot be eliminated through a PI controller. In recent years, various current harmonics suppression methods have been studied. These attempts could be categorized as follows.

The first group of attempts concentrates on improving the motor design via optimizing the rotor shape and better arranging the distribution of the stator windings [LIG16][DAJ14]. These attempts, while they are practical, may complicate the production process and increase the cost. In addition, back-EMF harmonics always exist in practical motors, even when some reduction techniques such as skewing is employed owing to inevitable machine design trade-offs and manufacturing tolerances [LIU06]. Besides, these attempts cannot solve the inverter nonlinearity problems.

The second group of attempts focuses on using novel control algorithms that can compensate the periodic distortion. Predictive control [ROD07][COR08][MOR09][HOL16], as a non-linear control, is used in [BAR11][SOZ13][LUO18]. The main characteristic of predictive control is the use of system model for the prediction of future behaviour of the current according to a predefined optimization criterion. Current harmonic suppression methods based on repetitive control method is proposed in [NAK08][BRA04][ESC07][ESC08][TAN17]. However, both these two control methods require high computational burden. Considering this, the multiple synchronous rotating frame transformations (MRFTs) control, which is simpler than the predictive control and the repetitive control, is used in [HUO13]. The periodic distortion can be transformed into DC components through MRFTs and low-pass-filters (LPFs) are used to separate the DC values from the transformed signals. The current harmonics are then compensated with additional PI controllers. In order to avoid the delay caused of LPFs, a closed-loop detection system which can extract the harmonics more accurately almost without

delay is proposed in [CHE16] and [LIU19B]. However, three parameters are needed for each closed-loop detection system design, which makes the design process extremely complex.

The third group of attempts concentrates on analysing the voltage distortion and eliminating the distortion by injecting opposite harmonic components. In [SPR98] and [ZHU11], the flux linkage harmonics are measured offline and then compensated via a look-up-table (LUT). Nevertheless, it should be noticed that the precise measurement of back-EMF is hard to obtain since it is usually measured on open-circuit, while the load may have significant influence on the back-EMF waveform [AZA14], and the offline compensation method does not consider the operation condition variations. In [ZHU10] and [KSH10], the back-EMF harmonics are identified online using a back-EMF estimator. Since the back-EMF estimation with higher order harmonics is difficult, the estimation of fundamental component of the back-EMF is proposed in [ABB17]. The higher order harmonics are added based on their known ratios to the fundamental component. It should also be noticed that the current harmonics cannot be completely eliminated by employing either back-EMF compensation or inverter nonlinearity compensation separately. Thus, it is important to considered various voltage distortions together. In [LIA18], an adaptive second-order sliding-mode observer is proposed. Nevertheless, the feasibility of this method heavily depends on the accuracy of motor parameters. A compensation method based on adaptive linear neuron (Adaline) is proposed in [QIU16]. Both Adaline estimators and Adaline compensators are needed to generate the compensation voltage which make the control algorithm rather complex.

In this chapter, an Adaline based current harmonics suppression method is proposed for BLAC drive with non-sinusoidal back-EMF. The current harmonics can be well suppressed by feedforwarding self-tuning compensation voltages. The proposed method does not need to estimate the current harmonics, which makes it easy to implement. The compensation voltages can be directly generated from the d- and q-axis currents. Moreover, the proposed method also require no motor or inverter parameter information. The effectiveness of the proposed current harmonics compensator is verified by simulation and test results.

3.2 Current Harmonic Analysis of BLAC Drive with Non-sinusoidal Back-EMF

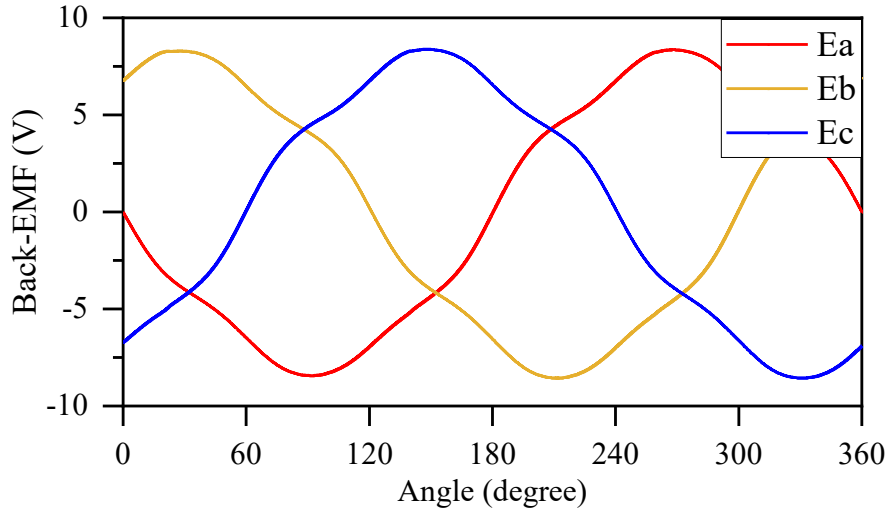
3.2.1 Non-sinusoidal Back-EMF Analysis

The voltage equations of BLAC drive can be expressed as

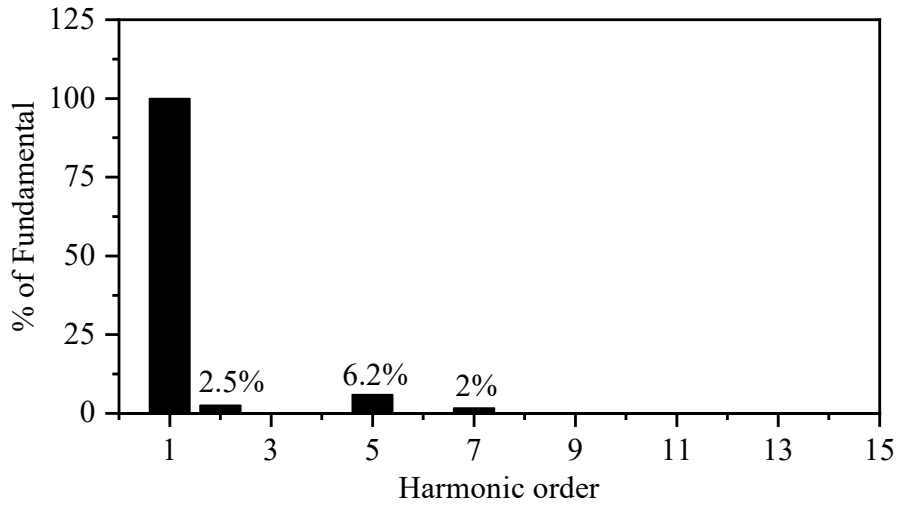
$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = R \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (3\text{-}1)$$

where R is the stator resistance, L and M are the self and mutual winding inductances. $U_{an,bn,cn}$, $i_{a,b,c}$ and $e_{a,b,c}$ are the three-phase supply voltages, phase currents and phase back-EMFs, respectively.

Under ideal condition, the three-phase back-EMFs are sinusoidal. Nevertheless, in practice, the back-EMFs are not ideal sinusoidal and may contain a series of harmonic components. The measured back-EMF waveforms and harmonic spectrum are shown in Fig. 3.1.



(a) Three phase back-EMFs.



(b) Harmonic spectrum.

Fig. 3.1. Measured back-EMF waveforms and harmonic spectrum.

The measured three phase back-EMFs of the prototype motor are shown in Fig. 3.1(a) while the harmonic spectrum is shown in Fig. 3.1(b). As can be seen, the low-frequency harmonics of the back-EMF mainly contain the 2nd, 5th and 7th order harmonics. The amplitudes of the harmonics are 2.5%, 6.2% and 2% of the fundamental component, respectively.

3.2.2 Voltage Distortion Analysis in Synchronous Reference Frame

If the back-EMF harmonic components are considered in the analysis, then the three phase back-EMFs can be expressed as

$$e_a = \sum_{n=1}^{\infty} \begin{matrix} \omega_e k_1 \cos(\omega_e t + \theta_1) \\ + \omega_e \mathrm{k}_{(3\mathrm{n}-1)} \cos[(3n-1)\,\omega_e t + \theta_{(3n-1)}] \\ + \omega_e k_{(3n+1)} \cos[(3n+1)\,\omega_e t + \theta_{(3n+1)}] \end{matrix}$$

$$e_b = \sum_{n=1}^{\infty} \begin{matrix} \omega_e k_1 \cos[(\omega_e t - \frac{2\pi}{3}) + \theta_1] \\ + \omega_e \mathrm{k}_{(3\mathrm{n}-1)} \cos[(3n-1)\,(\omega_e t - \frac{2\pi}{3}) + \theta_{(3n-1)}] \\ + \omega_e k_{(3n+1)} \cos[(3n+1)\,(\omega_e t - \frac{2\pi}{3}) + \theta_{(3n+1)}] \end{matrix} \quad (3\text{-}2)$$

$$e_c = \sum_{n=1}^{\infty} \begin{matrix} \omega_e k_1 \cos[(\omega_e t + \frac{2\pi}{3}) + \theta_1] \\ + \omega_e \mathrm{k}_{(3\mathrm{n}-1)} \cos[(3n-1)\,(\omega_e t + \frac{2\pi}{3}) + \theta_{(3n-1)}] \\ + \omega_e k_{(3n+1)} \cos[(3n+1)\,(\omega_e t + \frac{2\pi}{3}) + \theta_{(3n+1)}] \end{matrix}$$

where ω_e is the electrical angular velocity. k_1, $k_{(3\mathrm{n}-1)}$ and $k_{(3\mathrm{n}+1)}$ are the coefficients of the fundamental and harmonic back-EMF components. θ_1, $\theta_{(3\mathrm{n}-1)}$ and $\theta_{(3\mathrm{n}+1)}$ are the initial phase angles. In the conventional close-loop control system, the motor is usually controlled in a reference coordinate system rotating synchronously with the magnet flux through the coordination transformation. Then, the PI controller is used to generate the desired voltage vector. The coordination transformation function from a-b-c axis frame to d-q axis frame can be expressed as

$$C_{abc}^{dq} = \frac{2}{3}\begin{bmatrix} \cos\omega_e t & \cos(\omega_e t - \frac{2}{3}\pi) & \cos(\omega_e t + \frac{2}{3}\pi) \\ -\sin\omega_e t & -\sin(\omega_e t - \frac{2}{3}\pi) & -\sin(\omega_e t + \frac{2}{3}\pi) \end{bmatrix} \quad (3\text{-}3)$$

It is assumed that the coefficients and the initial phase angles of each EMF component of different phases are the same. After the coordination transformation, the $(3n \pm 1)^{th}$ order EMF harmonic disturbances in d-axis and q-axis can then be expressed as

$$\begin{aligned} E_{d(3n-1)} &= \omega_e k_{3n-1}\, cos(3n\omega_e t + \theta_{3n-1}) \\ E_{q(3n-1)} &= -\omega_e k_{3n-1}\, sin(3n\omega_e t + \theta_{3n-1}) \\ E_{d(3n+1)} &= \omega_e k_{3n+1}\, cos(3n\omega_e t + \theta_{3n+1}) \\ E_{q(3n+1)} &= \omega_e k_{3n+1}\, sin(3n\omega_e t + \theta_{3n+1}) \end{aligned} \tag{3-4}$$

The voltage distortions V_{d_emf} and V_{q_emf} in the synchronous reference frame caused by EMF harmonics are the sum of each EMF harmonic distortion. In this chapter, only the 2nd, 5th and 7th order harmonics are considered. Then, the voltage distortions in the d-axis and q-axis can be expressed as

$$\begin{aligned} V_{d\_emf} &= \omega_e[k_2\, cos(\,3\omega_e t + \theta_2) + k_5\, cos(\,6\omega_e t + \theta_5) + k_7\, cos(\,6\omega_e t + \theta_7)] \\ V_{q\_emf} &= \omega_e[-k_2\, sin(\,3\omega_e t + \theta_2) - k_5\, sin(\,6\omega_e t + \theta_5) + k_7\, sin(\,6\omega_e t + \theta_7)] \end{aligned} \tag{3-5}$$

The voltage distortion caused by EMF harmonics increases with the rotor speed. As shown in (3-5), the voltage distortion is the sum of the 3rd and 6th order components. For the test motor, the initial phase angles of $\theta_{1,2,5,7}$ are $\pi/2$, $-\pi/2$, $\pi/2$ and $\pi/2$ respectively.

The model is built in MATLAB/Simulink to simulate EMF harmonics in d-q axis frame. The motor is operating at $\omega_e = 400\pi$ rad/s ($f = 200$ Hz) under the rated load. The overall voltage distortion and the voltage distortion caused by each EMF harmonic in the d-axis and q-axis are presented in Fig. 3.2 and Fig. 3.3.

Apart from voltage distortion caused by EMF harmonics, it is known that the inverter nonlinearity will also induce distortion in the synchronous reference frame. In this chapter, only the dead time effect is considered to simplify the analysis. Unlike the voltage distortion caused by EMF harmonics, the amplitude of voltage distortion caused by the dead time effect is not related with the motor speed, and they are the 6th order harmonic and its multiples. Only the 6th order harmonic is further considered since the amplitude of rest harmonics are negligible compared with the 6th order one.

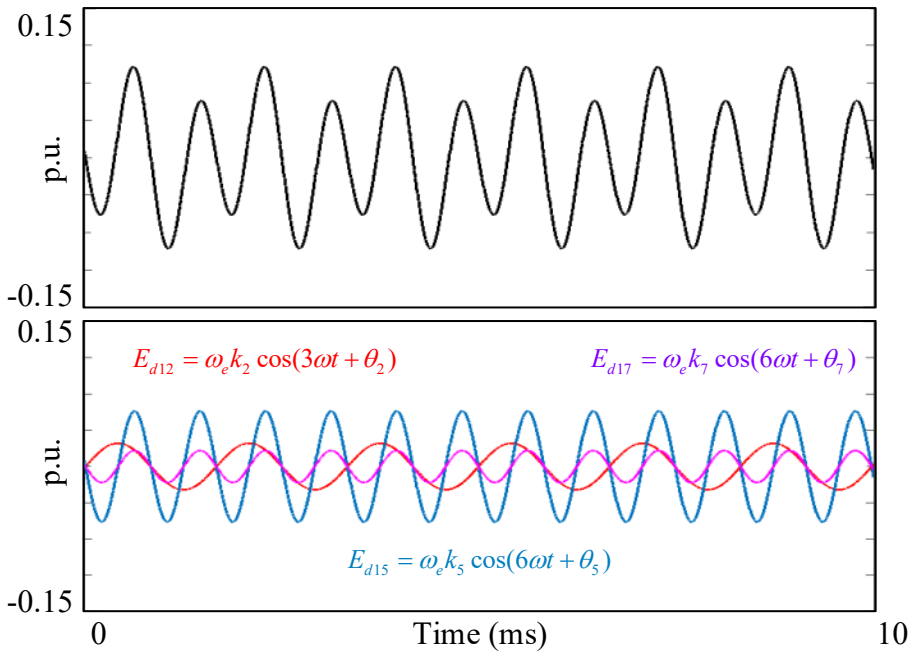


Fig. 3.2. EMF harmonic disturbances in d-axis.

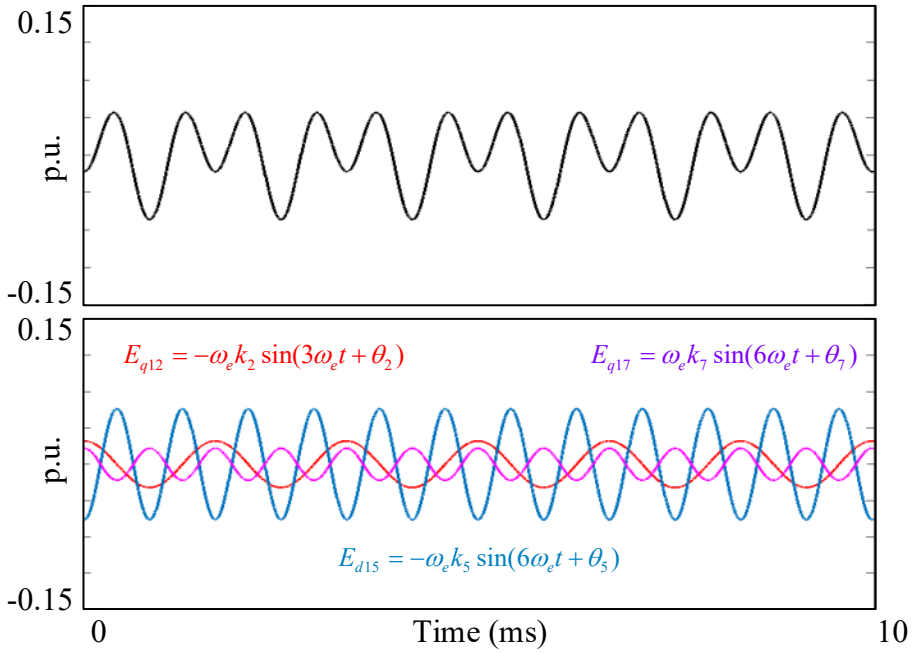


Fig. 3.3. EMF harmonic disturbances in q-axis.

Under $I_d = 0$ control, the angle between the current vector and the q-axis is zero. Then the inverter nonlinearity caused voltage distortions V_{d_dt} and V_{q_dt} can be expressed as [LIU14]

$$V_{d\_dt} = \frac{48\Delta V}{35\pi} sin(6\omega_e t)$$
$$V_{q\_dt} = \frac{8\Delta V}{35\pi} cos(6\omega_e t) \quad (3\text{-}6)$$

where ΔV is determined by inverter parameters. Since only the dead time effect is considered, ΔV can be substituted by $V_{dead} = \frac{T_{dt}}{T_{pwm}} V_{dc}$. T_{dt} is the pre-set dead time inserted in gate drive signals to prevent shoot-through in one inverter leg. T_{pwm} is the PWM switch period. V_{dc} is the supplied DC voltage. The voltage distortions V_{d_dt} and V_{q_dt} in the d-axis and q-axis are also simulated in the MATLAB/Simulink as presented in Fig. 3.4. In the simulation model, the PWM switching frequency is set to 20 kHz while the dead time is set to 1.5μs.

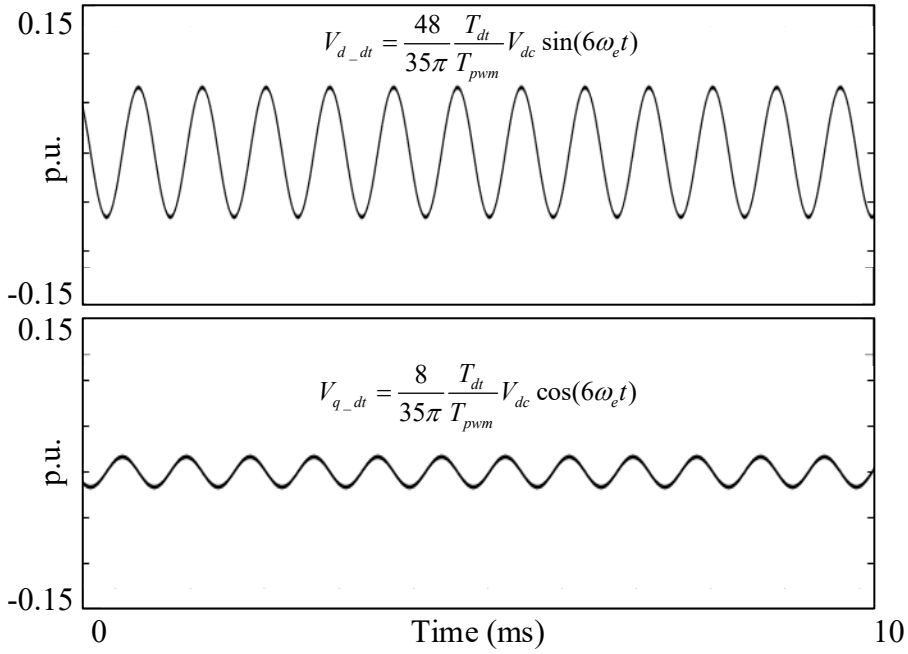


Fig. 3.4. EMF harmonic disturbances in q-axis.

The block diagram of BLAC drive system with non-sinusoidal back-EMF is shown in Fig. 3.5.

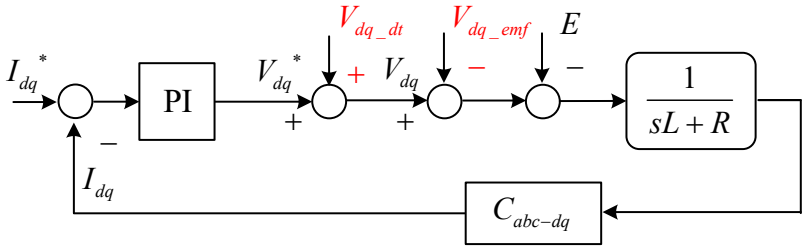


Fig. 3.5. Block diagram of BLAC drive system with non-sinusoidal back-EMF.

In Fig. 3.5, E stands for the fundamental component of the back-EMF in the synchronous reference frame.

3.2.3 Current Harmonics caused by Back-EMF Harmonics and Dead Time Effect

According to the above analyses, both EMF harmonics and dead time effect will introduce periodic disturbances. The distortion caused by EMF harmonics V_{dq_emf} increases with the motor speed while the dead time effect distortion V_{dq_dt} is related with the inverter parameters. The overall voltage distortions in the synchronous reference frame can be expressed as

$$\begin{aligned} V_{d\_har} &= -V_{d\_emf} + V_{d\_dt} \\ V_{q\_har} &= -V_{q\_emf} + V_{q\_dt} \end{aligned} \tag{3-7}$$

According to (3-1), (3-3), (3-5), (3-7) and (3-8), the current harmonics in the synchronous reference frame can be obtained as

$$\begin{aligned} I_{d_{har}} &= \frac{1}{Z_3} V_{d3_{har}} + \frac{1}{Z_6} V_{d6_{har}} \\ I_{q_{har}} &= \frac{1}{Z_3} V_{q3_{har}} + \frac{1}{Z_6} V_{q6_{har}} \end{aligned} \tag{3-8}$$

where

$$\begin{aligned} Z_3 &= \sqrt{R^2 + (3\omega_e L_s)^2} \\ Z_6 &= \sqrt{R^2 + (6\omega_e L_s)^2} \end{aligned} \tag{3-9}$$

where $L_s = L - M$. L_s is the stator inductance. Then, the current harmonics in the synchronous reference frame can be expressed as

$$\begin{aligned} &\begin{bmatrix} I_{d\_har} \\ I_{q\_har} \end{bmatrix} \\ &= \frac{-\omega}{\sqrt{R^2 + (3\omega_e L_s)^2}} \begin{bmatrix} k_2\, cos(3\omega_e t + \theta_2) \\ -k_2\, sin(3\omega_e t + \theta_2) \end{bmatrix} \\ &+ \frac{\omega}{\sqrt{R^2 + (6\omega_e L_s)^2}} \begin{bmatrix} -k_5\, cos(6\omega_e t + \theta_5) - k_7\, cos(6\omega_e t + \theta_7) + \dfrac{48V_{dead}}{35\omega\pi} sin(6\omega_e t) \\ k_5\, sin(6\omega_e t + \theta_5) - k_7\, sin(6\omega_e t + \theta_7) + \dfrac{8V_{dead}}{35\omega\pi} cos(6\omega_e t) \end{bmatrix} \end{aligned} \tag{3-10}$$

Substituting the initial phase angles $\theta_{2,5,7}$ into (3-11), then the current harmonics in the synchronous reference frame can be expressed as

$$\begin{bmatrix} I_{d\_har} \\ I_{q\_har} \end{bmatrix} = \frac{-\omega}{\sqrt{R^2 + (3\omega_e L)^2}} \begin{bmatrix} k_2 \sin(3\omega_e t) \\ k_2 \cos(3\omega_e t) \end{bmatrix} + \frac{\omega}{\sqrt{R^2 + (6\omega_e L)^2}} \begin{bmatrix} (k_5 + k_7 + \frac{48V_{dead}}{35\omega\pi}) \sin(6\omega_e t) \\ (k_5 - k_7 + \frac{8V_{dead}}{35\omega\pi}) \cos(6\omega_e t) \end{bmatrix} \tag{3-11}$$

The coordination transformation function from d-q axis frame to a-b-c axis frame can be expressed as

$$C_{abc}^{dq} = \begin{bmatrix} \cos\omega_e t & -\sin\omega_e t \\ \cos(\omega_e t - \frac{2}{3}\pi) & -\sin(\omega_e t - \frac{2}{3}\pi) \end{bmatrix} \tag{3-12}$$

Taking phase A current for example, after the coordination transformation, the overall current harmonic of phase A I_{a_har} can be expressed as

$$I_{a\_har} = \frac{-\omega_e k_2}{\sqrt{R^2 + (3\omega_e L)^2}} \sin(2\omega_e t) + \frac{\omega_e k_5 + \frac{4T_{dead}V_{dc}}{5\pi T_{pwm}}}{\sqrt{R^2 + (6\omega_e L)^2}} \sin(5\omega_e t) + \frac{\omega_e k_7 + \frac{4T_{dead}V_{dc}}{7\pi T_{pwm}}}{\sqrt{R^2 + (6\omega_e L)^2}} \sin(7\omega_e t) \tag{3-13}$$

The rest two phase currents can be obtained accordingly. It is shown that the current harmonics are determined by the motor speed, the motor parameters and the inverter parameters. In this chapter, the selective harmonic distortion (SHD) of phase current is used to analyse the current harmonics, which is defined as

$$SHD = \frac{\sqrt{I_2^2 + I_5^2 + I_7^2}}{I_1} \tag{3-14}$$

3.3 Proposed Current Harmonics Suppression Method

The proposed current harmonics suppression method is based on suppressing the voltage distortion in the synchronous reference frame. According to (3-7), the voltage distortion contains the 3rd and 6th order harmonics induced by both the EMF harmonics and the dead time

effect. If the two distortion causing factors are considered as a whole, then as long as the voltage distortion can be eliminated by adding a proper feedforward compensation voltage V_{ff_dq} in the synchronous reference frame, the current harmonics can be well compensated. The block diagram of a BLAC drive system with feedforward compensation is shown in Fig. 3.6.

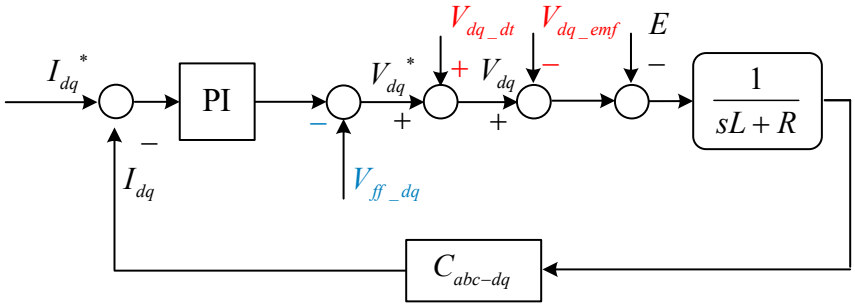


Fig. 3.6. Block diagram of a PMSM drive system with feedforward compensation.

The feedforward compensation voltages can be expressed as

$$\begin{aligned} V_{ff\_d} &= k_{c3d}\, cos(3\omega_e t + \theta_{c3d}) + k_{c6d}\, cos(6\omega_e t + \theta_{c6d}) \\ V_{ff\_q} &= k_{c3q}\, cos(3\omega_e t + \theta_{c3q}) + k_{c6d}\, cos(6\omega_e t + \theta_{c6q}) \end{aligned} \tag{3-15}$$

where k_{ci} and θ_{ci} are the amplitude and the phase of compensation voltage, respectively. An Adaline compensation voltage generation method is employed in this chapter. The structure of the Adaline is shown in Fig. 3.7.

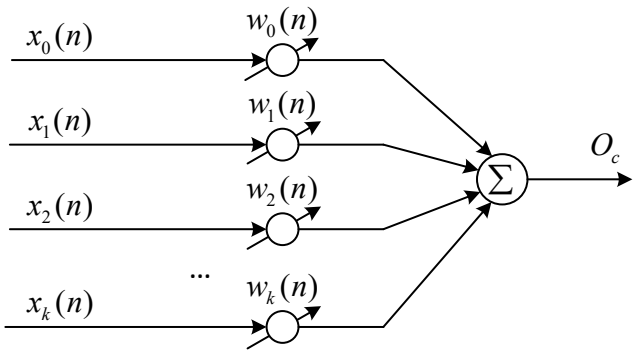


Fig. 3.7. Structure of Adaline.

The mathematical model of the Adaline can be expressed as [LIU11]

$$O_c^n = \sum_{i=0}^{k} x_i(n)\, w_i(n) \tag{3-16}$$

where x_i is the input vector and w_i is the weight factor of the corresponding vector. O_c is the output. In order to generate the compensation voltage which contains both the 3rd and 6th components, four input vectors are needed, and they are expressed as

$$\begin{aligned} x_{31} &= cos(3\omega_e t) \qquad x_{32} = sin(3\omega_e t) \\ x_{61} &= cos(6\omega_e t) \qquad x_{62} = sin(6\omega_e t) \end{aligned} \tag{3-17}$$

Then the corresponding weight factors are defined as w_{31}, w_{32}, w_{61} and w_{62}. The compensation voltage generated at the nth sample point can be written in vector format as

$$x^n (w^n)^T = {V_{ff\_dq}}^n \tag{3-18}$$

where the nth sample point of input vector x^n and weight factor w^n can be expressed as

$$\begin{aligned} x^n &= [cos(3\omega_e t^n) \quad sin(3\omega_e t^n) \quad cos(6\omega_e t^n) \quad sin(6\omega_e t^n)] \\ w^n &= [{w_{31}}^n \qquad {w_{32}}^n \qquad {w_{61}}^n \qquad {w_{62}}^n] \end{aligned} \tag{3-19}$$

The goal is to find the proper weight factor w^n so that $V_{ff\_dq}^n = V_{dq\_har}$. Let the error between $V_{ff\_dq}^n$ and V_{dq_har} at the nth sample point be defined as

$$e^n = V_{dq\_har} - x^n (w^n)^T \tag{3-20}$$

the least-mean-square (LMS) algorithm is then used for adaptive learning of weight factor. Two compensators for V_{d_har} and V_{q_har} are designed separately. The goal of the adaptive learning is to make the predefined error criterion achieve the minimum value so that each vector of the linear neuron network is approaching the learning object. A commonly used objective function J^n is the half of the squared-error criterion function [LIU11] that can be expressed as

$$J^n = \frac{1}{2}(e^n)^2 = \frac{1}{2}(V_{dq\_har} - x^n (w^n)^T)^2 \tag{3-21}$$

Here, the fundamental frequency is obtained based on the motor speed. The weight factor, which minimizes the criterion function J^n can be found by applying the gradient descent procedure. The gradient of J^n with respect to w^n, denoted by $\nabla J^n(w^n)$ can be expressed as

$$\nabla J^n(w^n) = -(V_{dq\_har} - x^n (w^n)^T) x^n = -e^n x^n \tag{3-22}$$

It is known that if the weight factors are updated in the reverse direction of the gradient, the cost function will then decrease. Thus, the weight factor updating rule is then given as

$$w^n = w^{n-1} + \eta_v e^n x^n \tag{3-23}$$

The property that the weight factors change much more slowly than the variable in the system is intrinsic to the adaptive algorithm. In practical terms, it means the adaptive gain η_v should be selected small [LIU11]. One of the results of the slow adaption is attenuation of high frequency components from inputs. The error e^n between $V_{ff\_dq}^n$ and V_{dq_har} can also be substituted by harmonic current I_{dqh} as

$$e^n = V_{dq\_har} - V_{ff\_har}^n = -Z_n I_{dqh} \tag{3-24}$$

where Z_n can be calculated based on (3-10). Since the goal of the adaptive learning is to let J^n achieve the minimum value, the DC component of the current, which remains unchanged regardless of the distortion, will not affect the calculating direction of the gradient between two steps. The motor resistance and inductance can be regarded as constant values which do not affect estimation process. Then, the error e^n between $V_{ff\_dq}^n$ and V_{dq_har} which is used to calculate the weight factors can further be substituted by I_{dq}. The weight factor updating rule can be expressed as

$$w^n = w^{n-1} - \eta_i {I_{dq}}^n x^n \tag{3-25}$$

Since the weight factors are adaptively tuned, the procedure does not rely on the knowledge of any motor parameters and is insensitive to the parameter variation. The compensation voltage generator is shown in Fig. 3.8.

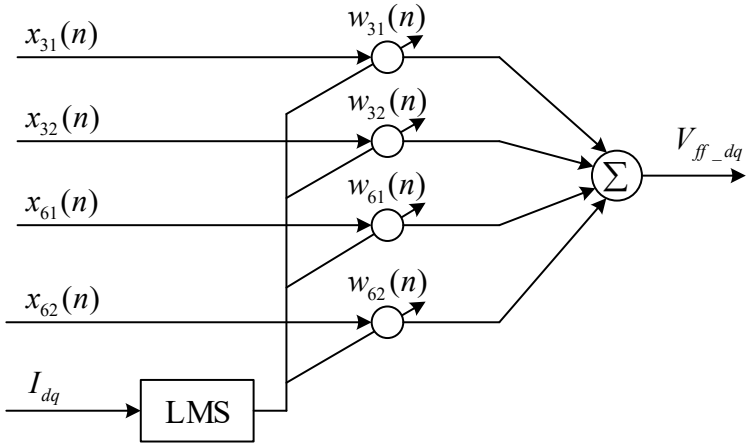


Fig. 3.8. Adaline based compensation voltage generator.

In the proposed method, the data that are used for the network training are the currents I_{dq} in the synchronous reference frame. The adaptive gain η_i is selected as $1\,e^{-6}$ in the both

simulation and experiment. It should be noticed that the proposed method needs to generate the 3rd and 6th order components, and thus, under practical condition, the sample accuracy and sample frequency might limit its application in high speed range. Nevertheless, since the BLAC drive is only employed to the test motor under low and medium speed ranges, the aforementioned problem will have a minor negative effect on the implementation as presented in this chapter. The control block diagram with the proposed Adaline based current harmonics compensation strategy is shown in Fig. 3.9.

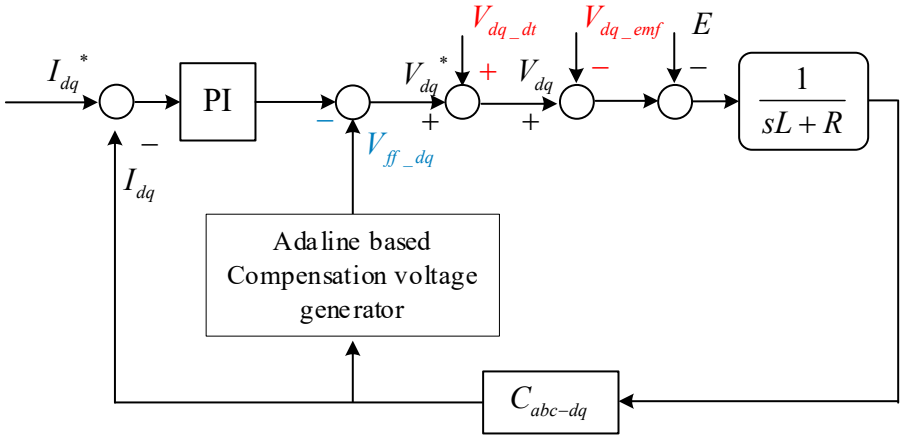


Fig. 3.9. Block diagram of BLAC drive system with the proposed method.

In the proposed method, the d-axis and q-axis currents are used as the criterions directly while four input vectors and four corresponding weight factors are used to generate the compensation voltage as presented in (3-17) and (3-19). The LMS algorithm is then used for adaptive training of weight factors so that the d-axis and q-axis currents can be reduced to the minimum value. The weight factor updating rule can be expressed as shown in (3-25) without any other current pre-processing. Thus, the delay caused by LPFs in the conventional methods can be eliminated. This also means that computation burden is relieved. Besides, since the proposed current harmonic suppression method regards different distortions as the same kind of disturbance, it is feasible without the knowledge of the relationship between the two distortion factors.

3.4 Simulation and Experimental Results

3.4.1 Simulation Results

The simulation model is built in MATLAB/Simulink to verify the effectiveness of the proposed method. A control model considering EMF harmonics and dead time effect is built. The characteristic parameters of the motor are given in Appendix I.

The phase A current waveform I_a and the d-q axis currents I_d and I_q without any current harmonics suppression method are shown in Fig. 3.10. The corresponding current spectrum of I_a is presented in Fig. 3.11. The motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) under rated load (0.24 Nm).

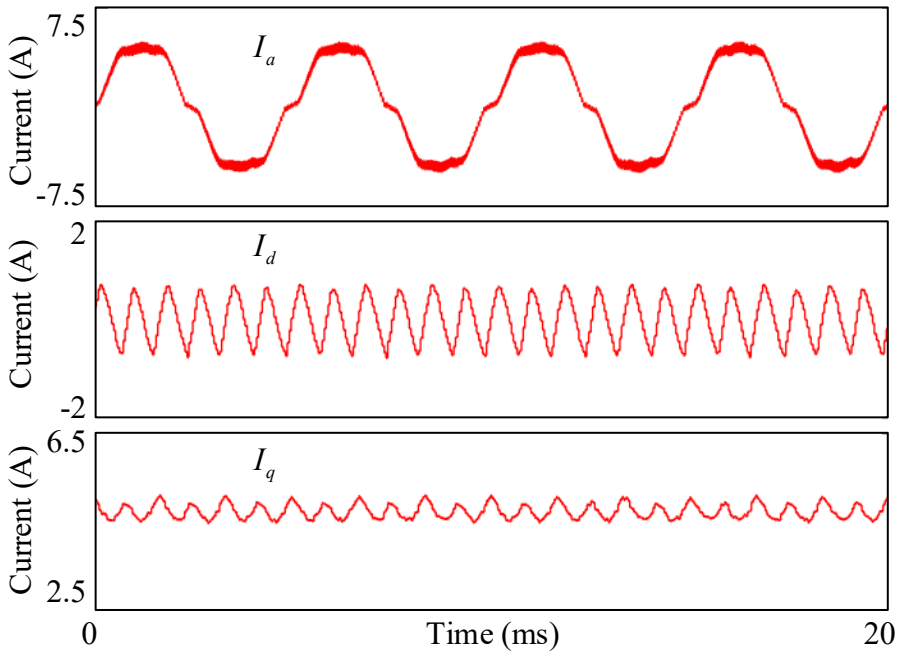


Fig. 3.10. Simulation current waveforms when the motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load, without current harmonics suppression.

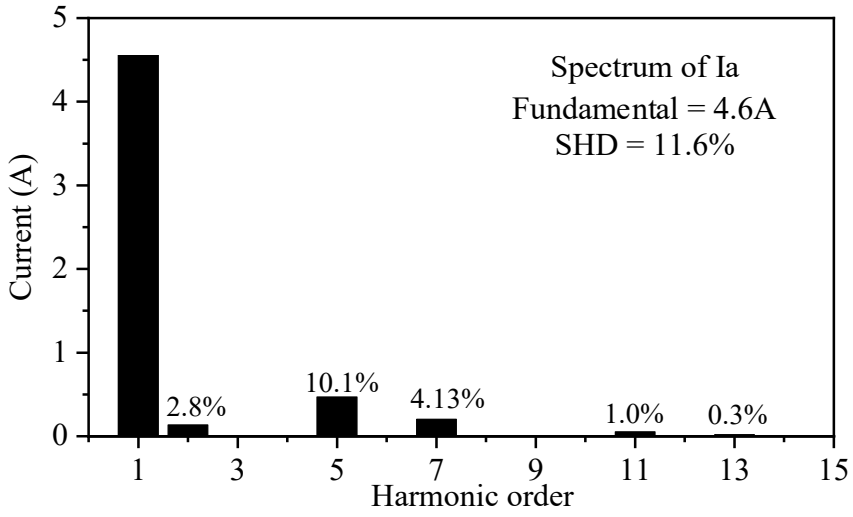


Fig. 3.11. Simulation phase current spectrum when the motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load, without current harmonics suppression.

As shown in the simulation results, due to the EMF harmonic components and the dead time effect, the current waveform is heavily distorted. There exists periodic distortion in the synchronous reference frame. The harmonic spectrum shows that the harmonics are the 2nd, 5th and 7th order in a-b-c axis frame which is the same as the analyses. The SHD of phase current without harmonics suppression is 11.6%.

In order to verify the influence of motor inductance on current harmonics, several simulation tests are undertaken when the motor inductance increases from 0.66mH to 5mH, with all the other parameters unchanged. When the motor inductance is 5mH, the phase A current waveform I_a and the d-q axis currents I_d and I_q without any current harmonics suppression method are shown in Fig. 3.12.

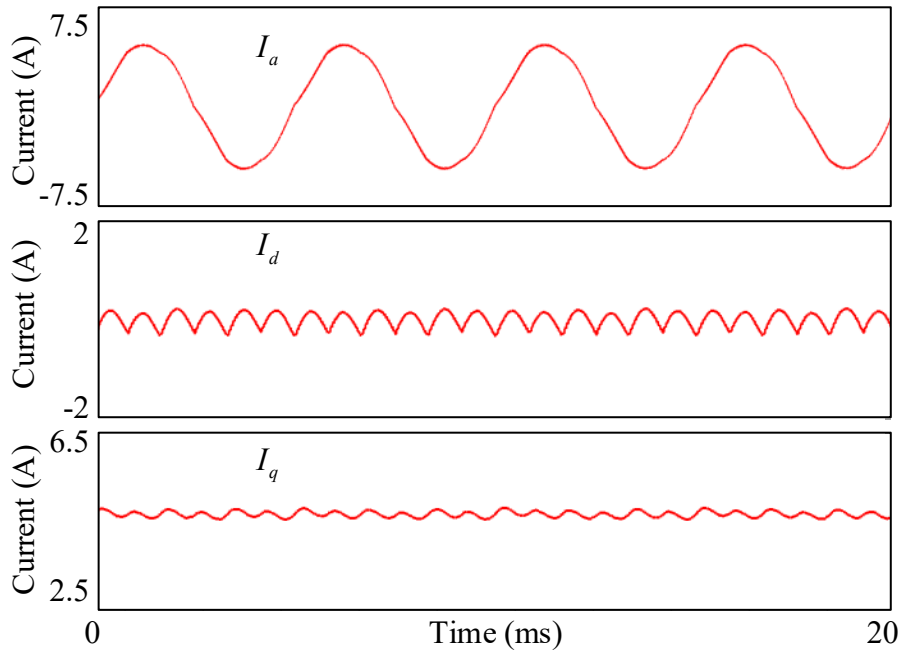


Fig. 3.12. Simulation current waveforms for a motor that has 5 mH of phase inductance. The motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load, without current harmonics suppression.

The corresponding current spectrum of I_a is shown in Fig. 3.13. As shown in Fig. 3.13, when the motor inductance increases, the current SHD will reduce which is the same as the theoretical analyses. When the motor inductance is large, the EMF harmonics and the dead time effect will still cause current distortion. Nevertheless, the current distortion is not obvious. For a motor with low inductances, the low order current harmonics induced by non-sinusoidal back-EMF

and inverter nonlinearity will become more severe. Thus, it is of more importance for the low inductance motor to compensate the current harmonics.

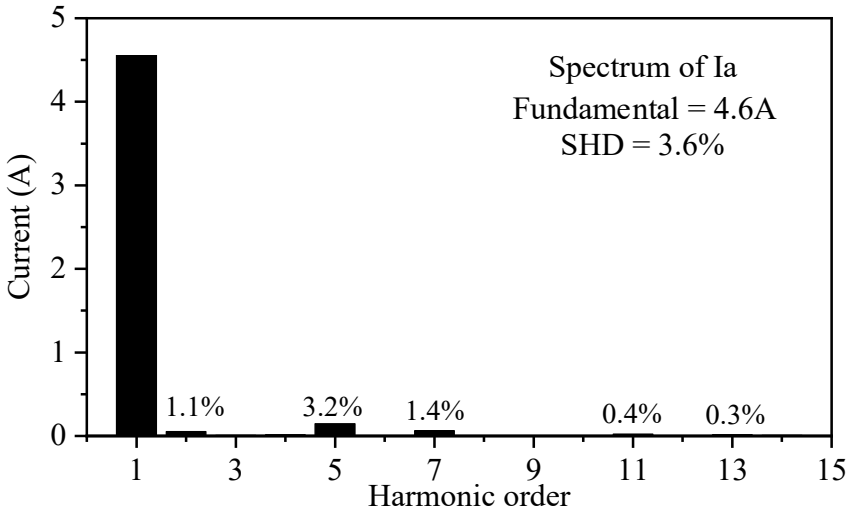


Fig. 3.13. Simulation phase current spectrum for a motor that has 5 mH of phase inductance. The motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load, without current harmonics suppression.

The simulation results of phase current and the corresponding current spectrum by employing the proposed current harmonics suppression method are given in Fig. 3.14 and Fig. 3.15. As shown in Fig. 3.14, the current distortion is well suppressed with the proposed method. As can be seen in Fig. 3.15, the low order current harmonics are well compensated while the current SHD is reduced to 0.4% from 11.6%.

It should be noticed there still exist the 11^{th} and 13^{th} order harmonics in the a-b-c reference frame after the compensation. These harmonics are caused by inverter nonlinearity. They are not suppressed because only the 6^{th} order harmonic is considered in the proposed method. In theory, these harmonics can be suppressed by expanding the Adaline structure into six inputs vectors and six self-tuning weight factors, which are shown in Fig. 3.16.

The current spectrum after expanding the Adaline structure is shown in Fig. 3.17. As can be seen, the 11^{th} and 13^{th} order harmonics are well reduced. However, it should be noticed that although the current harmonics can be further reduced, expanding the Adaline structure will increase the computation burden. Since these high order harmonics have small influence on the current waveforms, the further improvement of the proposed method is not necessary in reality.

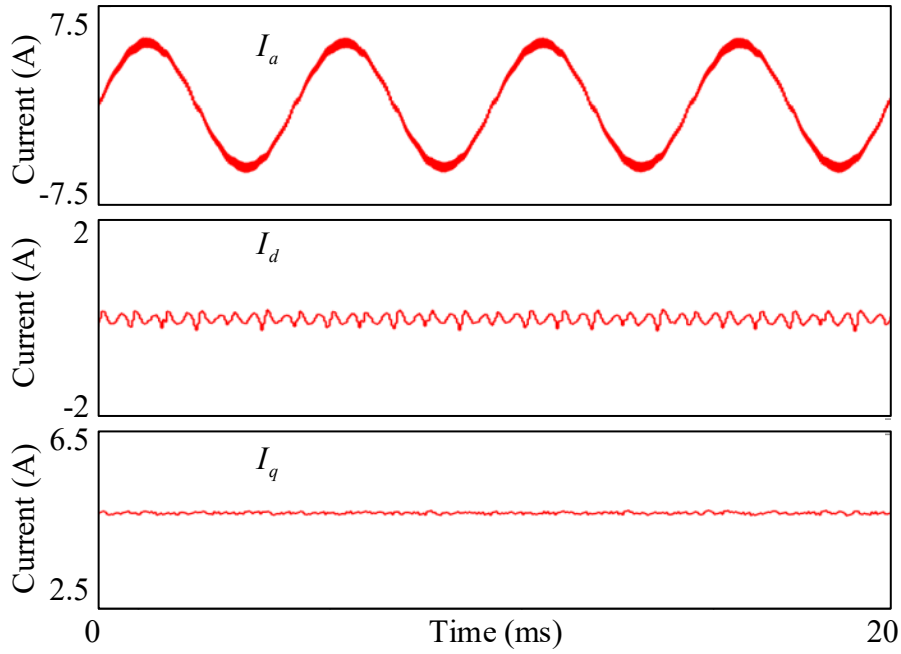


Fig. 3.14. Simulation current waveforms when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e =$ 200 Hz) at rated load, using the proposed current harmonics suppression method.

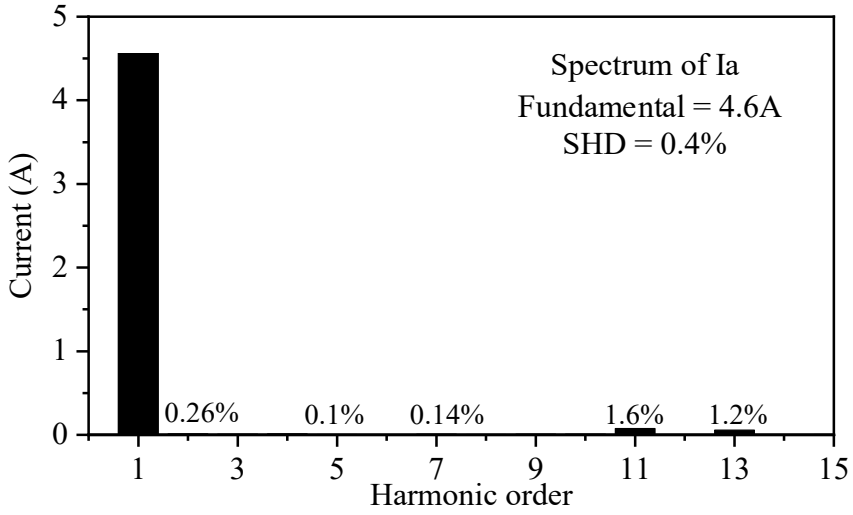


Fig. 3.15. Simulation phase A current spectrum when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load, using the proposed current harmonics suppression method.

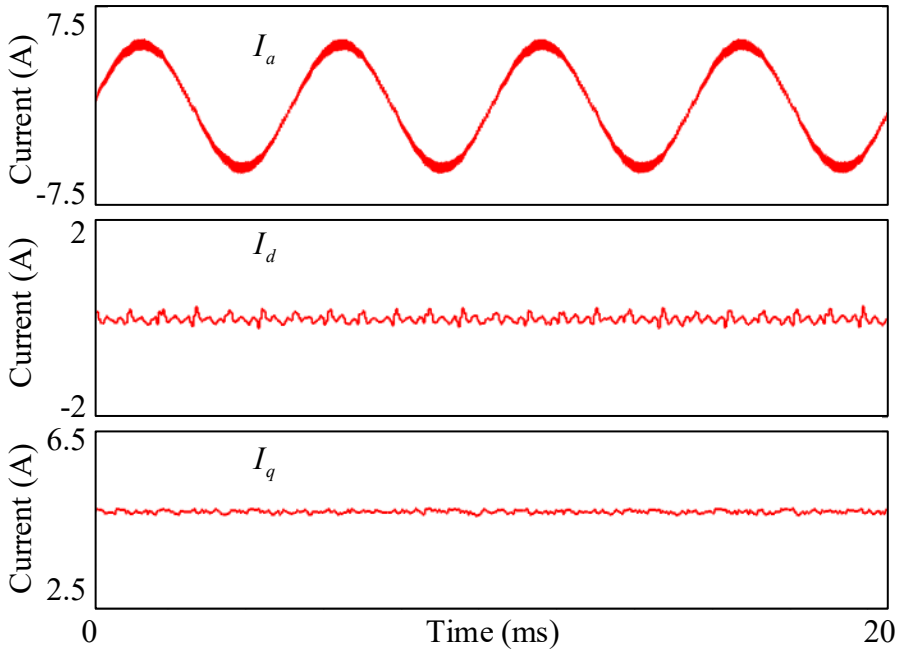


Fig. 3.16. Simulation current waveforms when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e =$ 200 Hz) at rated load. The Adaline structure is expanded to six inputs and six weight factors.

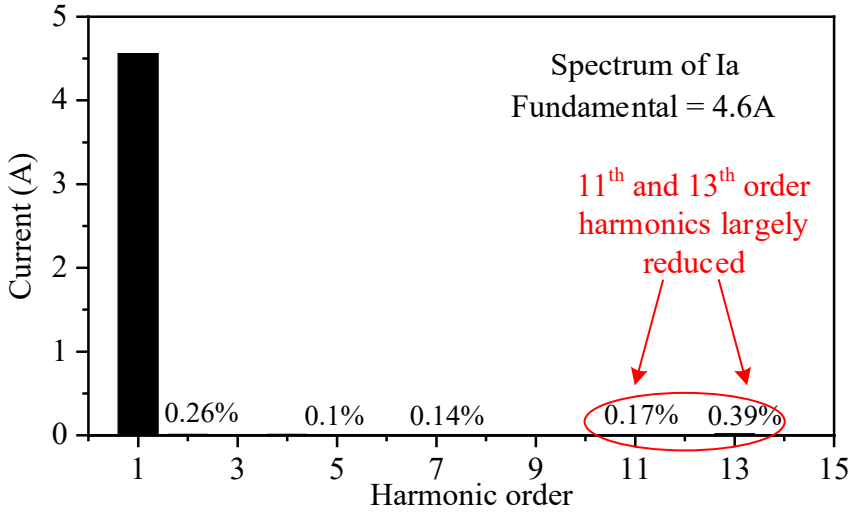
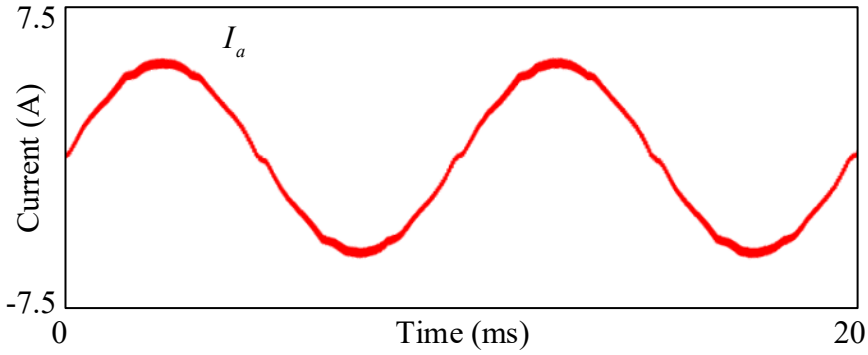
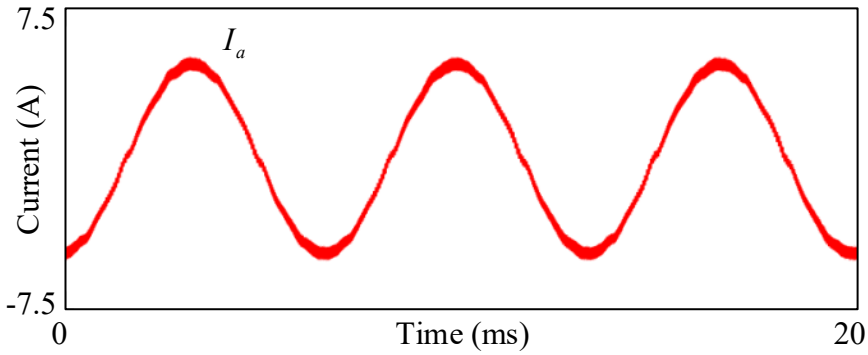


Fig. 3.17. Simulation current spectrum when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e =$ 200 Hz) at rated load. The Adaline structure is expanded to six inputs and six weight factors.

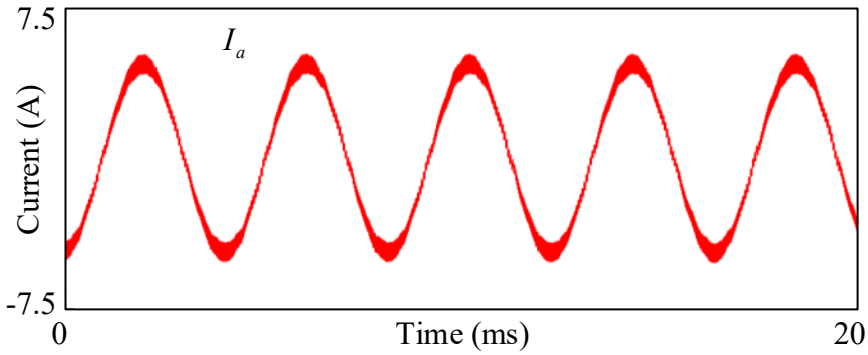
When the motor is operating at the rated load, the phase current at different speed conditions are shown in Fig. 3.18. As shown, the proposed method can successfully suppress the current harmonics and produce a sinusoidal current waveform under different speed conditions.



(a) Current waveform when $\omega_e = 200\pi$ rad/s ($f_e = 100$ Hz)



(b) Current waveform when $\omega_e = 300\pi$ rad/s ($f_e = 150$ Hz)



(c) Current waveform when $\omega_e = 500\pi$ rad/s ($f_e = 250$ Hz)

Fig. 3.18. Simulation current waveform under different speed at rated load with and without the proposed current harmonics suppression method.

The simulation results of current SHD with and without the proposed method under different motor inductance are given in Fig. 3.19. The simulations are taken under rated load while the Adaline structure has four inputs and four weight factors. As shown in Fig. 3.19, The current distortion cannot be neglected when the motor inductance is small. By employing the proposed

method, the current distortion is well suppressed regardless of the value of the motor inductance. Overall, The simulation results have verified the effectiveness of the proposed method.

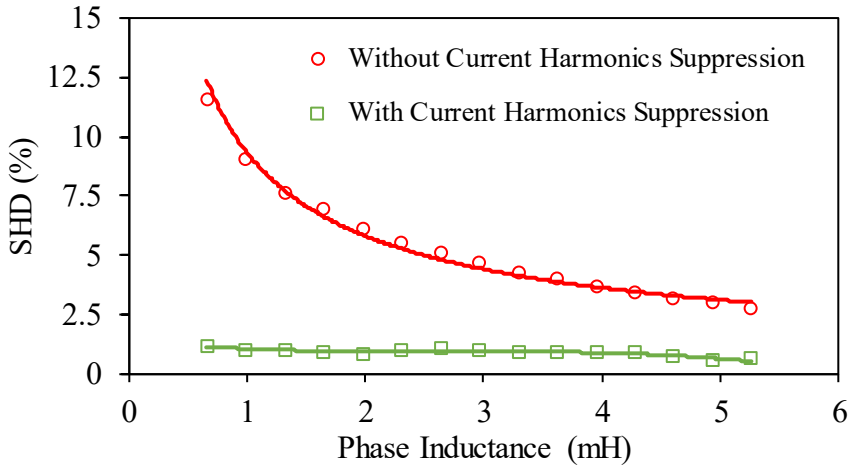


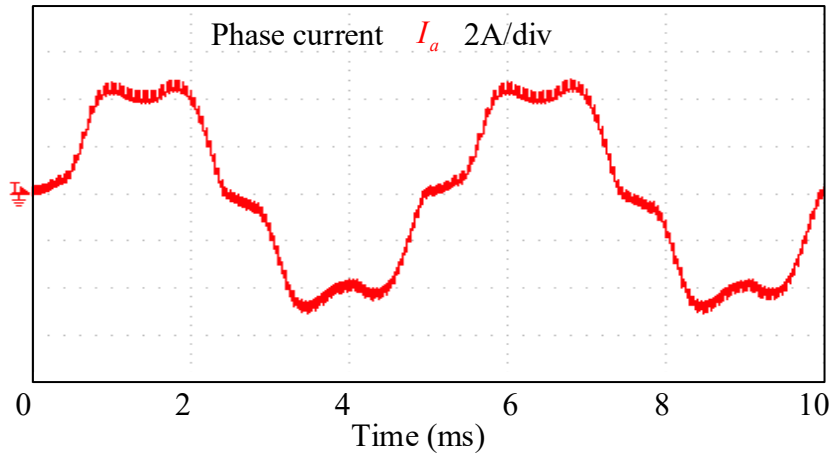
Fig. 3.19. Relationship between motor inductance and current distortion.

3.4.2 Steady State Experimental Results

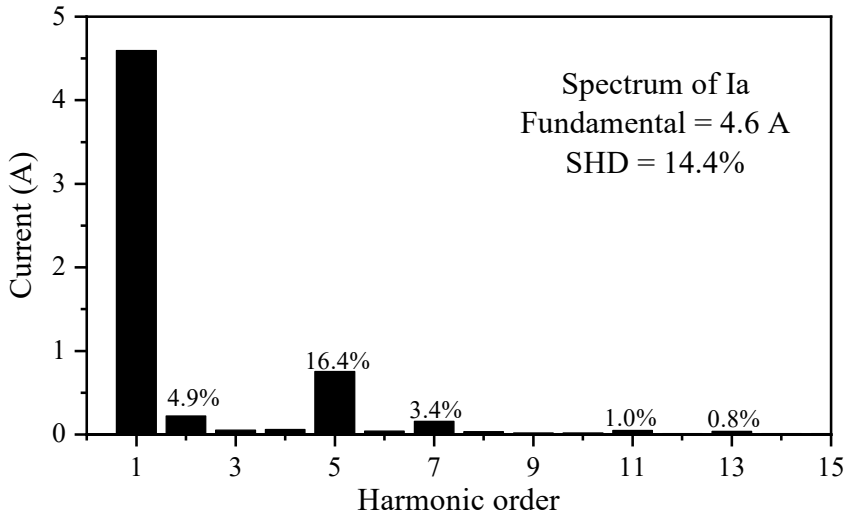
The test rig setup is presented in the Appendix. The measured phase current waveform and its spectrum without current harmonics suppression method under rated torque are shown in Fig. 3.20. The motor is still operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz), same as the typical simulation condition. The phase current waveform and spectrum are shown accordingly. The test results with different current harmonics suppression methods are given in Fig. 3.21- Fig. 3.23. The results with only dead time compensation are given in Fig. 3.21. Based on the offline measurement of back-EMF components, the results of harmonic suppression method with a LUT are given in Fig. 3.22. These two compensation methods are used as benchmark to compare with the proposed method. The results of the proposed method are given in Fig. 3.23. In each compensation method, the phase current waveform and spectrum are presented accordingly.

3.4.2.1 Test Results without Current Harmonics Suppression Method

In Fig. 3.20, the amplitudes of the 2nd, 5th and 7th order harmonics I_2, I_5 and I_7 are 4.9%, 16.4% and 3.4% of the fundamental current component I_1, respectively. As can be seen, the current waveform is heavily distorted. Without any harmonic suppression method, the SHD of the phase current is 14.4%. The back-EMF harmonics and the dead time effect induce voltage distortion. Since the motor inductance is relatively small, the distortion cannot be suppressed by the motor inductor and will cause large current harmonics.



(a) Phase current waveform.



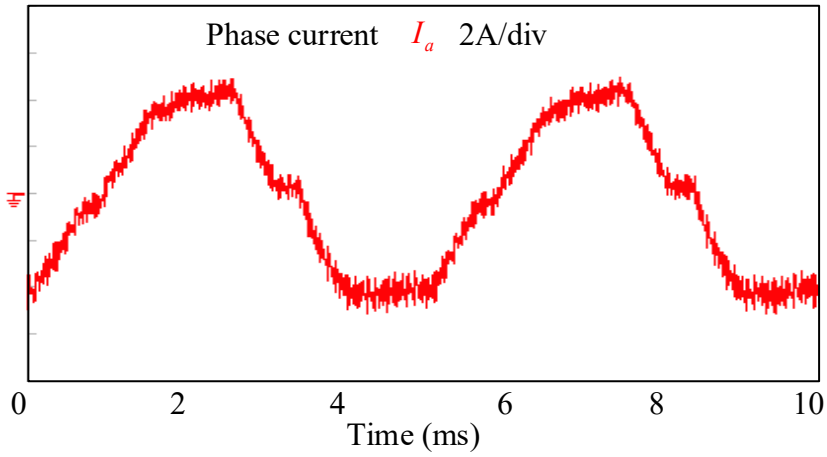
(b) Phase current spectrum.

Fig. 3.20. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load without compensation.

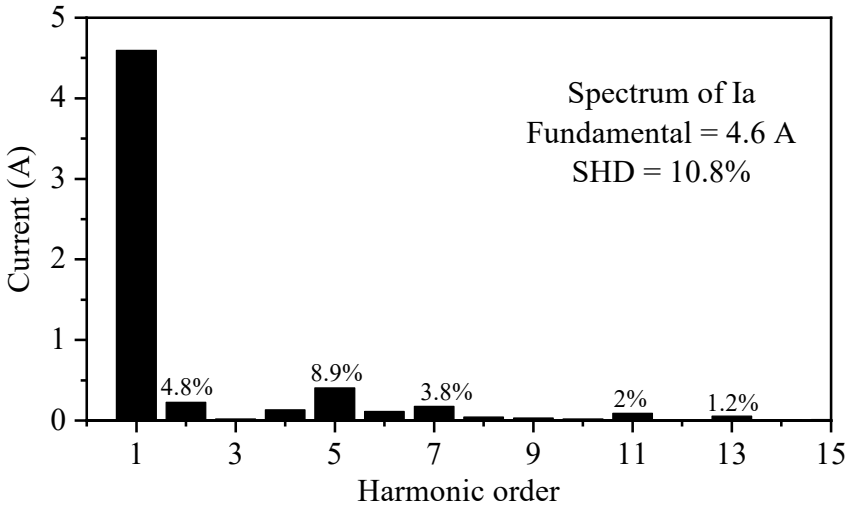
3.4.2.2 Test Results with Only Dead Time Compensation

If the back-EMF harmonics are not considered, the dead time effect is compensated based on the method proposed in [LIA18]. The current distortion is reduced as shown in Fig. 3.21. The amplitudes of 2nd, 5th and 7th order harmonics are 4.8%, 8.9% and 3.8% of the fundamental current component, respectively. It is known that the dead time compensation method has no effect on harmonics other than the 6th order and its multiples in the synchronous reference frame. Thus, the 5th order harmonic of phase current is largely reduced thanks to the dead time compensation while the 2nd order harmonic is not suppressed and remains almost the same

before and after the compensation. The phase current SHD reduces to 10.8%. Nevertheless, only the dead time effect is considered while other inverter nonlinearity effect is not compensated. Thus, the compensation voltages are not precise enough which makes the phase current still not sinusoidal and contain large amounts of harmonics. Thus, the EMF harmonics should also be considered and compensated.



(c) Phase current waveform.

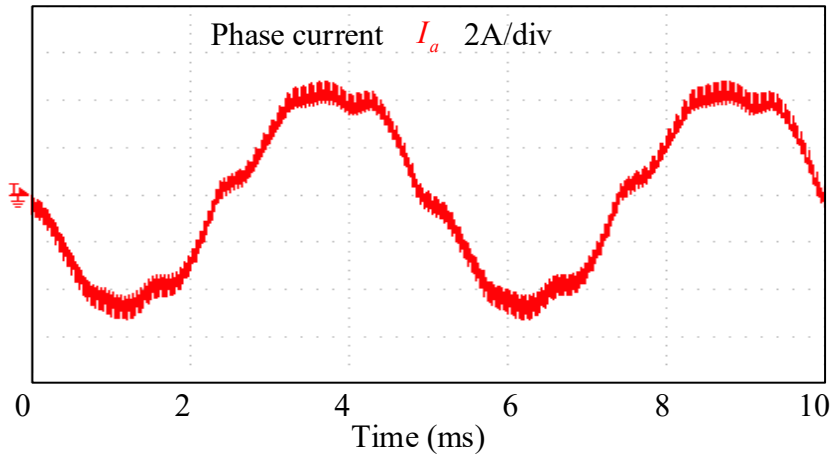


(d) Phase current spectrum.

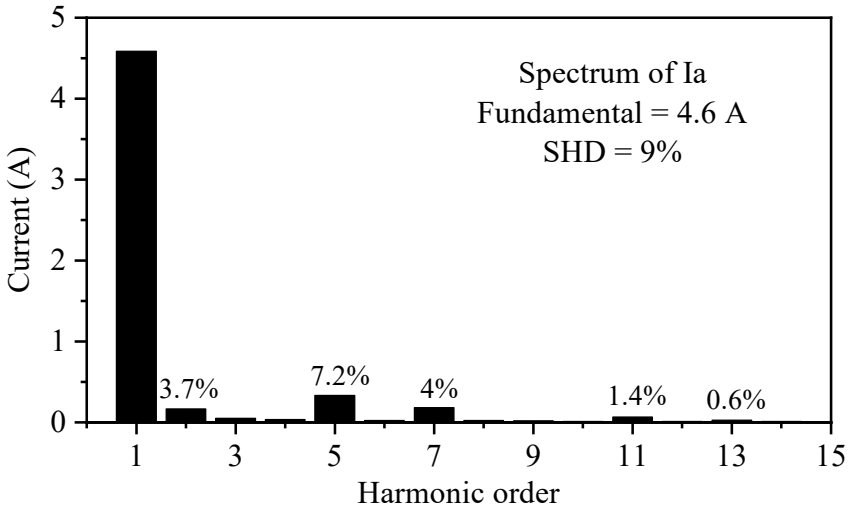
Fig. 3.21. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load with traditional dead time compensation method.

3.4.2.3 Test Results of Offline Current Harmonics Suppression Method based on LUT

Together with the dead time compensation, the current harmonics caused by the EMF harmonics are offline compensated based on pre-measured back-EMF LUT. The experimental results are shown in Fig. 3.22.



(a) Phase current waveform.



(a) Phase current spectrum.

Fig. 3.22. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load with offline current harmonics suppression method based on LUT.

By extracting the DC components of V_d and V_q, the compensation voltages for EMF harmonics are generated through multiplying V_{d_dc} and V_{q_dc} by the ratios of EMF harmonics to fundamental component. As shown in the figure, when the back-EMF harmonics are

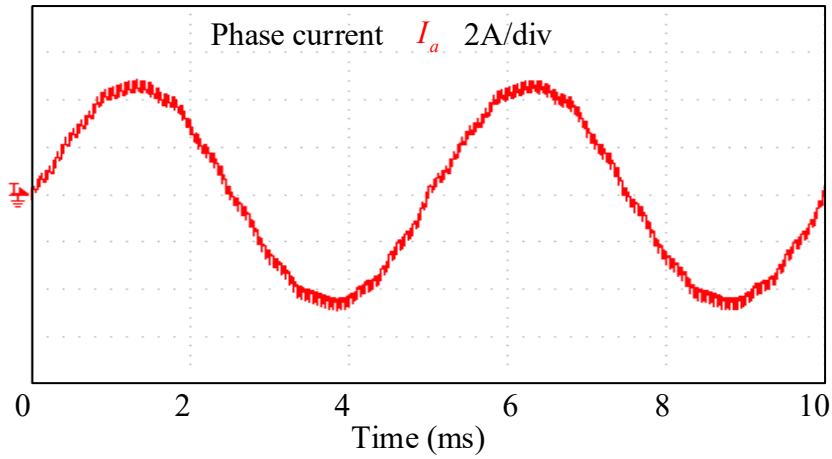
considered, the amplitudes of all three harmonics are suppressed. The 2nd, 5th and 7th order harmonics after the compensation are reduced to 3.1%, 7.2% and 4% of the fundamental current component, respectively.

Since the offline compensation method considers all three low order harmonics, the 2nd order and 5th order harmonics are reduced by 37% and 56%, respectively, compared with non-compensation condition. The 7th order harmonic remains almost unchanged before and after the offline compensation. With the offline LUT based compensation method, the SHD reduces to 9%. Nevertheless, since the information from LUT is not always precise and it does not consider the effect of operation condition variations on back-EMF, the compensation voltages are also not precise by this method. Thus, the offline compensation cannot provide ideal current. A more accurate current harmonics suppression method is needed.

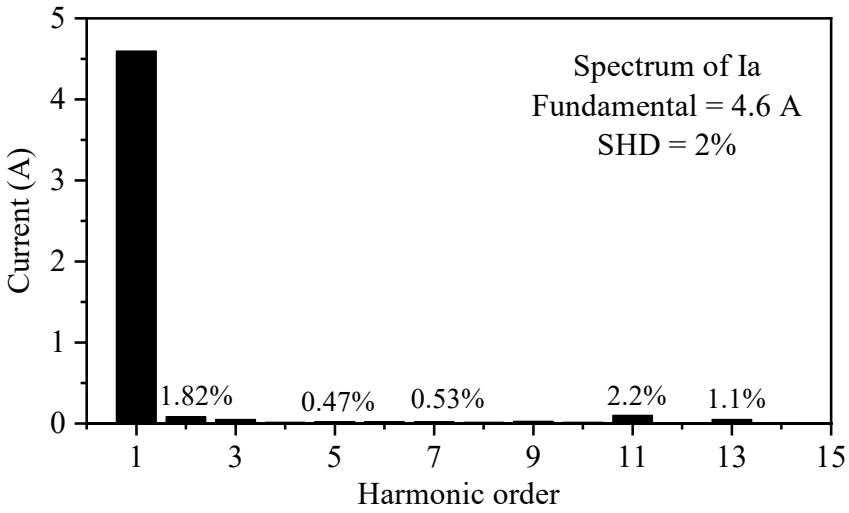
3.4.2.4 Test Results of the Proposed Method

The experimental result with the proposed Adaline based current harmonics suppression method is presented in Fig. 3.23. As shown in the figure, the current shows a sinusoidal waveform. Compared with the cases without compensation or offline compensation, the current waveform is improved significantly. The low order current harmonics are almost eliminated. Compared with two other methods that consider only dead time effect or the back-EMF harmonics, the proposed method generates precise compensation voltages. Both the dead time effect and the back-EMF harmonics are compensated with the proposed method.

The phase current SHD of the proposed method declines dramatically from 9% to 2%. It should also be noticed that since the Adaline compensation voltage generator can adaptively tuned the feedforward voltage, other periodic non-ideal factors that cause voltage distortion can also be compensated. The proposed method does not use inverter parameters, motor parameters and the EMF information to calculate the compensation voltage. Same as the simulation results, the measured 11th and 13th harmonics of phase current still exist after employing the compensation method. These harmonics can be further eliminated through adding more Adaline inputs. These results clearly indicate the effectiveness of the proposed method.



(a) Phase current waveform.



(b) Phase current spectrum.

Fig. 3.23. Experimental phase A current waveform and spectrum when motor is operating at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz) at rated load with the proposed current harmonics suppression method.

3.4.3 Transient State Experimental Results

Fig. 3.24 shows the measured waveforms during torque transient state with the proposed current harmonics suppression method. The speed is kept at $\omega_e = 400\pi$ rad/s ($f_e = 200$ Hz). The load increases during the transient state. As can be seen, the proposed method can also work well for the transient state. The q-axis current increases from 3A to 6A during the transient state test. With the increase of motor load, the amplitude of the phase current increases while the current is still sinusoidal. Overall, the proposed method shows good performance under both steady and transient states.

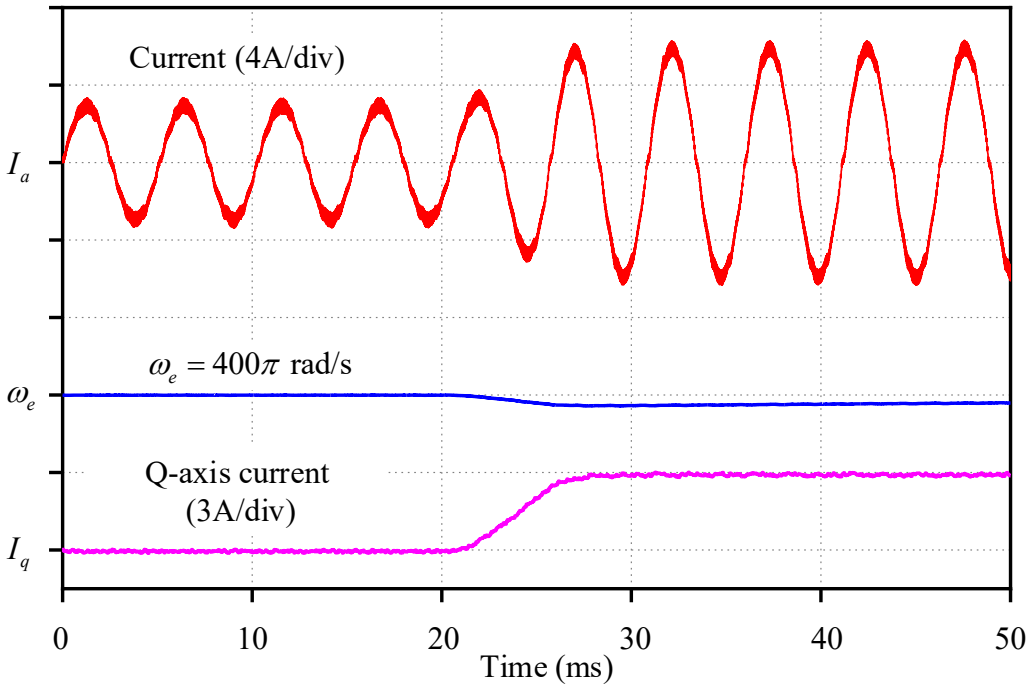


Fig. 3.24. Torque transient state results.

3.5 Conclusion

In this chapter, a neural-network based Adaline current harmonics suppression method is proposed for PM brushless motors with non-sinusoidal back electromotive force under BLAC control. The current harmonics can be well suppressed by feedforwarding an adaptively generated compensation voltage. Thanks to the Adaline algorithm, the current harmonics extraction is not needed for the feedforward compensation voltage generation process which reduces the computation burden. Compared with the traditional inverter nonlinearity only compensation method or the offline back-EMF harmonics compensation method based on LUT, the proposed self-tuning current harmonics compensator does not need the knowledge of back-EMF harmonic components and the dead time effect. Thus, a more precise compensation voltage could be generated. The proposed current harmonics suppression method also does not need additional hardware. The effectiveness of the proposed current harmonics method is verified by simulation and experimental results under both steady and transient states.

CHAPTER 4

COMMUTATION OPTIMIZATION STRATEGY FOR HIGH SPEED BRUSHLESS DC DRIVES WITH INACCURATE ROTOR POSITION SIGNALS

In Chapter 2 and Chapter 3, brushless alternating current (BLAC) drives are investigated and the current harmonics suppression methods are proposed. Although BLAC drives have the advantages of low torque ripples and reliable dynamic performances, the relatively complex control algorithms limit their application in high speed drive systems. Thus, brushless direct current (BLDC) drives are also considered in this thesis. The control performance of Hall sensor based high speed BLDC motor drives depends heavily on the accuracy of Hall sensor signals. Due to the existence of Hall signal errors, the system may operate under unbalanced conditions which will lead to asymmetric currents and high torque ripple. For high speed drive, the pulse-width modulation (PWM) update delay will also lead to inaccurate commutation. In this chapter, two Hall signal errors, i.e., misaligned and uneven Hall signal errors, are investigated and a Hall signal balancing strategy is developed to detect Hall signal errors and regenerate balanced Hall signals. A new PWM generation scheme is then proposed to eliminate the PWM update delay. Both simulation and experiment results have verified the effectiveness of the proposed strategy.

4.1 Introduction

Permanent magnet brushless motors are widely employed for many high speed applications due to their robust structure and high reliability [ZWY08] [SIL14]. For a high speed BLDC drive system where the inverter commutates every 60 electrical degrees, six discrete commutation points are vital for the control performance. Inaccurate commutation points will lead to unbalanced operation of the system where the conducting interval of one phase is different from others, causing asymmetric current waveforms, high torque ripple, and low system efficiency. The commutation points of BLDC drives can be detected from both sensorless schemes and position sensors.

For high speed BLDC sensorless schemes, the zero-crossing points (ZCPs) of the back-electromotive forces (EMFs) are usually used to detect the commutation points. However, the use of ZCP based sensorless methods is limited during start-up process. At zero and low speed range, the back-EMFs are not high enough for accurate ZCP detection. Specific start-up strategies are thus required [ZHO18]. Besides, for ZCP based sensorless methods, low-pass filters (LPFs) are needed in order to avoid false commutations [ZHO17B]. An inevitable LPF delay error will thus occur [LIW16]. Besides, asymmetric machine parameters [AHF10], non-ideal EMF shapes [CHE17B] and armature reaction [SHE03] also have a negative influence on the accuracy of detected ZCPs. The flux linkage based sensorless scheme may also be not suitable for high speed drives since it requires high sampling rate and heavy computation burden [CHE18B].

Hall sensors, on the other hand, are also widely used in high speed BLDC drives due to advantages of simplicity and robustness in wide speed and load range. When Hall sensors are used, machine parameters, EMF waveform, and armature reaction have no effect on detected Hall signals. Besides, since there is no high frequency noise in Hall signals, the effect of LPFs can also be neglected. Thus, in this chapter, Hall sensors are used to obtain commutation points. Nevertheless, Hall signal errors will still cause inaccurate commutation [FAN14]. In theory, three Hall signals should be 120 electrical degrees apart from each other. Nevertheless, Hall sensor placements are not always precise in practical conditions especially when the motor size is small. Manually adjusting the placements of sensors could solve the problem. However, it is not practical for mass production. Even if there is no Hall sensor misalignment, the phenomenon of uneven Hall signals exists, where the interval of one Hall signal during either its high or low state is not 180 electrical degrees. These two non-ideal factors will cause unbalanced operation of the system. Besides, the drive technique will cause commutation delay. In order to adjust the speed and torque of a high speed motor, the pulse-width modulation (PWM) drive technique is widely implemented to adjust the supply voltages. For a full-digital implementation system, voltage command PWM signals are generated once during each PWM period. Thus, they cannot be updated immediately at commutation instant. There will be an inevitable phase delay between the detected commutation point and the actual generated commutation point [CUI15A]. For high speed drives, this phenomenon becomes more severe.

Many researches have focused on solving the Hall signal error problem. In [SAM07A], the authors propose a method that uses a simple single-input-single-output filter to obtain the moving-average-filtering (MAF) value of Hall sensor signals. In [SAM07B] and [SAM08],

several multi-input-multi-output MAF techniques are proposed to improve the previous mentioned method and mitigate the effect of unbalanced placements of the Hall sensors. The dynamic performances of the system are also compared before and after the Hall sensor misalignment compensation. In [ALA12], the MAF techniques are modified and the authors propose the digital implementation of the filters. A balanced operation among the phases is achieved. However, the proposed MAF techniques are rather complex to implement. In [FAN14], the authors propose a method based on DC-link current to compensate the Hall sensor misalignment. Although the proposed method can achieve good performance, the computation burden is heavy and additional DC-link current sensors are needed. In [PAR17] and [ZHA18], the misaligned Hall sensor signals are compensated from the DC-link current and voltage information. All the aforementioned compensation methods are valid only under the assumption that the Hall signals are evenly generated during one fundamental period, i.e., the interval duration of the Hall signal output is 180 degrees when the signal is at either high or low state. Nevertheless, this is not always the true. In [SEO17], the causes of uneven Hall sensor signals are comprehensively analysed. The authors point out that several reasons, such as the threshold effect of Hall sensor, the reduction of magnetic flux density and different placement heights of the Hall sensors, could lead to the generation of uneven Hall signals. The authors also propose an optimal design strategy to solve the uneven Hall signals problems. The same researchers also propose a control technique in [LEE18A] to compensate the uneven Hall sensor signals. However, the Hall sensor misalignment problem is not considered.

The PWM update delay is considered by many researchers. In [BAE03A], the error caused by implementing the PWM technique in BLAC drive is analysed. The authors point out that if the PWM signals are updated at each sampling point, the minimum time delay would be one-and-a-half sampling periods. A compensation method for the PWM delay in the full-digital synchronous current regulator is also proposed. Many other compensation methods for BLAC control are proposed [ZHA19] [CHO12]. However, these proposed methods are valid under the assumption that PWM update delay is constant. However, this is not the case for the BLDC drive. In [KIM02], the PWM update delay problem for the BLDC drive is firstly presented. However, no compensation method for the PWM control is proposed in that paper. In [CUI15A], the PWM update delay under BLDC control is analysed. The authors point out that since the commutation signal may occur at any time during one PWM period, the PWM update delay is not constant. A pulse-amplitude modulation (PAM) technique using the two-stage inverter is proposed. The authors also compare the PWM and PAM control. It is shown that by

using the PAM control, the commutation delay caused by the digital implementation could be eliminated since the PWM chopper signals are no longer needed. However, the realization of PAM control requires a front-end converter to adjust the DC voltage supply [SCH14]. Thus, the control complexity and the cost of the system will be increased.

In brief, Hall sensor signal errors are caused by several different non-ideal factors. However, most of existing researches consider only one non-ideal factor, and some even need additional DC-link current and voltage information to generate balanced Hall signals. In this chapter, a Hall signal balancing method is firstly proposed considering different non-ideal factors together. Then, in order to eliminate the PWM caused commutation delay, a novel PWM generation scheme is also proposed for BLDC drives. Thus, a balanced operation of the system could be achieved. The effectiveness of the proposed commutation optimization method is verified through both simulation and experimental results.

4.2 Hall Signal Errors and PWM Update Delay Analysis of BLDC Drive System

The motor parameters of three phases are assumed to be identical in this chapter in order to simplify the analysis. The block diagram of a BLDC drive system with a general three-phase inverter is shown in Fig. 4.1, together with three inaccurate Hall sensors H_A, H_B and H_C.

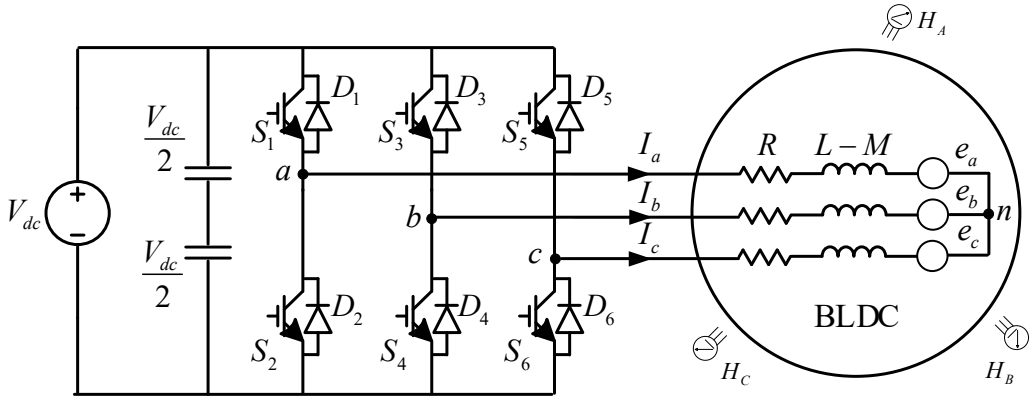


Fig. 4.1. Block diagram of BLDC drive system with Hall sensors.

The voltage equations of a BLDC motor can be expressed as

$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = R \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + (L-M)\frac{d}{dt}\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{4-1}$$

where R is the stator resistance, L and M are the self and mutual winding inductances. $U_{an,bn,cn}$, $I_{a,b,c}$ and $e_{a,b,c}$ are the three-phase supply voltages, phase currents and phase back-EMFs, respectively. The detected Hall signals and the phase back-EMFs are shown in Fig. 4.2, while the relationship between Hall signals $H_{a,b,c}$, the sector number N and the drive signals S_{1-6} are shown in Table 4.1.

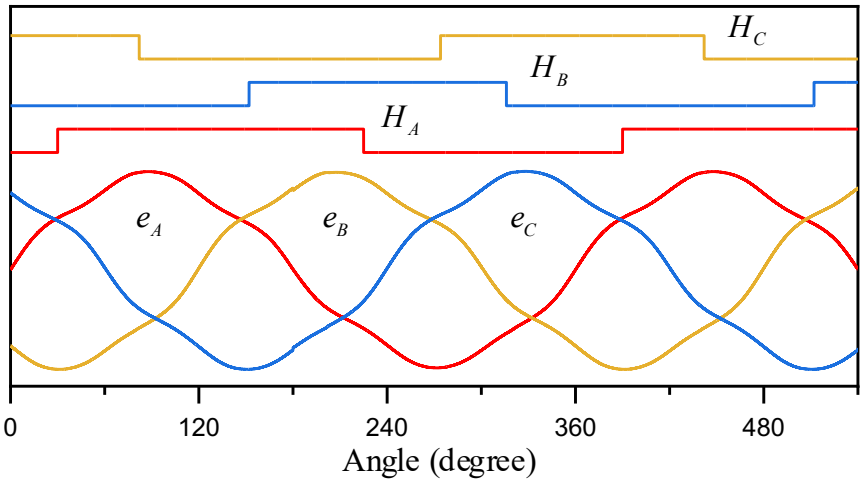


Fig. 4.2. Detected Hall signals and phase back-EMFs.

Table 4.1 RELATIONSHIP OF HALL SIGNALS, SECTOR NUMBER AND DRIVE SIGNALS

$H_aH_bH_c$	Sector number (N)	Drive signals (S_1- S_6)
101	I (A+B-C~)	100100
100	II (A+B~C-)	100001
110	III (A~B+C-)	001001
010	IV (A-B+C~)	011000
011	V (A-B~C+)	010010
001	VI (A~B-C+)	000110

4.2.1 Analysis of Misaligned Hall Signal Error

In theory, three Hall sensors should be placed exactly 120 electrical degrees apart. However, this assumption is not true for most circumstances. When the placements are not accurate, the misaligned Hall signal error can be represented by ε_{mis_A}, ε_{mis_B} and ε_{mis_C} accordingly for

the three Hall sensors. If the Hall sensor is retarded from the ideal position, the error has a positive value while the error has a negative value when the sensor is advanced from the ideal position. Thus, the detected rising and falling edges of Hall signals $H_{ra,b,c}$ and $H_{fa,b,c}$ can be expressed according to the rising and falling edges of ideal Hall sensor signals $H'_{ra,b,c}$ and $H'_{fa,b,c}$, together with the misaligned Hall signal errors as

$$H_{ra} = H_{ra}{}' + \varepsilon_{mis\_A} \quad H_{fa} = H_{fa}{}' + \varepsilon_{mis\_A} \tag{4-2}$$

$$H_{rb} = H_{rb}{}' + \varepsilon_{mis\_B} \quad H_{fb} = H_{fb}{}' + \varepsilon_{mis\_B} \tag{4-3}$$

$$H_{rc} = H_{rc}{}' + \varepsilon_{mis\_C} \quad H_{fc} = H_{fc}{}' + \varepsilon_{mis\_C} \tag{4-4}$$

4.2.2 Analysis of Uneven Hall Signal Error

Apart from the misaligned Hall signal error, the Hall sensors also suffer from the problem of unequal high and low state intervals, causing the commutation point shifted from accurate position. This is often caused by the threshold effect of the Hall sensor [SEO17] as shown in Fig. 4.3. In order to generate a Hall signal, the flux density B that passes through the Hall sensor must exceed the threshold operating flux density B_H of the sensor. If the Hall sensors are placed at different distances from the ideal positions or if the magnetic flux density reduces with the temperature, the flux density passing through the sensor would be different as shown as B_1 and B_2. Then, different Hall signal H_1 and H_2 with corresponding uneven errors ε_{une1} and ε_{une2} will be generated.

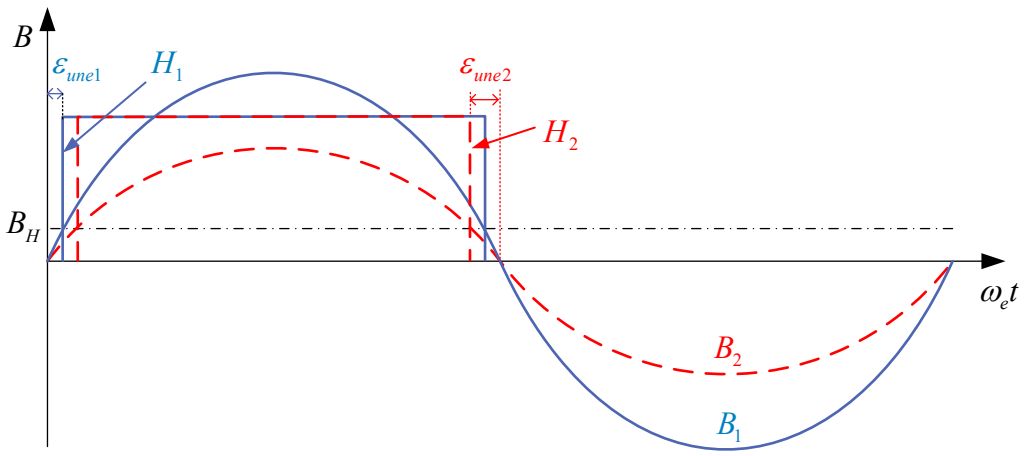


Fig. 4.3. Relationship between flux density and Hall signal considering threshold effect.

Assuming that the difference between the high and low state intervals of the three Hall sensors are $4\varepsilon_{une\_A}$, $4\varepsilon_{une\_B}$ and $4\varepsilon_{une\_C}$ respectively. If the high state interval is longer than and the low state interval, then ε_{une} has a positive value. Otherwise, the value is negative. Then, the detected rising and falling edges of Hall signals $H_{ra,b,c}$ and $H_{fa,b,c}$ can be expressed according the rising and falling edges of ideal Hall sensor signals $H'_{ra,b,c}$ and $H'_{fa,b,c}$, together with the uneven Hall signal error, as

$$H_{ra} = H_{ra}{}' - \varepsilon_{une\_A} \quad H_{fa} = H_{fa}{}' + \varepsilon_{une\_A} \tag{4-5}$$

$$H_{rb} = H_{rb}{}' - \varepsilon_{une\_B} \quad H_{fb} = H_{fb}{}' + \varepsilon_{une\_B} \tag{4-6}$$

$$H_{rc} = H_{rc}{}' - \varepsilon_{une\_C} \quad H_{fc} = H_{fc}{}' + \varepsilon_{une\_C} \tag{4-7}$$

4.2.3 PWM Update Delay of BLDC Drive

In order to regulate the BLDC motor speed, a variable voltage that is applied to the motor terminals is generated by the PWM technique [MIL12]. The fundamental reason that causes the PWM update delay for BLDC control is that when PWM technique is used, the commutation and the speed adjustment are coupled. For a full-digital implementation system, the PWM signals are usually generated by two different registers, i.e., the time-base period (TBPRD) register and the counter-compare (CMPA/B) register. The frequency of the PWM signals are controlled by TBPRD value and the mode of the time-base counter. Usually, the up-and-down count mode is chosen so that the symmetrical triangular carrier is generated. In this mode, the time-base counter starts from zero and increases until the TBPRD value is reached. When the period value is reached, the time-base counter then decreases until it reaches zero. At this point the counter repeats the pattern and begins to increment. The frequency of the PWM can be expressed as

$$f_{PWM} = \frac{1}{2 \times TBPRD \times t_{TBPRD}} \tag{4-8}$$

where $TBPRD$ is the register value while t_{TBPRD} is the time-base counter period.

The CMPA/B register is used to modulate the duty ratio. The CMPA/B value is continuously compared to the time-base counter value. Thus, when the time-base counter value equals the CMPA/B values, an appropriate event will occur. However, it should be noticed that the CMPA/B register has an associate shadow register which only allows the CMPA/B values to

update at strategic points. Usually, the CMPA/B values are updated at the instant when time-base counter value reaches zero. Thus, for a BLDC drive, when the commutation signal arrives, the PWM signals of the current period keep the same and they cannot be changed until the next PWM period. Taking the instant when the sector changes from Sector II to Sector III for example. The PWM signals are shown in Fig. 4.4.

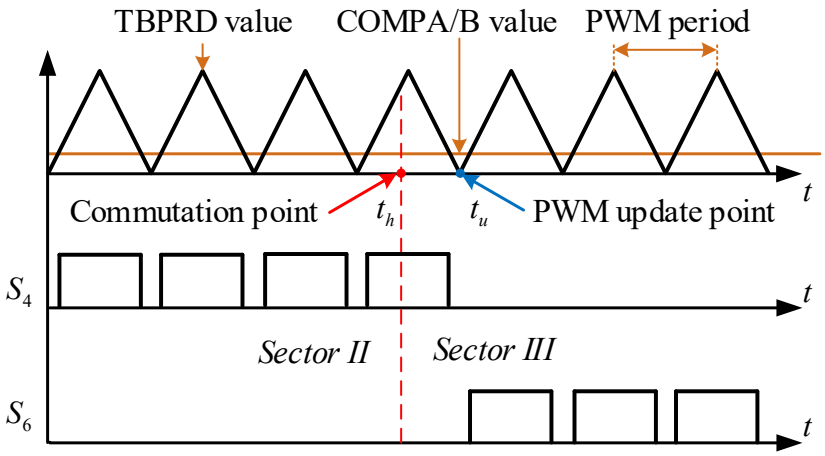


Fig. 4.4. PWM signals under BLDC control from Sector II to Sector III.

The BLDC control system is operating under H-ON-L-PWM mode. Before the rising edge of Hall B H_{rb} arrives, the upper bridge of phase A is ON, the lower bridge of phase B is on chopper mode, while the lower bridge of phase C is OFF. At the instant of the ideal commutation point t_h, the phase A signal does not change. Since the PWM signals cannot change instantly, the phase B switch S_4 is still chopping. The phase C switch S_6 starts working on chopper mode after the PWM update point t_u. Thus, there is an update delay between the commutation point and the PWM update point which can be expressed as

$$\varepsilon_{PWM\_delay} = t_h - t_u \tag{4-9}$$

It should be noticed that the Hall signals may happen at any point during one PWM period. Thus, the PWM update delay is not constant. The maximum delay may be as long as one PWM period. Thus, a proper method should be considered to solve this problem, as will be described in the next section.

4.3 Proposed Commutation Optimization Method for BLDC Drive System

As shown in the previous analyses, due to the misaligned and uneven Hall signal errors, the commutation points are no longer accurate and will lead to unbalanced operation of the system.

Besides, the PWM update will also cause the commutation points shift with the ideal position. In this section, a Hall signal balancing method is proposed for the BLDC drive. In the proposed method, the rising and falling edges of three Hall sensor signals are detected at time t_x, as shown in Table 4.2. After obtaining the balanced Hall signals, a novel PWM generation scheme is proposed for BLDC drive so that the PWM update delay is eliminated.

TABLE 4.2 Relationship Between Hall Signal and Edge Detection Time

Hall signal	Rising edge	Falling edge
H_a	t_1	t_4
H_b	t_3	t_6
H_c	t_5	t_2

4.3.1 Analysis of Misaligned Hall Signal Error

The time interval of each sector can be measured based on the detected Hall signals. Taking sector I for example, the time interval from t_1 to t_2 can be expressed as

$$\tau_{12} = t_2 - t_1 \tag{4-10}$$

The time intervals of other sectors $\tau_{xy} = t_y$-t_x can also be defined accordingly. The subscript denotes the sector interval from detection time t_x to t_y. Then, the angular interval of sector I is calculated as

$$\theta_{12} = \frac{t_2 - t_1}{T} \tag{4-11}$$

where T is the time period of one electrical cycle. T can be obtained from the last six time intervals as

$$T = (\tau_{12} + \tau_{23} + \tau_{34} + \tau_{45} + \tau_{56} + \tau_{61}) \tag{4-12}$$

Since the detected Hall signals are deviated from the ideal signals, the detected sector angular intervals are also different from the ideal ones. Still taking sector I for example, the relationship between the detected sector angular interval, the ideal sector angular interval and the Hall signal errors can be expressed as

$$\theta_{12} = \theta_{12}{}' - \varepsilon_{mis\_A} + \varepsilon_{mis\_C} + \varepsilon_{une\_A} + \varepsilon_{une\_C} \tag{4-13}$$

where θ'_{12} is the ideal angular interval of sector I.

The relationships of the Hall signals, the sectors and the corresponding sector angular intervals are presented in Fig. 4.5.

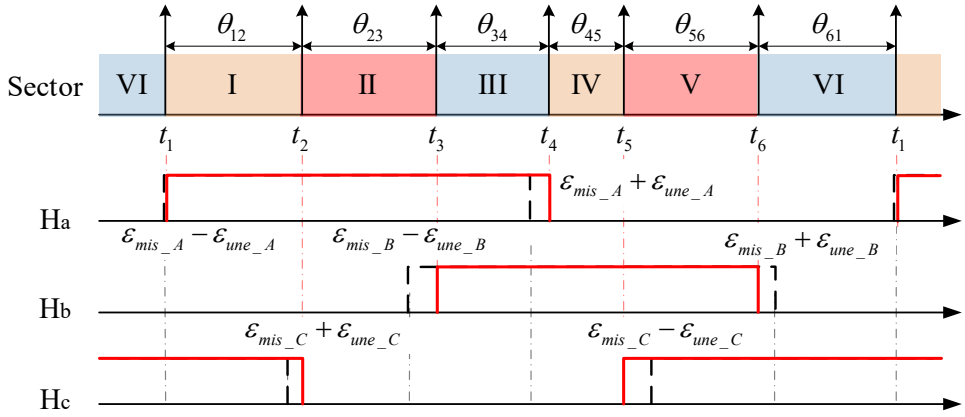


Fig. 4.5. Relationship of detected Hall signals, ideal Hall signals and corresponding sectors.

From the top to the bottom, the sector angular intervals, the sectors according to the detected Hall signals and the Hall signals are given. The detected Hall signals are marked in red line while the ideal Hall signals are marked in black dash line.

The six detected sector angular intervals can be expressed based on the ideal sector angular intervals and the Hall signal errors as

$$\begin{bmatrix}\theta_{12}\\ \theta_{23}\\ \theta_{34}\\ \theta_{45}\\ \theta_{56}\\ \theta_{61}\end{bmatrix} = \begin{bmatrix}-1 & 0 & 1 & 1 & 0 & 1\\ 0 & 1 & -1 & 0 & -1 & -1\\ 1 & -1 & 0 & 1 & 1 & 0\\ -1 & 0 & 1 & -1 & 0 & -1\\ 0 & 1 & -1 & 0 & 1 & 1\\ 1 & -1 & 0 & -1 & -1 & 0\end{bmatrix}\begin{bmatrix}\varepsilon_{mis\_A}\\ \varepsilon_{mis\_B}\\ \varepsilon_{mis\_C}\\ \varepsilon_{une\_A}\\ \varepsilon_{une\_B}\\ \varepsilon_{une\_C}\end{bmatrix} + \begin{bmatrix}\theta_{12}{}'\\ \theta_{23}{}'\\ \theta_{34}{}'\\ \theta_{45}{}'\\ \theta_{56}{}'\\ \theta_{61}{}'\end{bmatrix} \tag{4-14}$$

Since all the six ideal sector angular intervals are equal to one-sixth of one fundamental electrical period, they can be substituted as

$$\theta_{12}{}' = \theta_{23}{}' = \theta_{34}{}' = \theta_{45}{}' = \theta_{56}{}' = \theta_{61}{}' = \frac{\pi}{3} \tag{4-15}$$

Then, the Hall signal errors can be deduced by solving (4-12)-(4-14) as

$$\begin{bmatrix}\varepsilon_{mis\_A}\\ \varepsilon_{mis\_B}\\ \varepsilon_{mis\_C}\\ \varepsilon_{une\_A}\\ \varepsilon_{une\_B}\\ \varepsilon_{une\_C}\end{bmatrix}=\begin{bmatrix}-1/3 & -1/6 & 0 & -1/3 & -1/6 & 0\\ -1/6 & 0 & -1/3 & -1/6 & 0 & -1/3\\ 0 & -1/3 & -1/6 & 0 & -1/3 & -1/6\\ 1/12 & 1/12 & 1/12 & -5/12 & -5/12 & -5/12\\ -5/12 & -5/12 & 1/12 & 1/12 & 1/12 & -5/12\\ 1/12 & 1/12 & -5/12 & -5/12 & -5/12 & 1/12\end{bmatrix}\begin{bmatrix}\Delta\theta_{12}\\ \Delta\theta_{23}\\ \Delta\theta_{34}\\ \Delta\theta_{45}\\ \Delta\theta_{56}\\ \Delta\theta_{61}\end{bmatrix} \tag{4-16}$$

As shown in the previous analysis, the Hall signal errors could be obtained from the detected Hall signals. In this chapter, the rising and falling edges of Hall signals will both trigger an interrupt, and a DSP timer is used to detect and store the Hall edge instants $t_x(n)$. Here, n denotes the n[th] sample of the corresponding signal. Based on (4-10) and (4-11), the sector angular intervals $\tau_{xy}(n)$ can be calculated. Then, the Hall signal errors can be calculated based on (4-16). The Hall signals and the commutation points can be modified by reducing the Hall signal errors to zero. The proportional–integral (PI) controllers are used to generate the compensation signals. Using the PI scheme, the compensation signals for three phase misaligned Hall signal errors $\varepsilon_{cm\_A,B,C}(n)$ and uneven Hall signal errors $\varepsilon_{cu\_A,B,C}(n)$ can be determined as

$$\varepsilon_c = -(k_p + \frac{1}{s}k_i)\cdot\varepsilon_{mis} \tag{4-17}$$

where k_p and k_i are the PI gains.

After obtaining the compensation signals, the Hall signals are modified to trigger the next interrupt so that a balancing operation of the system could be achieved after the Hall signal balancing process is completed. Taking the rising and falling edges of Hall A signal as example, the Hall signal at the n+1[th] commutation instants can be expressed as

$$\begin{aligned} t_1(n+1) &= t_1(n) + \left[\frac{-\varepsilon_{cm_A}(n) + \varepsilon_{cu_A}(n)}{2\pi} + 1\right]T \\ t_4(n+1) &= t_4(n) - \left[\frac{\varepsilon_{cm\_A}(n) + \varepsilon_{cu\_A}(n)}{2\pi} - 1\right]T \end{aligned} \tag{4-18}$$

The other signals can be compensated accordingly. The flowchart of the proposed Hall signal balancing method is shown in Fig. 4.6.

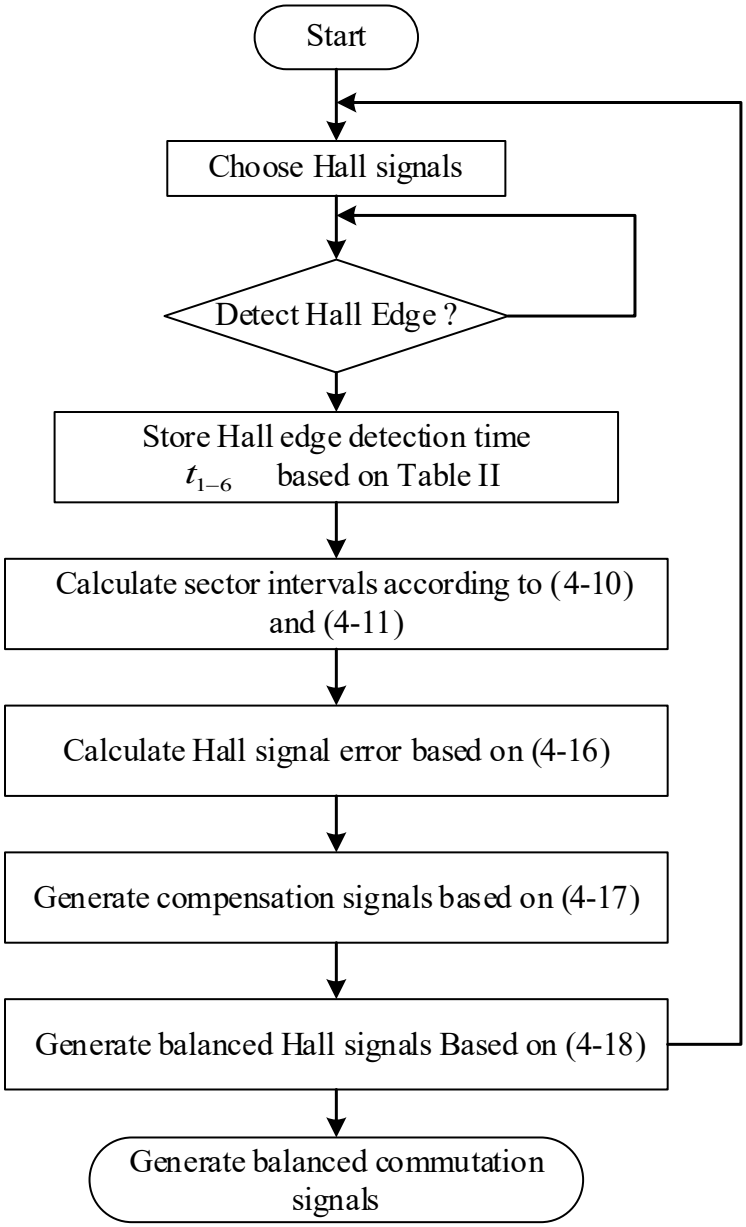


Fig. 4.6. Flowchart of proposed Hall signal balancing method.

4.3.2 Proposed PWM Generation Scheme

As analysed in the previous section, the traditional PWM generation scheme for BLDC control will cause the PWM signal update delays especially under high speed. The commutation process would be different from the ideal condition. Thus, a new PWM generation scheme that can decouple the commutation and the speed adjustment is considered. In order to achieve this, the balanced Hall signals are used together with the chopping PWM signal. The duty ratio of the PWM signal is still determined by the speed controller so that the motor speed can be adjusted. Rather than generating the PWM signal separately for different phases in each sector, a preliminary PWM signal S_{pwm} which is only related with the speed controller is generated.

Then, the preliminary PWM signal S_{pwm} and the balanced Hall signals are controlled by logical operator to generate the new PWM signals. It should be noticed that the logical operator can be achieved by either additional logical circuit or on-chip module of the microcontroller. Thus, the proposed PWM generation scheme can be applied to the mainstream system. Since the H-ON-L-PWM mode is used, only the lower bridge switches suffer from the PWM delay. The proposed PWM generation scheme for $S_{2,4,6}$ are shown in Fig. 4.7.

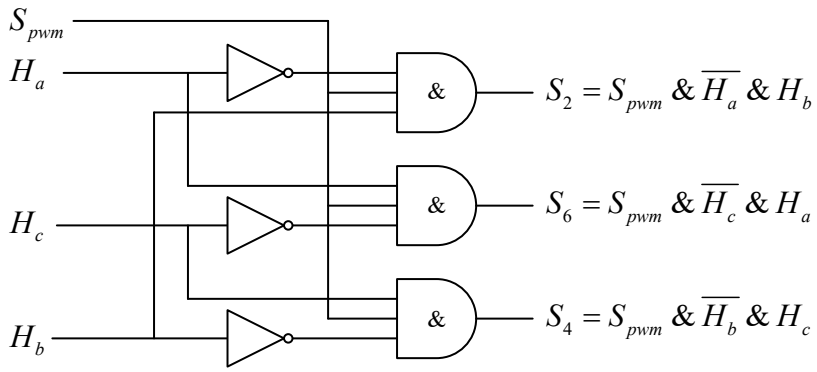


Fig. 4.7. Proposed PWM generation scheme.

Still taking the instant when the sector changes from sector II to sector III for example. The PWM signals and the balanced Hall signals with the proposed PWM generation scheme when the sector is changing from sector II to sector III is shown in Fig. 4.8.

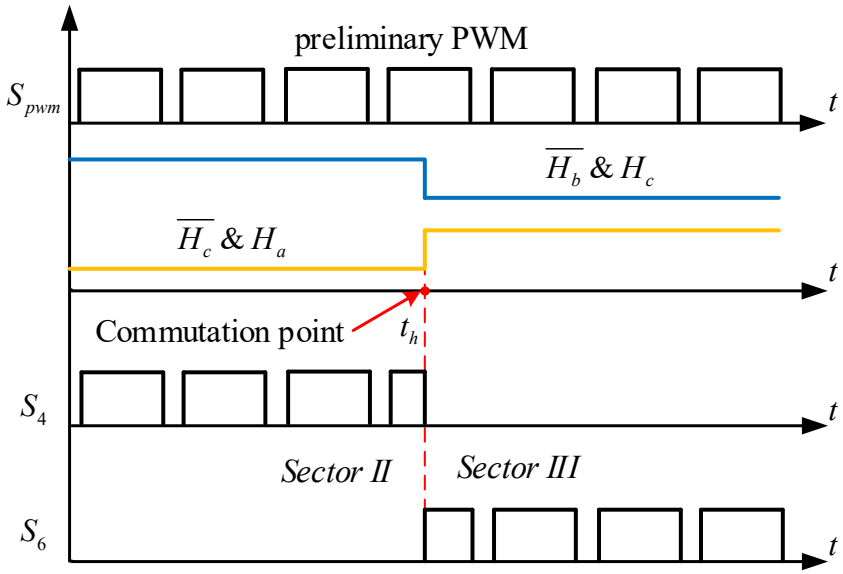


Fig. 4.8. PWM signals from Sector II to Sector III with proposed PWM generation scheme.

The Hall signals $H_aH_bH_c$ change from 101 to 100. In order to avoid the PWM update delay, the chopping PWM signal of phase B switch S_4 should be terminated as soon as the

commutation point arrives. At the same time, the switch S_6 should start to chop. Before the commutation instant, $\overline{H_b}\&H_c$ is 1 while $\overline{H_c}\&H_a$ is 0. Thus, the switch S_4 is chopping while the switch S_6 is OFF. After the commutation instant, $\overline{H_b}\&H_c$ changes to 0 so that the switch S_4 is terminated. The switch S_6 starts to work on chopping mode. The PWM signals at other commutation instant can be generated accordingly. The PWM update delay can be eliminated with the proposed PWM generation scheme.

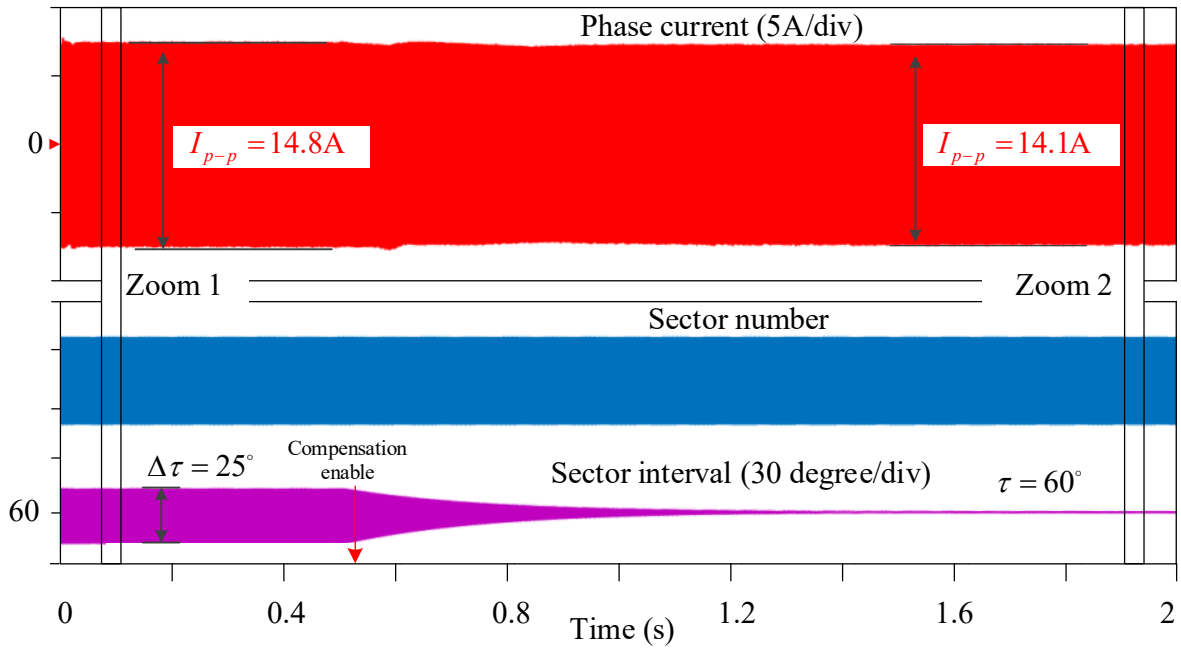
4.4 Simulation and Experimental Verification

4.4.1 Simulation Verification

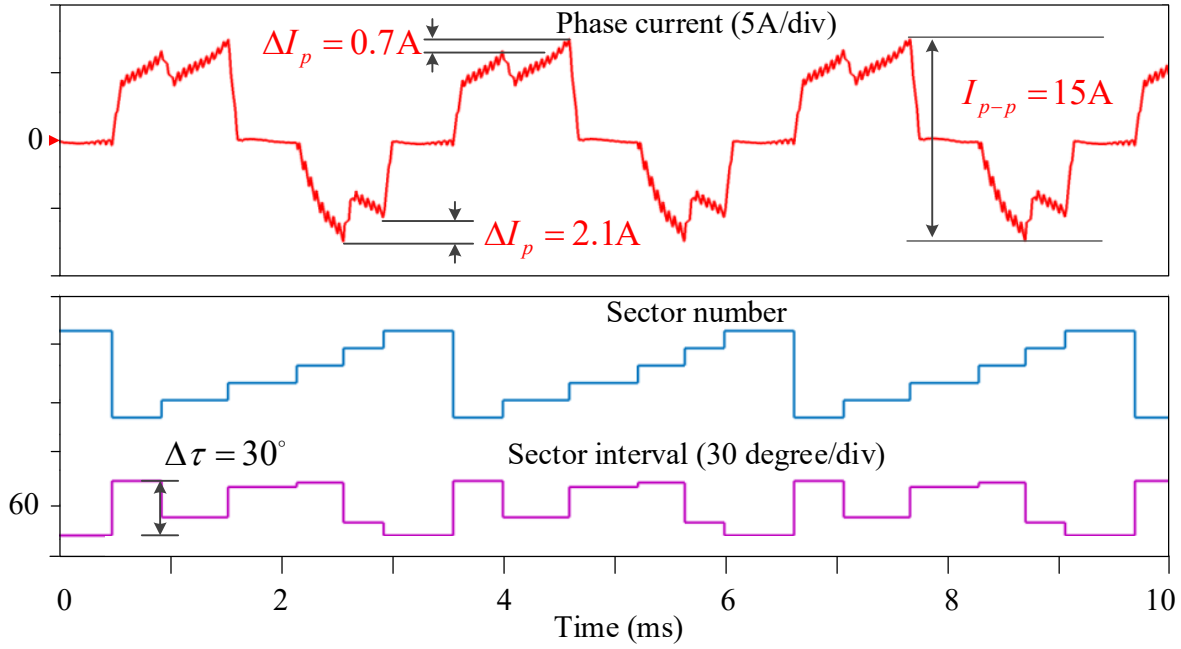
To verify the effectiveness of the proposed Hall signal balancing method, a simulation model is built in MATLAB/Simulink. The characteristic parameters of the motor are given in the Appendix. The switch frequency is set to 20 kHz. The three misaligned Hall signal errors ε_{mis_A}, ε_{mis_B} and ε_{mis_C} are 7°, -6° and -2° while the uneven Hall signal errors ε_{une_A}, ε_{une_B} and ε_{une_C} are 7°, -8° and -6° respectively.

The simulation results before and after employing the proposed Hall signal balancing method when motor is operating at $\omega_e = 667\pi$ rad/s ($f_e = 333.3$ Hz) under full load (0.3 Nm) are given in Fig. 4.9. The phase current, the sector number and sector intervals are shown from the top to the bottom in Fig. 4.9(a). The Hall signal balancing method is enabled at 0.5s while the results in Zoom 1 and Zoom 2 are shown in Fig. 4.9(b) and Fig. 4.9(c) respectively.

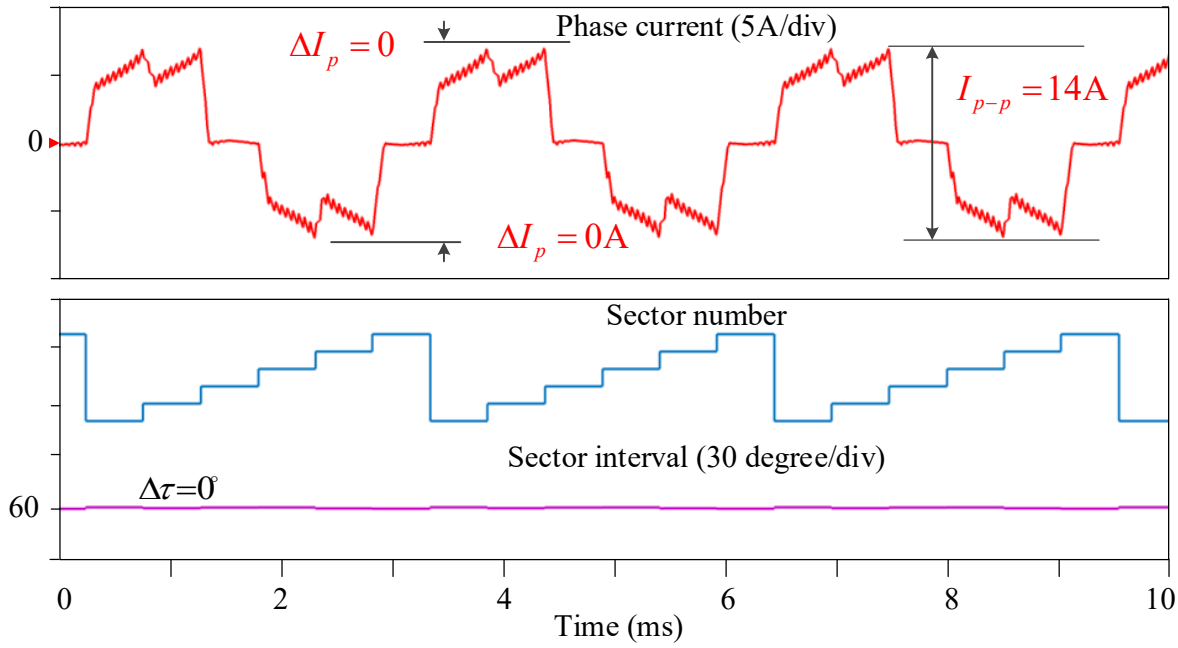
As shown in Fig. 4.9(a), before the Hall signal balancing method is enabled, the intervals of each sector are not always 60° due to the existence of the Hall signal errors. The interval difference $\Delta\tau$ between the longest interval τ_{61} and the shortest interval τ_{56} could be as much as 30°. This unbalanced operation could also be seen in Fig. 4.9(b), where the current waveform is no longer symmetrical and also not cyclic for sector intervals. The current peak value during different sectors are also different from each other. As shown in Fig. 4.9(b), the maximum difference in current peaks can be as large as 2.1A. After the proposed method is enabled, the sector intervals gradually converge to 60° so that the interval difference $\Delta\tau$ is reduced to zero. Thus, a balancing operation of the system is achieved. The maximum difference in current peaks is reduced to zero while the P-P value of phase current also reduces to 14A. As shown in Fig. 4.9(c), the phase current is symmetrical and the six sector intervals are identical, together with almost identical current peaks.



(a) Hall signal balancing process.



(b) Results without Hall signal balancing method in Zoom 1.



(c) Results with Hall signal balancing method in Zoom 2.

Fig. 4.9. Simulation results of phase current, sector number and sector intervals when motor is operating at $\omega_e = 667\pi$ rad/s ($f_e = 333.3$ Hz) under full load.

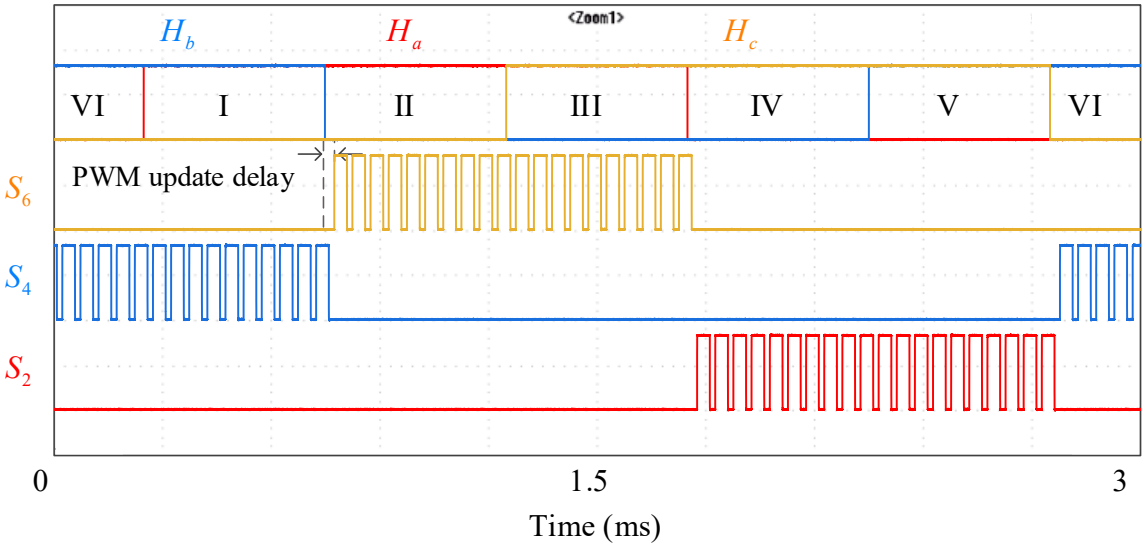
4.4.2 Experimental Verification

The proposed method is also applied to a BLDC drive system and implemented using the test rig presented in the Appendix. The parameters of the motor are the same as those used in the simulation. The motor is still operating at $\omega_e = 667\pi$ rad/s ($f_e = 333.3$ Hz). The switching frequency is still set to be 20k Hz. The DC supply voltage is 100V.

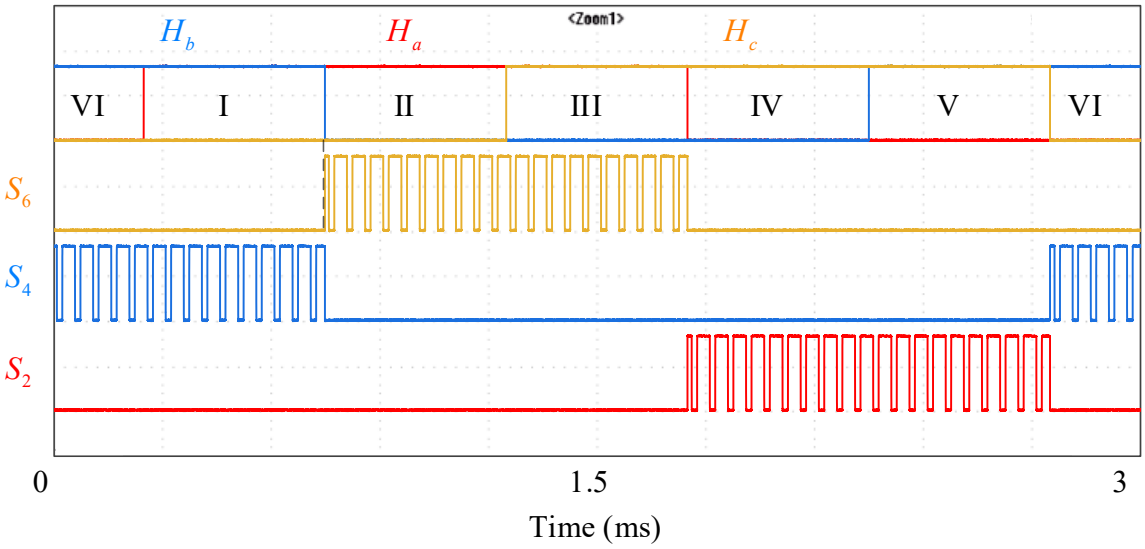
In Fig. 4.10, the PWM signals of different switches in one fundamental period are presented to prove the effectiveness of the proposed PWM generation scheme. From the top to the bottom, the Hall signals and PWM signals of phase C, phase B, phase A are shown accordingly.

As shown in Fig. 4.10(a), when the conventional PWM is used, there exists the PWM update delay. As analyzed in the previous section, since the commutation signals may occur at any instant during one PWM period, the PWM delay is inconstant. It should be noticed that with the variation speed and load conditions, the situation might be different. Nevertheless, the PWM update delay always exists. The PWM signals under the proposed generation scheme is given in Fig. 4.10(b). Taking the instant when the sector switches from Sector I to Sector II for example, as shown in the figure, the phase B switch S_4 is turned off immediately. At the same

time, the phase C switch S_6 starts to chop. Thus, the PWM delay is eliminated. Overall, the effectiveness of the proposed PWM generation scheme is proved.



(a) Conventional PWM generation scheme.

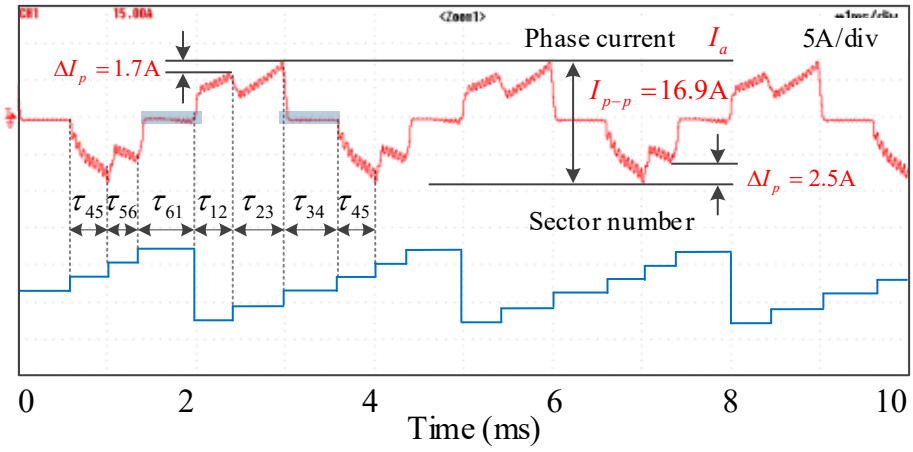


(b) Proposed PWM generation scheme.

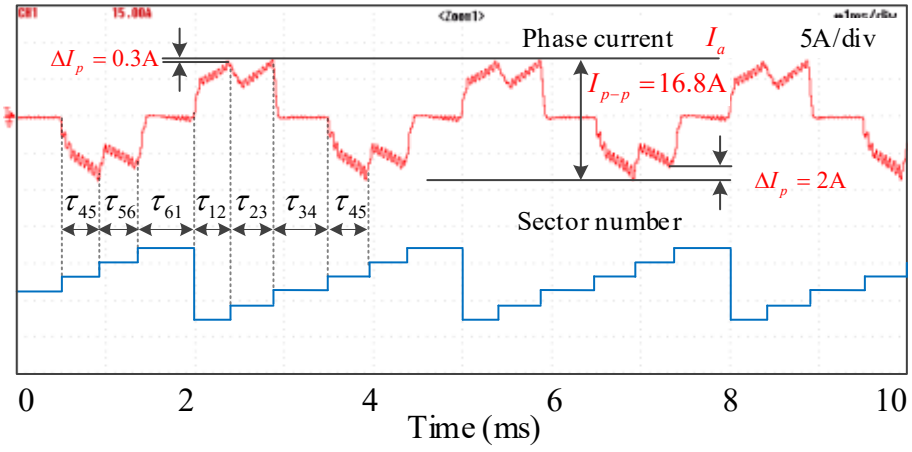
Fig. 4.10. PWM signals with conventional and proposed PWM generation scheme.

Several experiments have been taken to verify the effectiveness of the proposed Hall signal balancing method under different conditions. In Fig. 4.11, the experimental results when motor is operating at $\omega_e = 667\pi$ rad/s ($f_e = 333.3$ Hz) under full load are given. The results without any Hall signal errors compensation, with only uneven Hall signal errors compensation, with misaligned Hall signal errors compensation and with the proposed Hall signal balancing

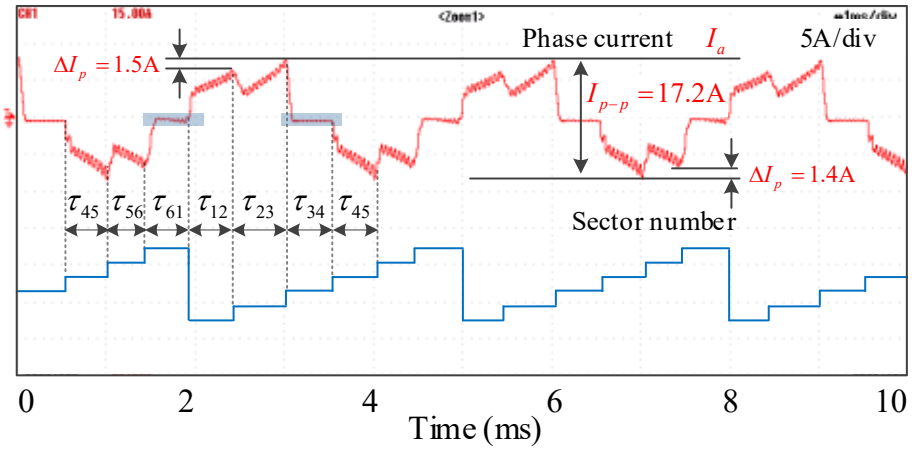
method are shown in Fig. 4.11(a)-(d), respectively. In each figure, the phase current waveform and the sector number are given from the top to the bottom. Besides, the corresponding sector intervals are also presented.



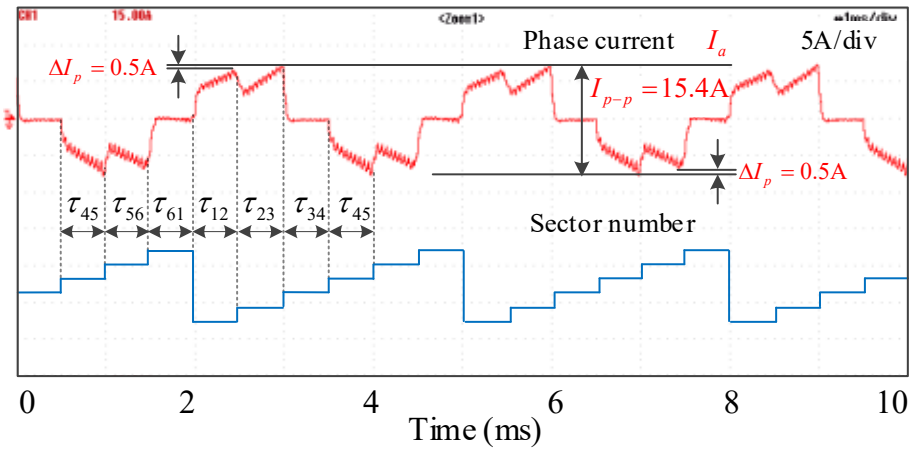
(a) Without compensation.



(b) With uneven Hall signal errors compensation.



(c) With misaligned Hall signal errors compensation.



(d) With the proposed compensation method.

Fig. 4.11. Experimental results of phase currents and sector numbers when motor is operating at $\omega_e = 667\pi$ rad/s ($f_e = 333.3$ Hz) under full load.

The experiment results without using any Hall signal errors compensation method are shown in Fig. 4.11 (a). As can be seen from the results, the phase current is not symmetrical with a P-P value of 16.9A, while the difference between the current peaks is significant. The maximum difference in current peaks is 2.5A. The intervals of different sectors are different from each other. The interval of sector VI, τ_{61}, is much longer than that of sector I, τ_{56}. Besides, due to the existence of uneven Hall signal errors, the phase current under unconducted intervals τ_{61} and τ_{34} has DC offset as marked blue in the figure. Thus, the control performance of the system will be compromised without Hall signal balancing method.

When the uneven Hall signal errors are compensated with the method given in [LEE18], the results are shown in Fig. 4.11 (b). The phase current waveform is still asymmetric. However, since the Hall signals are even at this condition, i.e., each Hall signal has equal high and low state intervals, the sum of any three constructive intervals is 180°. The maximum difference in current peaks is 2A under this condition with the P-P value of phase current is 16.8A.

When only the misaligned Hall signal error is compensated with the method proposed in [ALA12], the experiment results are shown in Fig. 4.11 (c). Similar to the previous results, the sector intervals are different from each other. Besides, since the Hall signals are still uneven while the sum of any three constructive intervals is no longer 180°. For example, the sum of τ_{12}, τ_{23} and τ_{34}, which is the high state of Hall A signal, is longer than that of τ_{45}, τ_{56} and τ_{61}

which is the low state of Hall A signal. The system is still unbalanced with a 1.5A maximum current peak difference. The DC current offset exists due to the uneven Hall errors.

The experiment results with the proposed Hall signal balancing method are shown in Fig. 4.11(d). After the proposed method is employed, the sector intervals become identical. The phase current waveform becomes symmetrical and the P-P value reduces to 15.4A. The phase current under unconducted interval also becomes zero. The maximum difference in current peaks is significantly reduced to around 0.5A by around 80% compared with the non-compensation condition. The overall control performance is thus improved. The performance of the proposed method at different speeds conditions are also tested and found to be similar to the presented one.

In Table 4.3, the six sector intervals τ_{16}~$\tau_{61}$and the maximum current peak difference ΔI_p are compared under four different conditions shown in Fig. 4.11(a)-(d). As can be seen, the proposed method can achieve a minimum current peak difference compared with other conditions. The sector intervals also become almost the same after employing the proposed compensation method. Overall, the effectiveness of the proposed method is verified by experimental results.

TABLE 4.3 Comparison of Measured Control Performance under Different Compensation Method

	Without compensation		With uneven compensation		With misaligned compensation		With proposed compensation	
τ_{12}	52°	-8°	50°	-10°	58°	-2°	59°	-1°
τ_{23}	68°	+8°	56°	-4°	72°	+12°	60°	0
τ_{34}	70°	+10°	74°	+14°	62°	+2°	60°	0
τ_{45}	52°	-8°	51°	-9°	61°	+1°	60°	0
τ_{56}	42°	-18°	55°	-5°	48°	-12°	60°	0
τ_{61}	76°	+16°	74°	+14°	59°	-1°	61°	+1°
ΔI_p	2.5A		2A		1.5A		0.5A	

4.5 Conclusion

Since the relatively complex control algorithms limit application of BLAC drives in high speed drive systems, the BLDC drives are investigated in this thesis. The control performance of Hall sensor based high speed BLDC motor drives depends heavily on the accuracy of Hall sensor signals. In this chapter, a Hall signal balancing method is thus firstly proposed to compensate both the misaligned and uneven Hall signal errors for PM brushless motor under BLDC control. In order to eliminate the PWM update delay, a novel PWM generation scheme is also proposed for high speed BLDC drive with the regenerated balanced Hall signals. With the proposed method, the phase current magnitude, the maximum current peak difference and torque ripple can be reduced. The effectiveness of the proposed method is verified by both simulation and experimental results. The proposed method can be easily implemented for traditional voltage source inverters to achieve a balanced operation of the system.

It should be noticed that for high speed BLDC drive control, even if the Hall signal errors are eliminated, there still exists phase delay error which is caused by the long free-wheeling period. In the next chapter, this problem will be investigated to further improve the performance of the high speed control system.

CHAPTER 5

COMMUTATION ERROR COMPENSATION STRATEGY FOR HIGH SPEED BRUSHLESS DC DRIVES BASED ON D-AXIS CURRENT

In the Chapter 4, the Hall signal error is compensated for the high speed brushless direct current (BLDC) drive to achieve a balanced operation. A new pulse-width modulation (PWM) generation scheme is also proposed to eliminate the PWM update delay. However, even if the system is controlled by balanced Hall signals with zero PWM update delay, there still exists the phase delay error which is caused by the phase angle deviation between the current and the back-electromotive force (EMF), especially under high speed operation. In this chapter, a commutation error compensation strategy for high speed BLDC drives which can eliminate the phase delay error is proposed. The d-axis current is introduced and used as the criterion to determine the phase delay error and generate the phase advance angle. Since the phase currents of BLDC drive contain large amounts of harmonics, which makes the d-axis current hard to detect, a least mean square (LMS) algorithm based adaptive linear neuron (Adaline) filter is proposed. The optimal phase advance angle is adaptively generated by reducing the filtered d-axis current to zero. The proposed method does not need the motor parameter information or additional hardware, and can be implemented in general inverter controllers. The effectiveness of the proposed strategy is verified by both simulation and experimental results.

The major part of this chapter is published on Transactions on Industrial Electronics, and is referred as [WAN20C] in the references.

5.1 Introduction

Permanent magnet (PM) BLDC motors are widely employed for many high speed applications such as compressor, blower and drilling spindle etc. due to high torque density, high efficiency and high reliability [ZWY08][GER14][CRE14]. For a BLDC drive system, six discrete commutation points are usually needed for six-step conduction mode control where the inverter commutates every 60 electrical degrees. However, the commutation errors usually exist which will lead to large torque ripple and low efficiency. Since the PWM update delay has already

been eliminated by the novel PWM generation scheme proposed in the previous chapter, it is not further considered here.

The non-ideal commutation points are mostly caused by two kinds of errors, i.e. the rotor position detection error and the phase delay error. Firstly, the detected rotor position signals through both sensorless control techniques and position sensors are usually not accurate in high speed drives. Various high speed BLDC sensorless control techniques have been investigated, in which the position signals are mostly detected from zero-crossing points (ZCPs) of the back-EMF. However, it should be noticed that the accuracy of detected position signals is compromised by many non-ideal factors, such as armature reaction, asymmetric machine parameters and low pass filter (LPF) of the hardware detection circuit [DAR15][CHE19B]. Besides, the back-EMF based sensorless control techniques does not work well at all speed range, especially during the start-up process. Hall sensors are also widely used in high speed BLDC drive. It has the advantages of simplicity and robustness in wide speed and load range. Thus, in this chapter, Hall sensors are used to obtain the position information. Ideally, three Hall sensors should be mounted 120 electrical degrees apart from each others. Nevertheless, the Hall sensor placement error usually exists in practical conditions which will also lead to unbalanced conduction among the motor phases [ALA08]. Secondly, apart from the rotor position detection error, the phase delay error also exists. For the BLDC drive, the ideal current waveform should be rectangular. However, this is not the case in practice. When the drive switches from one sector to another, the free-wheeling period always exists. For a traditional low-speed BLDC motor, this can usually be neglected because the free-wheeling period of low-speed motor is short. However, under the high-speed condition, the long free-wheeling period will cause the phase current lagging behind the back-EMF [SHI17]. The phase deviation between the current and the back-EMF will also undermine the control performance. In recent years, various commutation compensation methods have been studied. These attempts could be categorized as follows.

Many researches have been focused on improving the accuracy of the detected rotor position signals. In [SHE03], the armature reaction caused rotor position detection error is investigated through finite element analysis method under different conditions. Nevertheless, this method needs motor parameter information. LPFs are commonly used in the ZCPs detection circuit for filtering the PWM noise. In [CUI15B] and [CHE17A], the impact of the LPF is analysed and the rotor position detection error is compensated by modified commutation logic tables. However, the feasibility of these proposed methods depends heavily on the design of the filter

parameters. In [SAM08] and [ALA12], the Hall sensor signals are filtered to generate six balanced commutation signals. However, the rotor position detection error cannot be eliminated since these methods can only lock the commutation points to the one of the three Hall sensors with the minimal placement error. Another Hall sensor placement error compensation method based on the DC current is also proposed in [FAN14]. This method can eliminate the placement error. However, it needs an additional DC current sensor and complex control algorithms. Several other rotor position detection error compensation methods based on DC current [ZHO17A], virtual 3rd harmonic back-EMF [LIU16A] [SON18A], flux linkage function [CHE17B][CHE18B] and current index [LEE16] are also proposed. The effect of asymmetric machine parameters on the position signal detection is analysed and compensated in [AHF10] and [YAN20A] for the BLDC drive. However, the feasibility of the proposed method for high speed drives is not given in [AHF10]. It should also be noticed that although the aforementioned researches could improve the accuracy of the detected rotor position signals, the phase delay error is not considered.

Various researches have also been focused on eliminating the phase delay error in recent years. Phase advance control has been investigated to solve this problem. Since the phase deviation is hard to measure directly, the free-wheeling angle is calculated as the substitute in [PAR17]. However, the calculation is far from accurate and the proposed method still needs DC current and voltage sensors. In [TAN19], the authors propose a phase delay error compensation method according to the phase current and the motor inductance. The drawback of this method is that the motor parameters are hard to obtain accurately. In [LEE18B], a compensation method based on analysing the dynamic model of the motor winding and its Fourier series is proposed. The proposed method needs large computing capability and is hard to implement in high speed drive. The concept of internal power factor (IPF) angle, which is calculated through the PM flux linkage and the integral of phase current, is proposed in [SHI17] and [GUC18] to define the phase delay error. The phase delay error is compensated by reducing the IPF angle to zero through a phase-lock-loop. Since integrators are used in the proposed method, the authors also design a second-order high-pass filter (HPF) to suppress the drift of integrators. In [SON19], the second-order filter is modified to solve the phase deviation problems of the HPF. An additional XOR logic gate hardware is also used to detect the ZCPs of PM flux linkage and the integral of phase current. Although the researches in [SHI17], [GUC18] and [SON19] can obtain satisfied performance, they are all implemented in the three-phase half-bridge inverter with a front-end buck-converter where the pulse-amplitude modulation (PAM) control is used.

For the general inverter that is controlled by PWM, no experimental results are given in these researches. Besides, since the motor parameters are needed to calculate the PM flux linkage, the parameter variation will also undermine the control performance.

In this chapter, a novel commutation compensation strategy for BLDC drives is proposed. Rather than trying to detect the IPF angle, the proposed method compensates the phase delay error by reducing the d-axis current to zero. Since the phase current of BLDC control contains large amounts of harmonics, which makes the d-axis current coupled with harmonics after the coordination transformation, a linear adaptive neuron (Adaline) filter is proposed. The proposed method is motor parameter independent since only phase current is used. It also does not need additional hardware and can be implemented general invertor controllers.

5.2 Commutation Error Analysis of High Speed BLDC Drive System

In order to simplify the analysis, the motor resistance and inductance parameters of three phases are assumed to be identical. The block diagram of a BLDC drive system with general three-phase inverter is shown in Fig. 5.1.

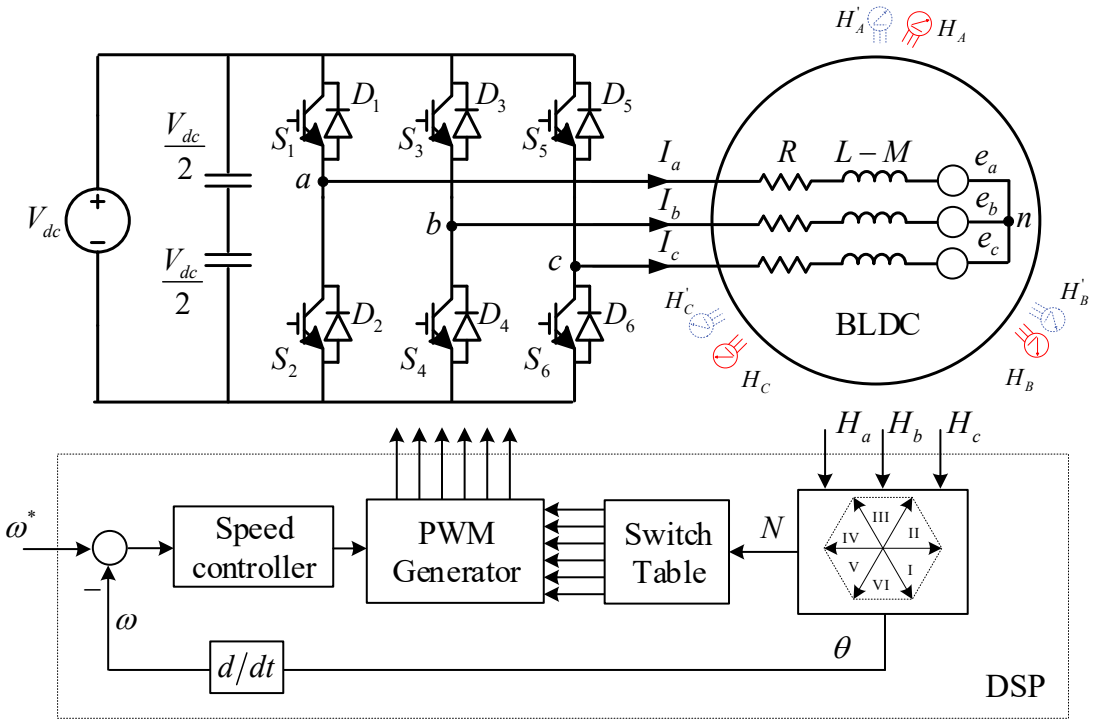


Fig. 5.1. Block diagram of BLDC drive system with Hall sensors.

The Hall sensors are used to detect the rotor position due to low-cost and high-robustness property in wide speed and load range. The voltage equations can be expressed as

$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = R \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + (L - M) \frac{d}{dt} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{5-1}$$

where R is the stator resistance, L and M are the self and mutual winding inductances. $U_{an,bn,cn}$, $I_{a,b,c}$ and $e_{a,b,c}$ are the three-phase supply voltages, phase currents and phase back-EMFs, respectively. The relationships of the Hall signals, the sector number and the drive signals are shown in Table 5.1 and Fig. 5.2.

Table 5.1 RELATIONSHIP OF HALL SIGNALS, SECTOR NUMBER AND DRIVE SIGNALS

$H_aH_bH_c$	Sector number (N)	Drive signals (S_1- S_6)
101	I (A+B-C~)	100100
100	II (A+B~C-)	100001
110	III (A~B+C-)	001001
010	IV (A-B+C~)	011000
011	V (A-B~C+)	010010
001	VI (A~B-C+)	000110

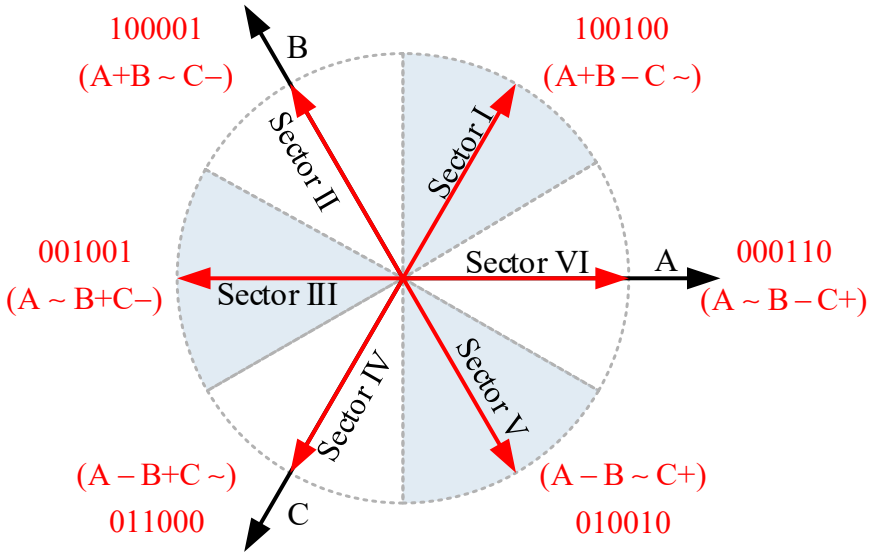


Fig. 5.2. Relationship between the sector number and the drive signals.

5.2.1 Analysis of Hall Sensor Placement Error

It is known that the Hall sensor cannot be placed accurately in the practical conditions [ALA08]. In theory, the Hall sensors should be placed 30 electrical degrees behind the corresponding phase back-EMFs. Under this circumstance, the ZCPs of Hall sensors are the same as the ZCPs of the line-to-line back-EMFs. The ideal and the real positions of Hall sensors are illustrated in Fig. 5.1 as $H'_{A,B,C}$ and $H_{A,B,C}$ respectively. The real of Hall signals and the line-to-line back-EMFs are shown in Fig. 5.3. Based on Table 5.1, the sectors are also divided according to the Hall signals.

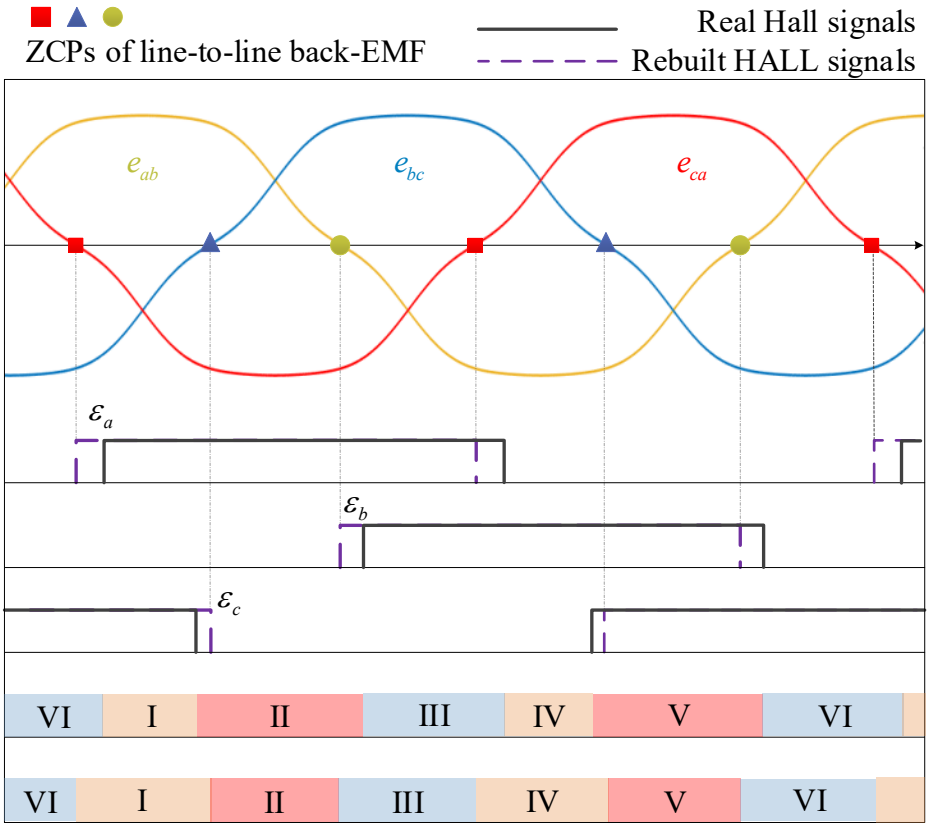


Fig. 5.3. Analysis of Hall sensor placement error.

As shown in Fig. 5.3, the rotor position detection error caused by the Hall sensor misplacement is represented by $\varepsilon_{a,b,c}$. The error $\varepsilon_{a,b,c}$ is only related with the placement accuracy of the Hall sensors [FAN14]. Once the sensor is mounted on the motor, the corresponding Hall sensor placement error is fixed. When the Hall sensor is placed in advance of the ideal position, the error is defined as positive, otherwise, it is negative. Due to the existence of the Hall sensor placement error, the sectors are unevenly divided. Thus, the offline compensation method is

utilized in this chapter. The rebuilt Hall sensor signals $H'_{a,b,c}$ can be expressed according the detected Hall signals $H_{a,b,c}$ and the pre-measured sensor placement error $\varepsilon_{a,b,c}$ as

$$H_{a,b,c}{}' = H_{a,b,c} - \varepsilon_{a,b,c} \tag{5-2}$$

The rebuilt Hall signals and the modified sectors are also shown in Fig. 5.3.

Since the line-to-line back-EMFs depend only on the rotor position and are independent of the position sensors, they can be detected through the stator terminal voltages under open-circuit condition [ALA08]. Then, the Hall sensor placement error $\varepsilon_{a,b,c}$ is relatively easy to obtain offline by comparing the rising and falling edges of Hall signals and the ZCPs of the line-to-line back-EMFs. The offline method is easy to implement and does not require additional DC current and voltage sensors or complex control algorithms. It also has the merit of absolute accuracy and will not cause any position detection error. After obtaining the accurate Hall signals, it is also important to further detect the absolute rotor position signal. Many position estimation algorithms with Hall signals have been proposed in the previous researches, such as the vector tracking observer and the linear extrapolation algorithm [CAP06]. For the vector tracking observer, the absolute position is estimated using a vector tracking phase-lock-loop. Although this kind of method has the advantages of zero-lag tracking capability [KIM11], the performance of observer usually relies on the motor parameters or the mechanical models. The linear extrapolation algorithm, on the other hand, provides an easy way to obtain the absolute position and is thus widely used. Since the algorithm is based on average speed calculation, its performance might suffer from the average speed error problem. However, this kind of problem can be mitigated by choosing high order speed approximation. Thus, in this chapter, the first-order linear extrapolation algorithm is used considering both the control performance and the computation burden. The absolute position signal θ is approximated as [CAP06]

$$\theta = \theta_N + \omega_{0N}(t - t_N) + \frac{\omega_{0N} - \omega_{0(N-1)}}{2\Delta t_{N-1}}(t - t_N)^2 \tag{5-3}$$

where θ_N is the initial angle of sector N, t_N is the instant when rotor enter sector N which can be obtained through the rebuilt Hall signals, Δt_{N-1} is the interval of the previous sector N-1, ω_e is the estimated motor speed which can be expressed as

$$\omega_e = \frac{\pi}{3\Delta t_{N-1}} \tag{5-4}$$

The relationship between the phase back-EMF, the estimated absolute position signal, the detected Hall signals and the rebuilt Hall signals are shown in Fig. 5.4. As shown, by using the first-order linear extrapolation algorithm, the absolute position signal can be generated.

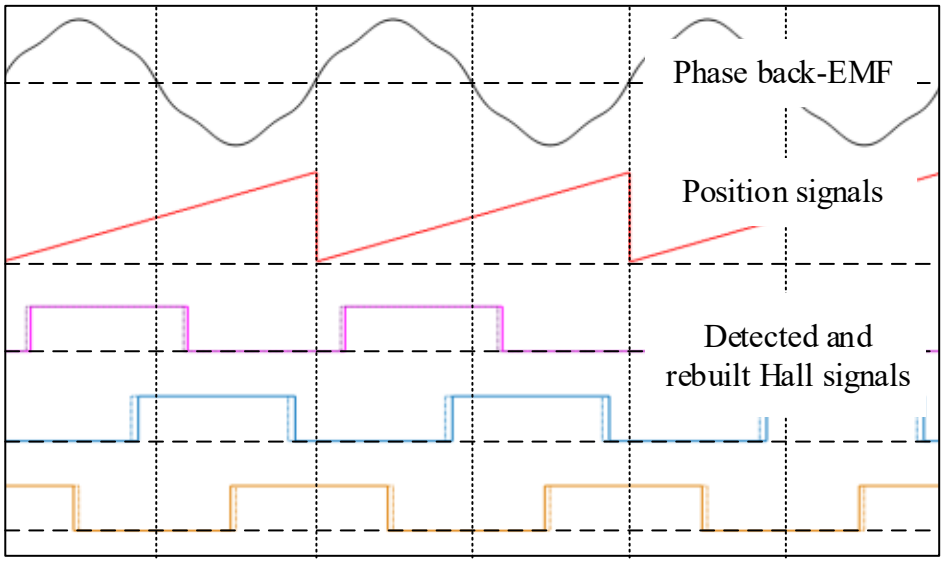


Fig. 5.4. Relationship between the phase back-EMF, the estimated absolute position signal and the Hall signals.

5.2.2 Analysis of Phase Delay Error

Due to the free-wheeling time of BLDC drive caused by the motor inductance, the phase currents and the phase back-EMFs are usually not in phase with each other [GUC18]. Taking phase A for example, the waveforms of phase current I_a and phase back-EMF e_a are shown in Fig. 5.5. The ZCPs of phase A back-EMF occurs in the middle of Sector III and Sector VI as marked. If there exists no phase deviation, the ZCPs of phase current should be the same as the ZCPs of phase back-EMF. For BLDC drive, the fundamental component of phase current is extracted and expressed as I_{a_1}. It can then be used to determine ZCPs of phase current [SON19]. As can be seen, the phase current lags behind the phase back-EMF by ε_{lag}. For BLDC drive, the phase delay error is hard to theoretically calculate. Nevertheless, it is known [SON19][ZHU01] that the phase delay error is related with several factors, such as motor speed ω_e, winding resistance R, winding inductance L_s, and load condition. For some high-speed motors, the phase delay error may be very significant [ZHU01]. In general, this phase delay error can be expressed as

$$\varepsilon_{lag} = f(\omega_e, R, L_s, T, \dots) \tag{5-5}$$

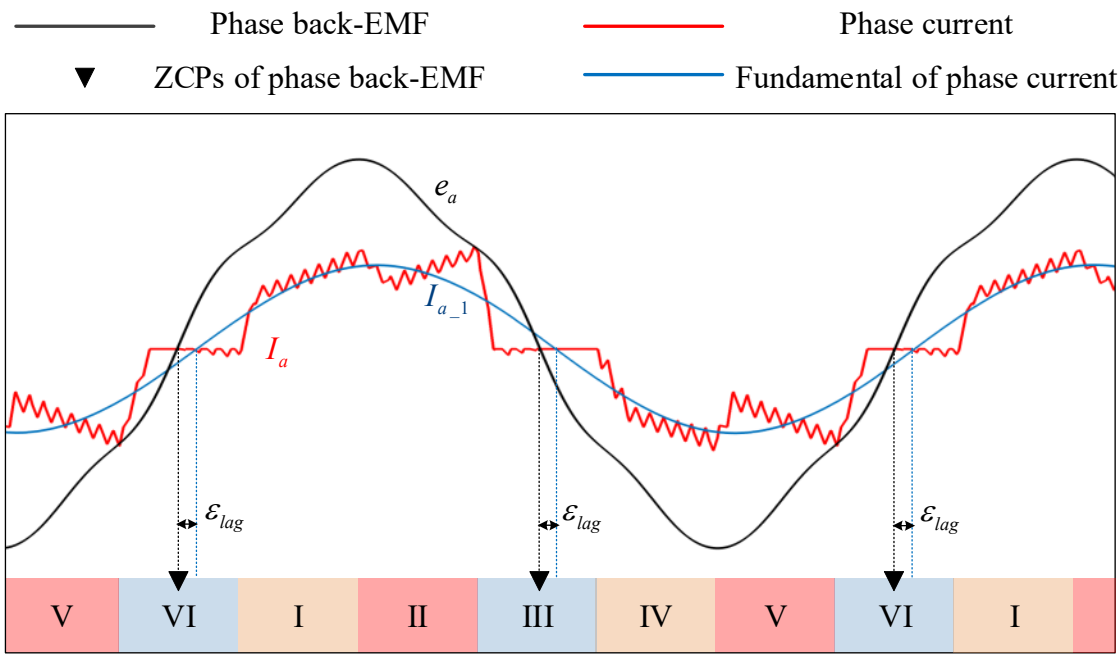


Fig. 5.5. Analysis of phase delay error.

5.3 Proposed Current Harmonics Suppression Method

As shown in the previous analysis, even though the Hall signals are rebuilt, the phase delay error still exists. In this section, a commutation error compensation method is proposed for the BLDC drive system. Rather than detecting or analysing the phase delay angle, the d-axis current is used as the criterion to determine the delay error indirectly. Since the phase current of BLDC drive contains a large amount of harmonics, the d-axis current cannot be directly used after the coordination transformation. An Adaline filter is proposed to extract the fundamental component of the current so that the d-axis current can be obtained through the filtered current signals. A PI controller is then used to generate the compensation signal. Together with the rebuilt Hall signals, a novel communication error compensation method is proposed.

5.3.1 Phase Delay Error Detection

Due to the phase delay error, the commutation error exists even after the Hall placement error is compensated. It should be noticed that the phase delay error is usually hard to obtain theoretically. Thus, in this chapter, we use an indirect way to determine the phase delay error. For the PM motor drive, the space vectors are commonly used for the analysis. In order to obtain these vectors, the coordination transformation is usually needed while the transformation function C_{abc}^{dq} from a-b-c axis frame to d-q axis frame can be expressed as

$$C_{abc}^{dq} = \frac{2}{3}\begin{bmatrix} \cos\omega_e t & \cos(\omega_e t - \frac{2}{3}\pi) & \cos(\omega_e t + \frac{2}{3}\pi) \\ -\sin\omega_e t & -\sin(\omega_e t - \frac{2}{3}\pi) & -\sin(\omega_e t + \frac{2}{3}\pi) \end{bmatrix} \tag{5-6}$$

The space vectors of fundamental current $\vec{\imath}$, back-EMF $\vec{e}$ and supplied voltage $\vec{u}$ for BLDC drive in the synchronous reference frame are shown in Fig. 5.6.

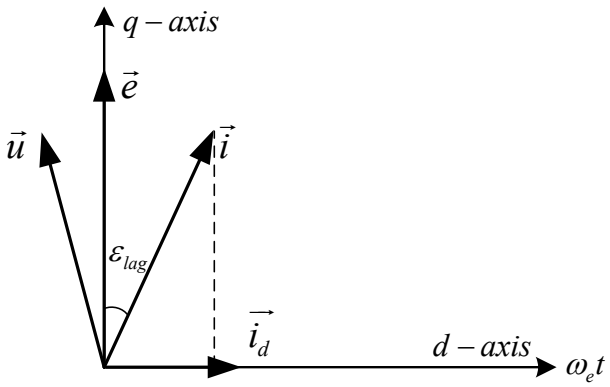


Fig. 5.6. Space vectors in synchronous reference frame.

After the coordination transformation, the phase delay error ε_{lag} is transformed to the deviation between the current vector $\vec{\imath}$ and the back-EMF vector $\vec{e}$ in the synchronous reference frame. Since the position signal is obtained from Hall effect sensors together with the offline compensation method, there will be no position detection error and the d-axis current is accurate. Due to the phase delay error ε_{lag}, the d-axis current vector is no longer zero while the magnitude of the d-axis current can be expressed as

$$i_d = |\vec{\imath}| \sin\varepsilon_{lag} \tag{5-7}$$

where $|\vec{\imath}|$ is the magnitude of the current space vector $\vec{\imath}$. Based on (5-7), it can be seen that the d-axis current is related with the phase delay error ε_{lag}. Thus, it is suitable to use the d-axis current as the criterion to determine the phase delay error. By employing phase advance control, the phase delay error will then be compensated. When the d-axis current is reduced to zero, the phase advance angle could be obtained and the current delay could be eliminated. Nevertheless, it should be noted the phase currents of BLDC control are not sinusoidal and the currents contain a large amount of motor speed related frequency harmonics. Since the Hall placement error has already been compensated, it has no effect on either the fundamental current or the harmonic components.

The phase A current is used as an example and can be expressed as

$$I_a = I_{a1} + I_{an} = -I_1 \sin(\omega_e t - \varepsilon_{lag}) - \sum_{n=5,7,11,13\ldots} I_n \sin n\,(\omega_e t - \delta_n) \tag{5-8}$$

where $I_1$and I_n are the magnitudes of the fundamental and the motor speed related frequency harmonic respectively. δ_n is the phase delay angle of the 5th order harmonic component. The rest two phases can be obtained accordingly. Considering the harmonic components, the d-axis current can be expressed as

$$\begin{aligned} I_d &= C_{abc}^{dq} I_{a1,b1,c1} + C_{abc}^{dq} I_{an,bn,cn} \\ &= I_{d1} + I_{dn} = I_1 \sin(\varepsilon_{lag}) + \sum_{n=5,7,11,13\ldots} I_n \sin[(n \pm 1)\omega_e t - n\delta_n] \\ &+ : n = 5,11,17\ldots \\ &- : n = 7,13,19\ldots \end{aligned} \tag{5-9}$$

As shown in (5-9), the d-axis current is not zero after the coordination transformation. It is composed of a DC-offset which is caused by the phase delay error and the 6th order and its multiple harmonics which are caused by the phase current harmonics. The frequency spectrum of the d-axis current under BLDC control is presented in Fig. 5.7.

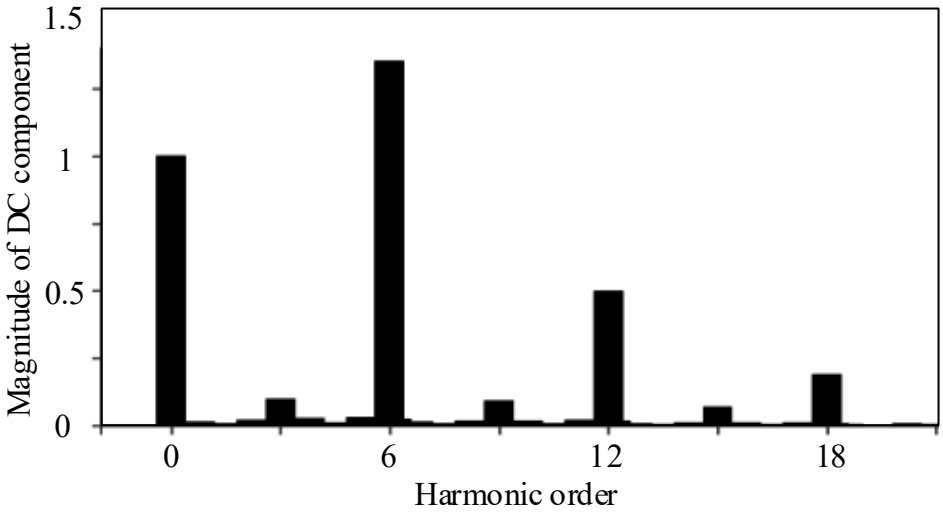


Fig. 5.7. D-axis current spectrum under BLDC control.

As shown in the figure, the main harmonics are the 6th order and the 12th order ones. The magnitude of the harmonics might even be larger than the DC component. Thus, it is essential to extract the fundamental component of the phase current. It should also be noted that the extracted signal should not suffer any phase deviation compared with the original signals. In this chapter, an Adaline filter based on LMS algorithm is used. The structure of the LMS based Adaline filter is shown in Fig. 5.8.

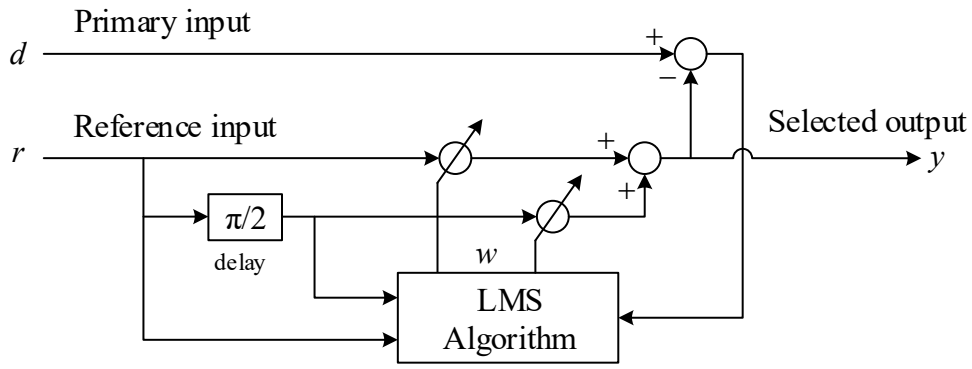


Fig. 5.8. LMS based Adaline filter.

The mathematical model of the Adaline filter [JUN11] output can be expressed as

$$y = \sum_{i=0}^{k} r_i \, w_i \tag{5-10}$$

where r_i are the reference input vectors and w_i are the weight factors of the corresponding vectors. d and y are the primary input and selected output. In this condition, they are the phase current and the fundamental component of the phase current respectively. It is known that the number of input vectors and weight factors of the Adaline should be equal. This number is predefined according to the desired filtering frequency range. In this chapter, since only the fundamental component of the current is needed, the filter needs only to extract one specific frequency, i.e., the fundamental frequency. In order to act as a single-frequency band-pass filter which only lets the fundamental frequency of the phase current pass, two speed-related reference input vectors are needed, and they are expressed as

$$r_1 = cos(\omega_e t) \qquad r_2 = sin(\omega_e t) \tag{5-11}$$

Then, the corresponding weight factors can be defined as w_{cos} and w_{sin}. The filter is employed in the discrete system where the sampling time is set as T_s. The nth sample point of reference input vectors r^n and weight factors w^n can be expressed as

$$r^n = [cos(\omega_e t^n) \quad sin(\omega_e t^n)]$$
$$w^n = [w_{cos}^n \quad w_{sin}^n] \tag{5-12}$$

where

$$t^n = nT_s \tag{5-13}$$

The selected output is calculated based on the input vectors and weight factors as

$$y = r_1 w_1 + r_2 w_2 \tag{5-14}$$

Then, the selected output at the nth sample point can be written in vector format as

$$y^n = r^n (w^n)^T \tag{5-15}$$

The weight factors w^n are adaptively changed so that the output y^n could be the same as the fundamental frequency of the primary input d^n at the n[th] sample point. The error between d^n and y^n at the nth sample point is defined as

$$e^n = d^n - r^n (w^n)^T \tag{5-16}$$

Then, the LMS algorithm is used for adaptive learning of weight factor. The goal of the adaptive learning is to make the predefined error criterion achieve the minimum value so that each vector of the linear neuron network is approaching the learning object. A commonly used half-squared-error criterion function [LIU11] J^n can be expressed as

$$J^n = \frac{1}{2}(e^n)^2 = \frac{1}{2}(d^n - r^n (w^n)^T)^2 \tag{5-17}$$

The frequency of reference input signal is obtained based on the motor speed. The weight factor, which minimizes the criterion function J^n can be found by applying the gradient descent procedure. The gradient of J^n with respect to w^n, denoted by $\nabla J^n(w^n)$ can be expressed as

$$\nabla J^n(w^n) = -(d^n - r^n (w^n)^T) r^n = -e^n r^n \tag{5-18}$$

It is known that the criterion function will decrease if the weight factors are updated in the reverse direction of the gradient. Thus, the weight factor updating rule is then given as

$$w^n = w^{n-1} - 2\eta \nabla J^n(w^n) \tag{5-19}$$

$$= w^{n-1} + 2\eta e^n r^n$$

where η is the learning rate of the LMS based Adaline filter. Then, the transfer function $G(z)$ from d to y in z-domain can be expressed

$$G(z) = \frac{y}{d} = \frac{y}{y+e} = \frac{2\eta(z\cos\omega_e T_s - 1)}{z^2 - 2(1-\eta)z\cos\omega_e T_s + 1 - 2\eta} \tag{5-20}$$

It should be noticed that the Adaline filter acts similar to a resonance controller based selective frequency signal extractor. The transfer function of a resonant controller can be expressed as [ZHO18B]

$$G_R(s) = \frac{K_R s}{s^2 + {\omega_R}^2} \tag{5-21}$$

where K_R and ω_R are the resonant coefficient and resonant frequency. However, the ideal resonant digital controller is hard to be digital implemented in practice where the discretization process is required. Due to its properties such as the narrow band and infinite gain, the resonant controller is very sensitive to the discretization process. Different discretization methods, such as zero-order hold method, forward Euler method and zero-pole matching method, are compared in [YEP10]. It is shown that the choose of the discretization method is crucial for application performance. The Adaline filter, on the other hand, is easy to be digital implemented in the discrete system as presented in this chapter.

The Bode diagram of the proposed LMS based Adaline filter for $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) with different learning rates η is shown in Fig. 5.9. As shown in the figure, the Adaline filter can successfully let the selected frequency signals pass without phase deviation or magnitude attenuation. The learning rate η is important to the control system. However, there is a trade-off between the filter pass band and the learning speed when choosing the learning rate η. When the learning rate is chosen small, the pass band becomes narrower at the cost of slow learning speed. On the other hand, the pass band becomes wider with the increase of learning rate. In order to solve this, the recursive least-square (RLS) algorithms which online updates the Adaline filter learning rate is proposed [ZHA16]. However, the RLS based method requires more computations compared with LMS based method. For the high speed control, the computation resources are limited and thus the LMS based method are chosen. In practice, the learning rate is selected according to the practical conditions. In this chapter, the learning rate η is selected as 0.005.

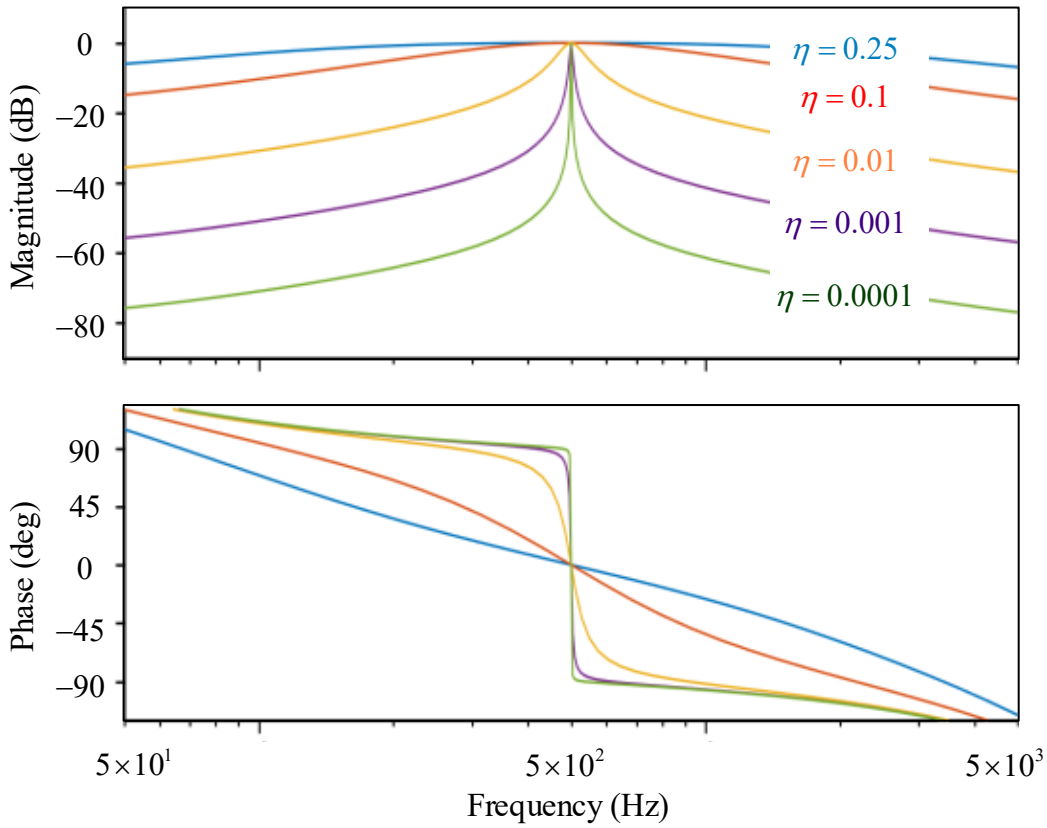
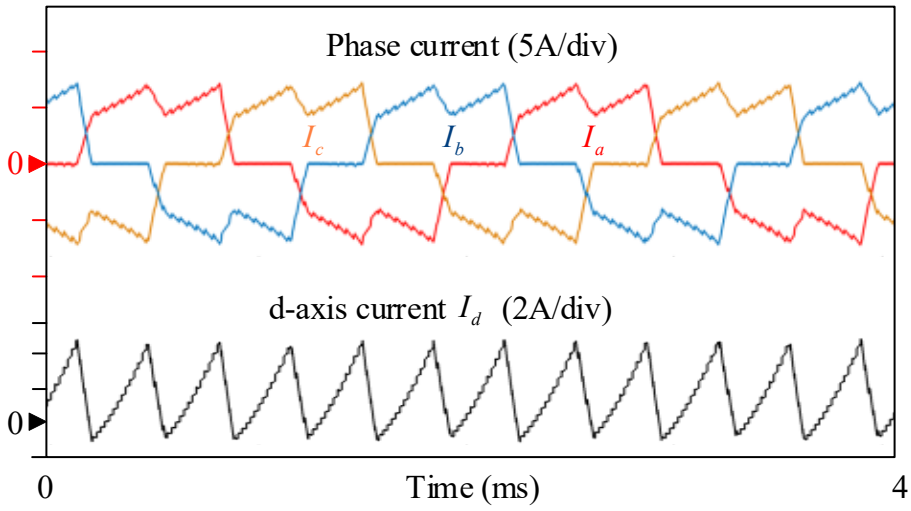
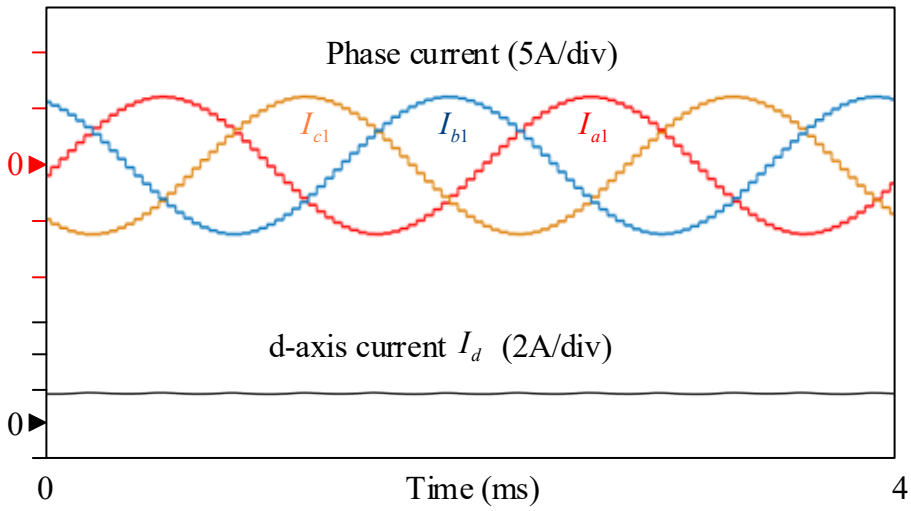


Fig. 5.9. Bode diagram of the LMS based Adaline filter.

The three phase current and the d-axis current waveforms before and after employing the Adaline filter are shown in Fig. 5.10. The motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz). As can be seen, the proposed LMS based Adaline filter can successfully extract the fundamental phase current. The d-axis current after employing the Adaline filter suffers no current harmonics.



(a) Simulation current waveforms before employing Adaline filter.



(b) Simulation current waveforms after employing Adaline filter.

Fig. 5.10. Three phase current and the d-axis current waveforms before and after employing Adaline filter.

Taking phase A current for example, the evolution of the Adaline weight factors during the learning process is shown in Fig. 5.11.

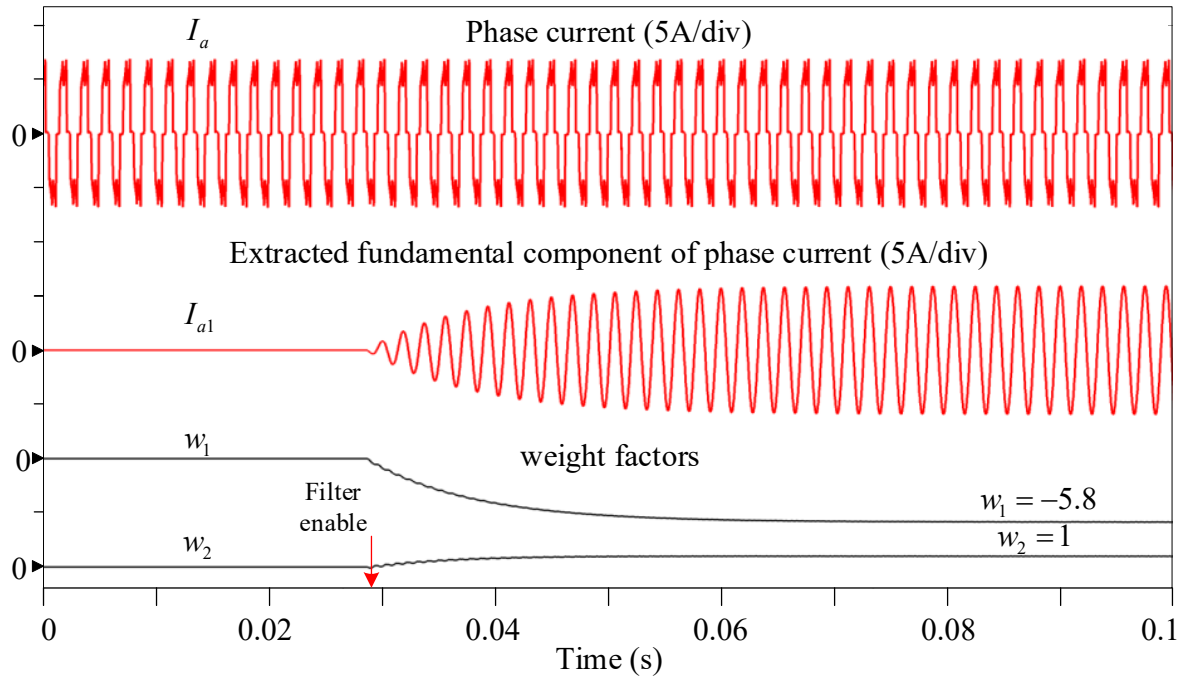


Fig. 5.11. Evolution of the Adaline weight factors during the learning process.

From the top to the bottom, the phase current I_a, the extracted fundamental component of the phase current I_{a1} and the two weight factors $w_1 w_2$ are presented accordingly. To be consistent

with the previous analysis, the frequency of the phase current is still set to be 500 Hz. As shown in the figure, the weight factors can adaptively update to approach the learning object. The fundamental component of the phase current can be extracted with the proposed LMS based Adaline filter.

5.3.2 Compensation Method

As shown in the previous section, the Adaline filter can extract the fundamental component of the phase current signals without suffering any phase deviation. Thus, in the proposed method, the three phase currents $I_{a,b,c}$ are firstly processed by the LMS based Adaline filter proposed in Fig. 5.8. After obtaining the fundamental components $I_{a1,b1,c1}$, the processed phase current signals are transferred from the stationary reference frame into the synchronous reference frame. After obtaining the d-axis current, it is used to determine the proper phase advance angle so that the phase delay error can be eliminated. A proportional–integral (PI) controller is employed to generate the proper phase advance angle θ_{adv}. The block diagram of the proposed phase delay error compensation method is shown in Fig. 5.12.

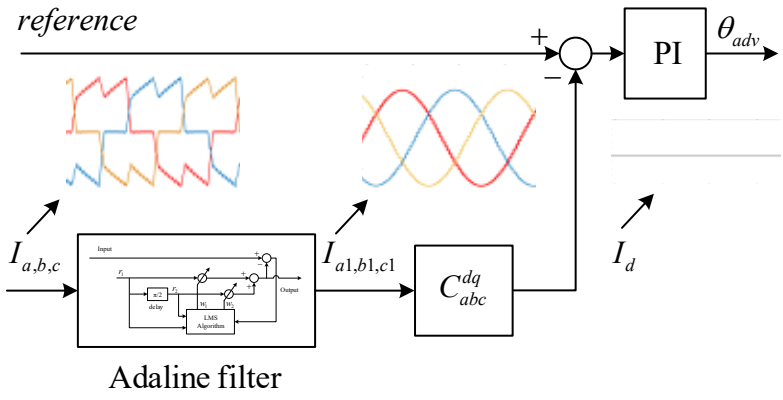


Fig. 5.12. Block diagram of the proposed phase delay error compensation method.

The Hall sensor placement error is eliminated according to (5-2). The rebuilt Hall signals are then used to determine the absolute position according to (5-3). The phase advance angle θ_{adv} and the rebuilt Hall signals are used together to generate the proper drive signals. The block diagram of BLDC drive system with proposed commutation error compensation method is shown in Fig. 5.13. It should be noted that since the fundamental currents are used to be aligned with the back-EMFs, the proposed method would be better suited for the motor with almost sinusoidal back-EMF waveform. For high speed motors, it is desirable to have more sinusoidal airgap field distribution and back-EMF waveform in order to reduce the iron losses [GUC18].

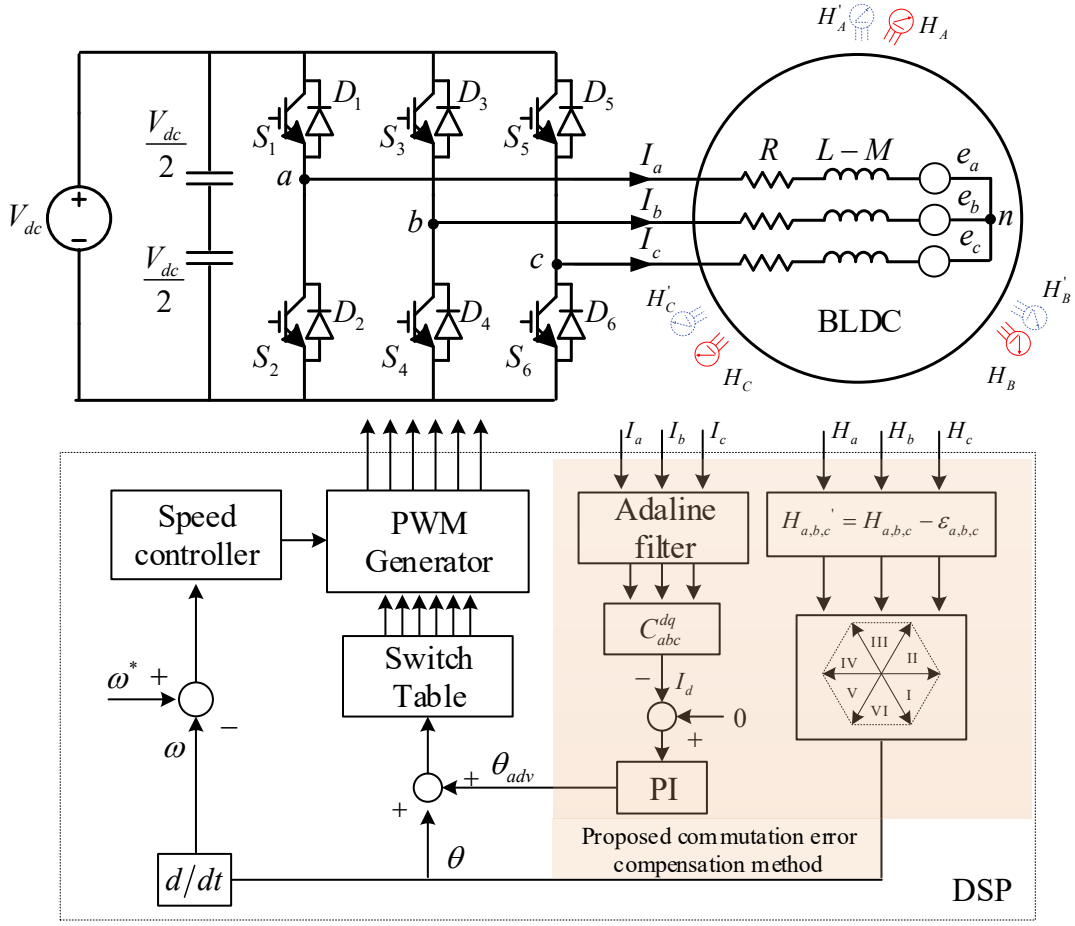


Fig. 5.13. Block diagram of BLDC drive system with proposed commutation error compensation method.

5.3.3 Simulation Verification

To verify the effectiveness of the proposed commutation compensation method, a simulation model is built in MATLAB/Simulink. The sampling period T_s is set to 50 μs while the switch frequency is set to 20 kHz.

The simulation results before and after the compensation when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) under full load (0.3Nm) Fig. 5.14. The phase current, the fundamental component of the phase current, the d- axis current and the phase advance angle are shown from the top to the bottom. The compensation is enabled at 0.3s while the results before and after the compensation are given in Zoom 1 and Zoom 2 respectively.

As shown in Fig. 5.14, the fundamental component of the phase current can be obtained with the proposed LMS based Adaline filter. The corresponding d-axis does not suffer from the coupled harmonics problem, making it able to be used for the compensation process. Before

the compensation is enabled, the d-axis current 0.9A. The phase current is delayed behind the corresponding back-EMF. After the compensation is enabled, the phase advance angle increases gradually while the d-axis current is reduced to zero. The peak-to-peak value of the phase current declines from 14.2A to 13.1A by 8%. The control performance is improved after the proposed compensation method is employed.

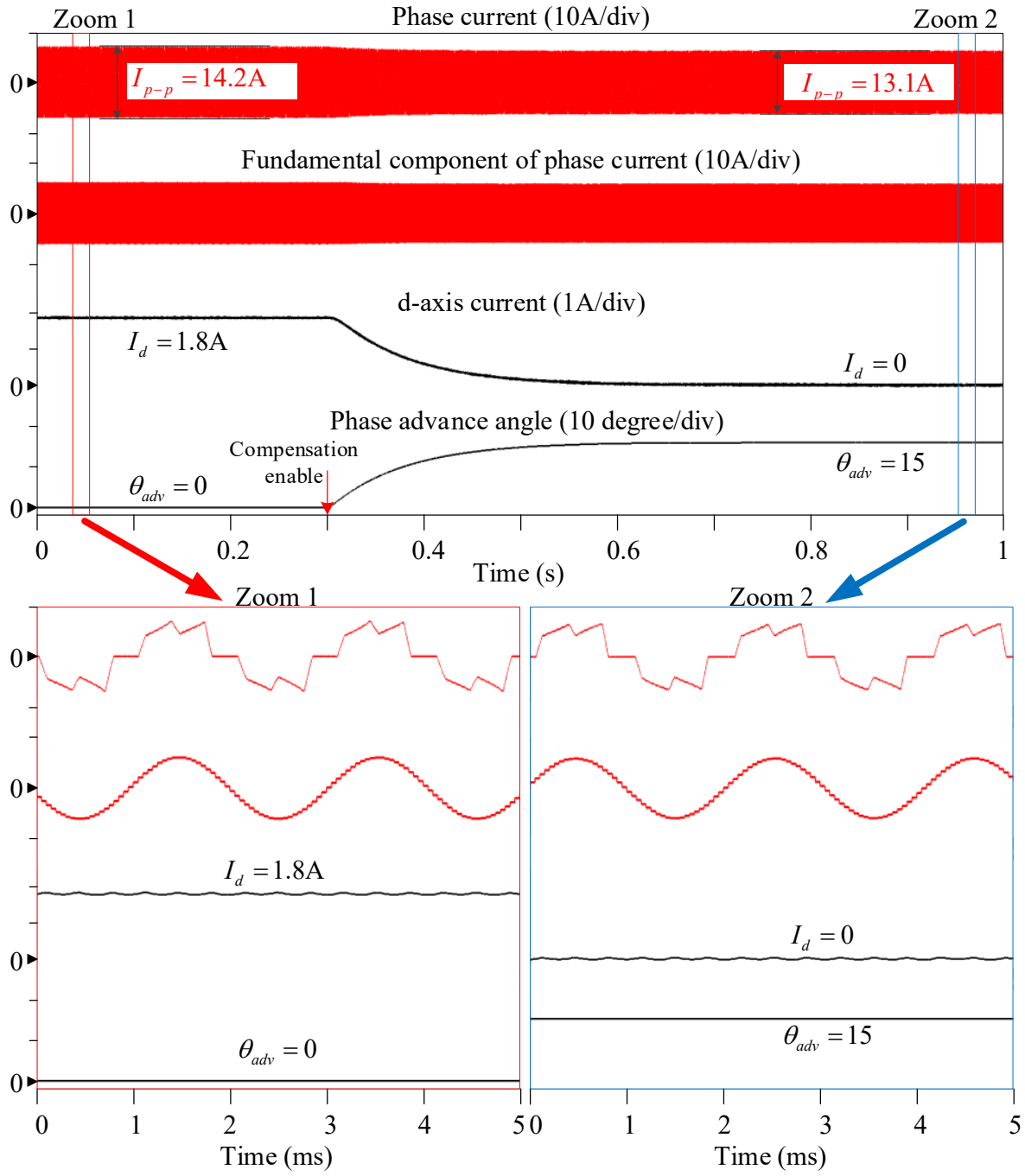


Fig. 5.14. Simulation results before and after compensation when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) under full load.

The simulation results of detected and compensated commutation points with the proposed compensation method when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) under full load are shown in Fig. 5.15. The detected commutation points which are generated by detected Hall signals are marked in solid line. With the proposed commutation compensation method, the commutation points are corrected by the phase advance angle θ_{adv} so that the commutation error can be eliminated. The compensated commutation points are marked in dash line. Overall, the effectiveness of the proposed commutation error compensation method is verified through simulation results.

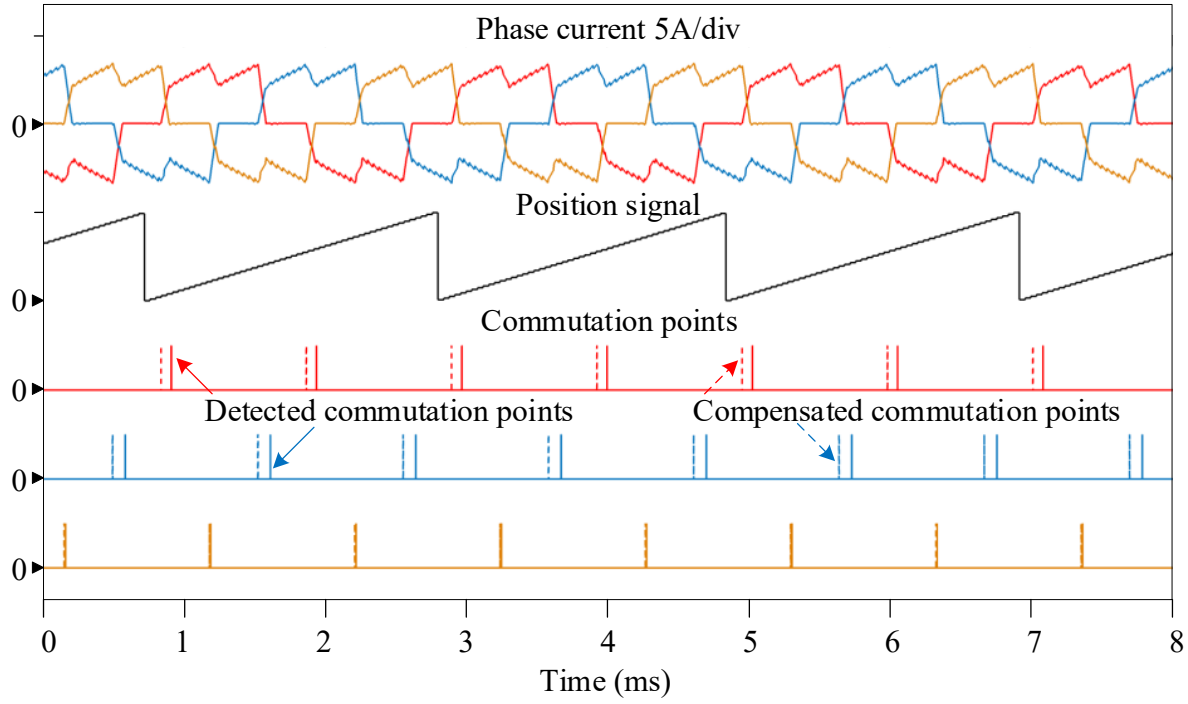
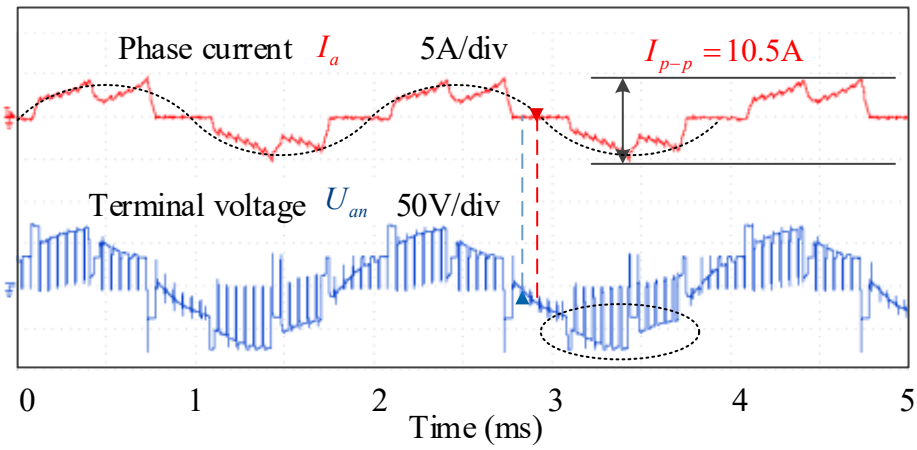


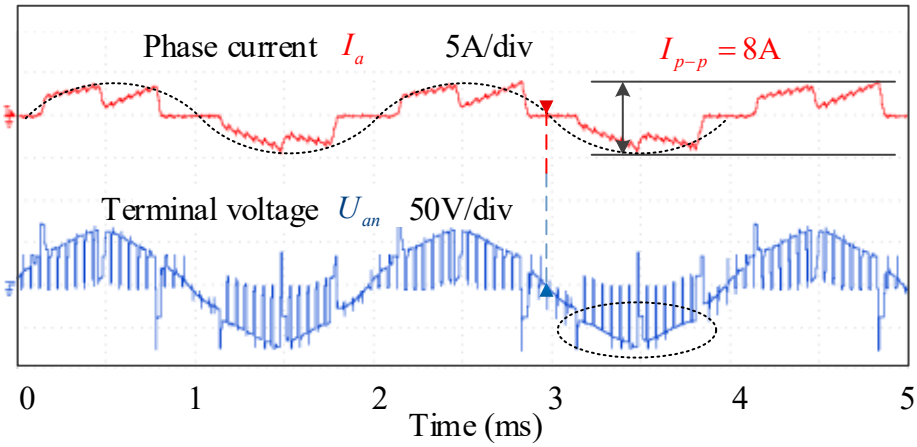
Fig. 5.15. Simulation detected and compensated commutation points with the proposed compensation method when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) under full load.

5.4 Experimental Evaluation

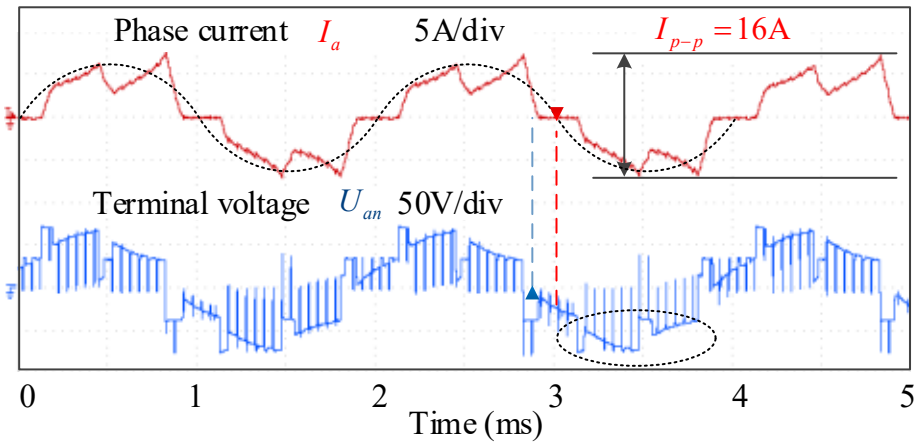
The test rig setup is presented in the Appendix. In order to verify the effectiveness of the proposed method, various experiments are taken under different conditions. The experimental results of the proposed commutation errors compensation method at steady state when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) are given in Fig. 5.16.



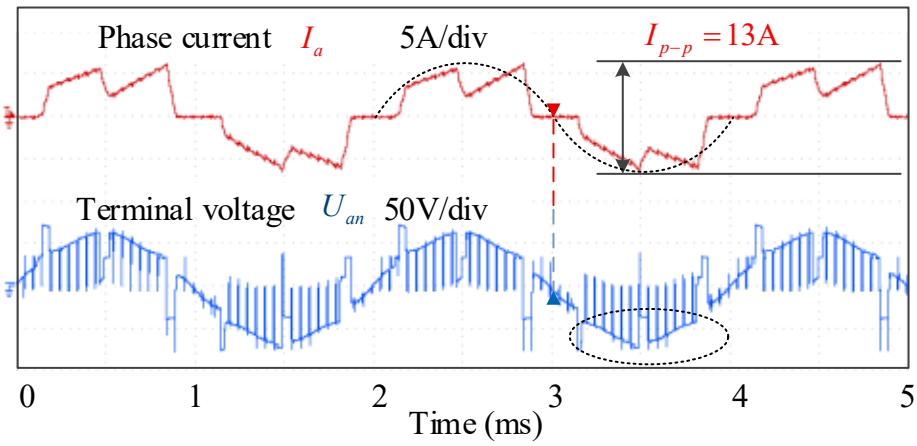
(a) Light load without compensation.



(b) Light load with compensation.



(c) Full load without compensation.



(d) Full load with compensation.

Fig. 5.16. Experimental results of phase current and phase terminal voltage when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz)

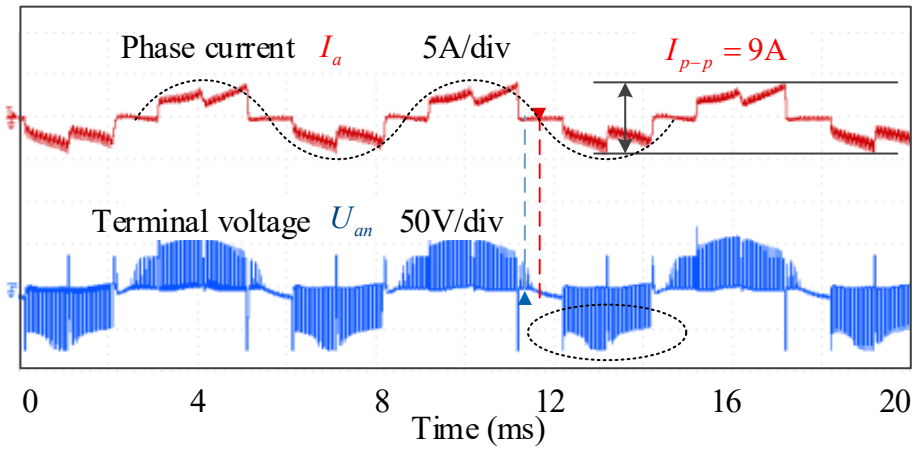
It is known that the back-EMF waveforms cannot be obtained during the operation, thus, the phase terminal voltages are used instead to monitor the phase delay error since phase terminal voltages are the same as the back-EMF when the corresponding phase are floated. Fig. 5.16 (a) and Fig. 5.16 (b) show phase current and phase terminal voltage without and with the proposed compensation method under light load while the results under full load are given Fig. 5.16 (c) and Fig. 5.16 (d) respectively.

In order to illustrate the commutation errors, the ZCPs of the phase terminal voltage and the fundamental component of the phase current are marked in the figures. As shown in Fig. 5.16 (a) and Fig. 5.16 (c), without proposed compensation, the phase current lags behind the phase terminal voltage. With the increase of the motor load, the commutation error becomes more obvious. The peak-to-peak values of the phase current are 10.5A and 16A under light and rated load. When the proposed commutation error compensation method is enabled, the commutation errors are eliminated as shown in Fig. 5.16 (b) and Fig. 5.16 (d). The phase current is then in the same phase as the phase terminal voltage.

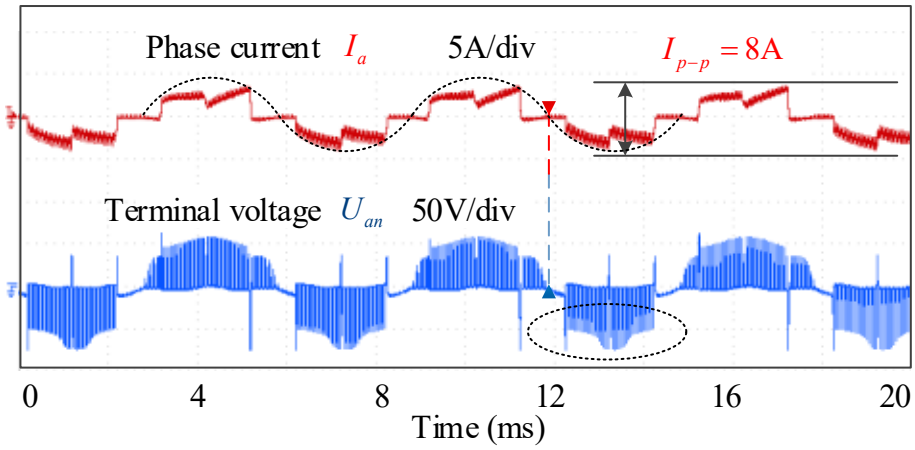
The terminal voltage is used as an indirect way to illustrate the commutation errors. The commutation error compensation can also be seen according to free-wheeling period as marked with dashed circle in figures. When no commutation error compensation method is used, the terminal voltages is asymmetric due to the commutation errors. With the proposed compensation method, free-wheeling period happens in the middle of the phase terminal

voltage. After the compensation, the peak-to-peak values of the phase current reduce to 8A and 13A under light and rated load. The control performance is improved.

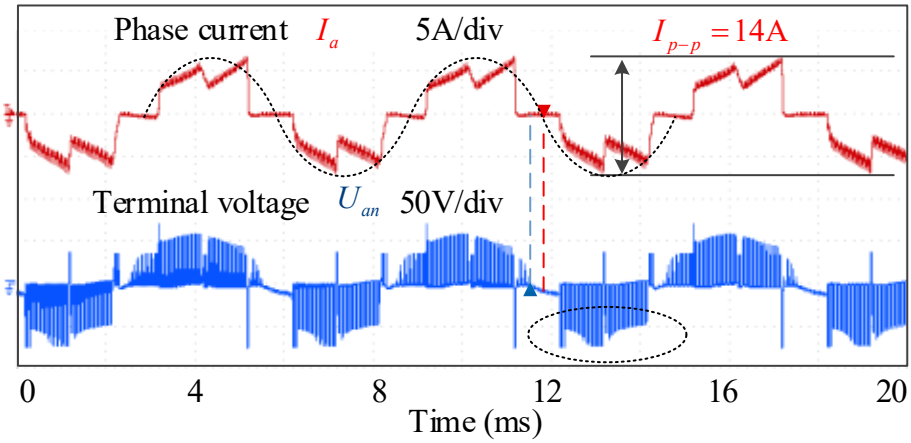
The experimental results of the proposed commutation errors compensation method at steady state when motor is operating at $\omega_e = 333.3\pi$ rad/s ($f_e = 166.7$ Hz) are given in Fig. 5.17. With the proposed compensation method, the terminal voltage becomes more symmetrical as marked with dashed circle. Under light load condition, the proposed compensation method reduces peak-to-peak current from 9A to 8A by 11%. Under rated load, the peak-to-peak current is reduced from 14A to 12.5A.



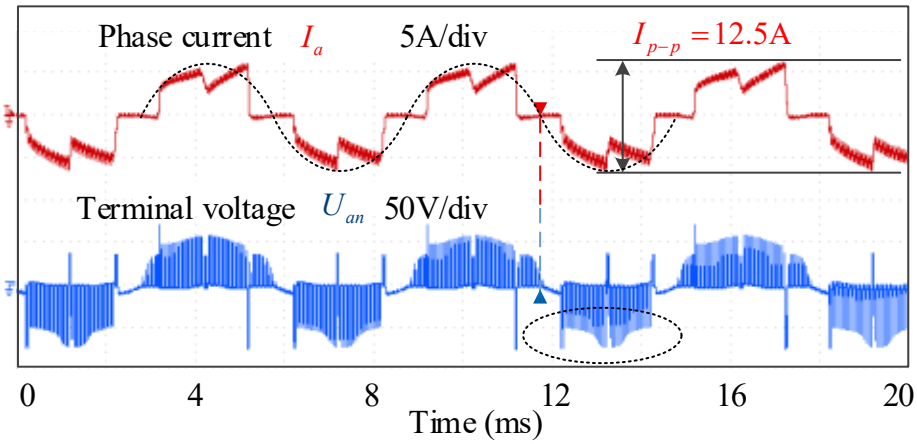
(a) Light load without compensation.



(b) Light load with compensation.



(c) Full load without compensation.



(d) Full load with compensation.

Fig. 5.17. Experimental results of phase current and phase terminal voltage when motor is operating at $\omega_e = 333.3\pi$ rad/s ($f_e = 166.7$ Hz)

The results of the peak-to-peak current under steady state at when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) are shown in Fig. 5.18 under different load conditions with and without the proposed compensation method. As can be seen from the figure, the peak-to-peak current increases with the increase of load. Under heavy loads, the commutation error problem becomes more severe if no compensation method is employed. Once the proposed compensation method is employed, the peak-to-peak current will largely reduce compared with the no compensation conditions. Overall, the test results verify the effectiveness of the proposed commutation errors compensation method under different speed and load conditions.

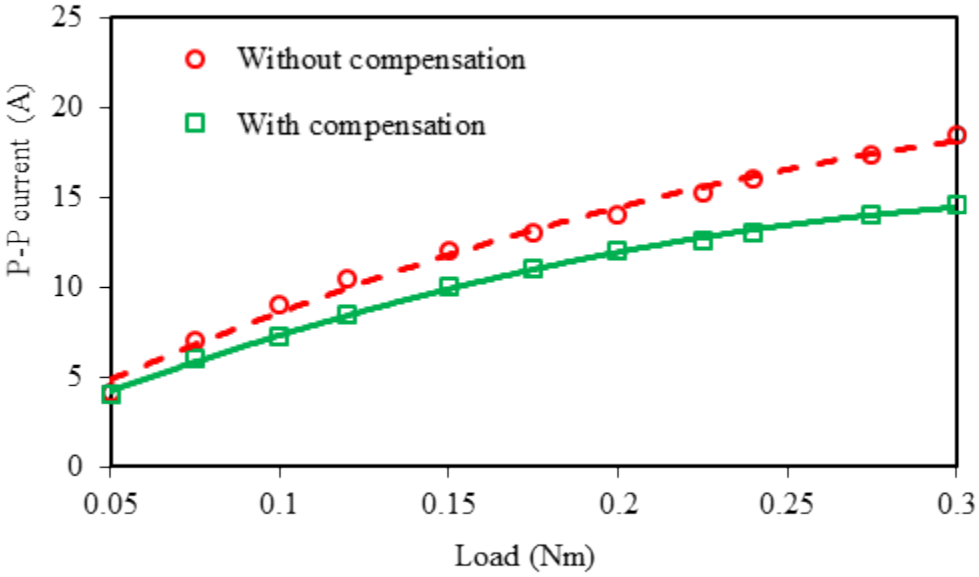
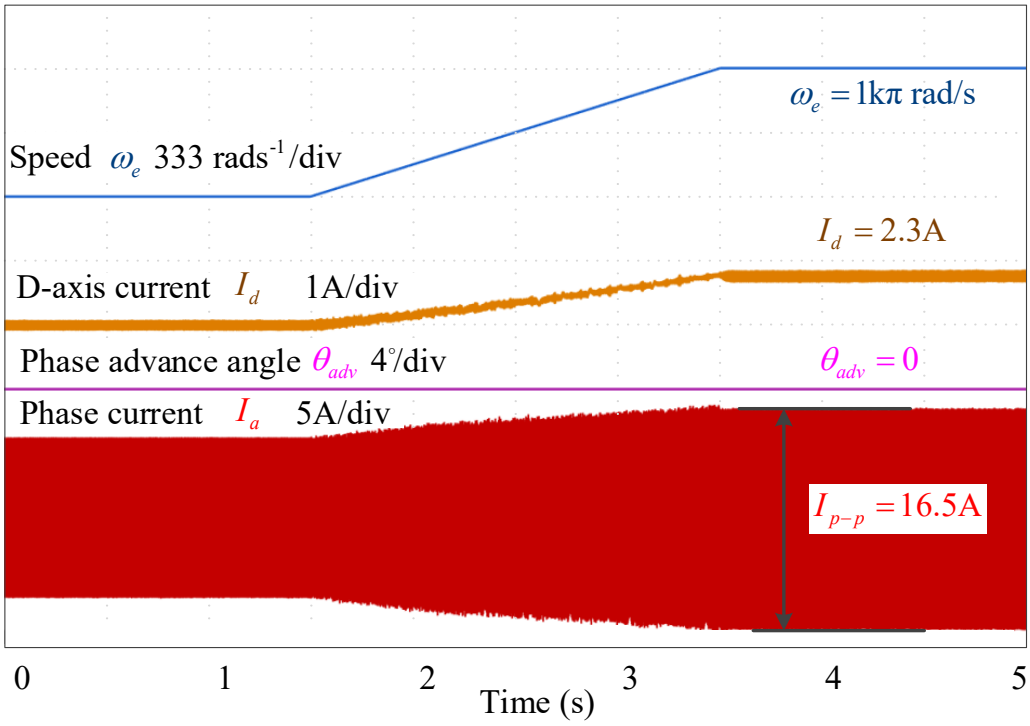


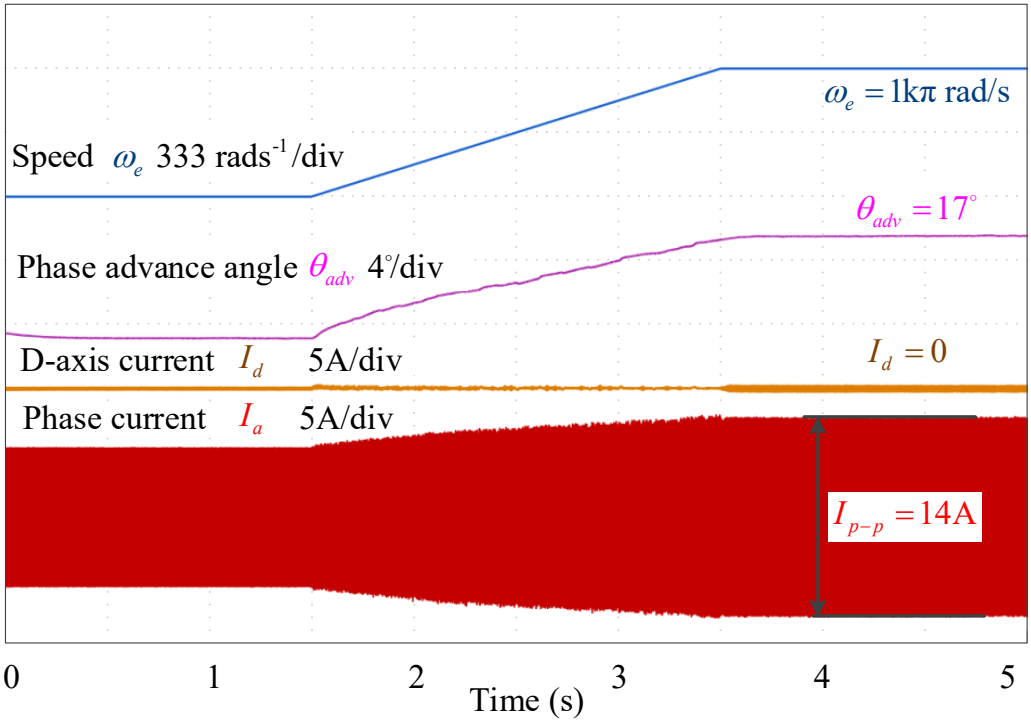
Fig. 5.18. Peak-to-peak current under different loads with and without compensation when motor is operating at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz).

Apart from the steady state test, the results without and with the proposed commutation error compensation method during the transient state are presented in Fig. 5.19(a) and Fig. 5.19(b), respectively. The speed of the motor increases gradually from $\omega_e = 333.3\pi$ rad/s ($f_e = 166.7$ Hz) to $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz). The motor speed, the phase advance angle generated by the commutation compensation method, the d-axis current and the phase current are given in the figure accordingly.

When the commutation compensation is not used, the d-axis current increases with the increase of the speed as shown in Fig. 5.19(a). When the commutation compensation is used, the proposed method can automatically change the proper phase advance angle with the change of speed. With the increase of speed, the phase advance angle increases from 11° to 17° as shown in Fig. 5.19(b) so that the phase currents are still in the same phase with the phase back-EMFs. With the proposed commutation error compensation method, the peak-to-peak current also reduces during the transient state. The experimental results prove the effectiveness of the proposed compensation method during the transient state.



(a) Without compensation.



(b) With compensation.

Fig. 5.19. Experimental results during the transient state.

5.5 Conclusion

In this chapter, a novel commutation compensation strategy for high speed BLDC drives is proposed in order compensate the phase delay error. The d-axis current is chosen as the criterion to determine the commutation errors and then used to generate the proper compensation signal. Since the phase current of BLDC control contains a large amount of harmonics, which makes the d-axis current coupled with harmonics after the coordination transformation, a LMS based Adaline filter is proposed to extract the d-axis current from the harmonics. The extracted d-axis current is then used to generate the phase advance angle for eliminating the commutation error. The proposed method does not depend on the motor parameters. It also does not need additional hardware and can be implemented in general inverter controllers. The effectiveness of this method is verified through both simulation and experimental results.

It should be noticed that since the d-axis current is used for the phase delay error elimination, the precise position signal is vital for the overall control performance. In this chapter, the absolute position is obtained through the Hall signals together with the offline measured Hall signal errors. In the next chapter, a phase delay error compensation method based on the stator current will be investigated so that the absolute position is no longer needed and the control complexity can be reduced.

CHAPTER 6

COMMUTATION ERROR COMPENSATION STRATEGY FOR HIGH SPEED BRUSHLESS DC 150-TSC DRIVES BASED ON STATOR CURRENT

In Chapter 5, a commutation error compensation strategy for high speed brushless DC (BLDC) drives based on the d-axis current is proposed. Although the proposed method can successfully eliminate the phase delay error, a continuous absolute position signal is still needed in order to implement the coordinate transformation. Besides, the traditional 120° mode six-step control (120-SSC) strategy is used which results in large current harmonics. In this chapter, the 150° mode twelve-step control (150-TSC) is adopted for high speed BLDC drives since it can generate a quasi-sinusoidal current waveform. An online commutation error compensation method is also proposed for the high speed BLDC 150-TSC drive which utilizes the stator current as the criterion. The optimal phase advance angle is generated when the stator current magnitude is reduced to the minimum value with the help of the gradient descent optimization (GDO) algorithm. No continuous absolute position signal or motor parameter information is needed for the proposed commutation optimization method. The effectiveness of the proposed strategy is verified by simulation results.

6.1 Introduction

Permanent magnet (PM) brushless motors are widely employed for many high speed applications due to their robust structure and high performance [ZWY08] [CUI15B] [CRE14]. Traditionally, for a brushless DC (BLDC) drive system, the 120-SSC strategy is usually used where inverter commutates every 60 electrical degrees. However, it is known that the traditional 120-SSC will generate rectangular phase currents which contain large current harmonics. Besides, for high speed motors, it is desirable to have a sinusoidal airgap field distribution and back-EMF waveform in order to reduce the iron losses [BER15]. Thus, a large torque ripple will be produced due to sinusoidal back-EMF and rectangular current which deteriorates the system control performance.

In recent years, the concept of wide angle BLDC controls, which helps to generate a quasi-sinusoidal current waveform, is proposed. Rather than fixing the conducting angle of each phase at 120 electrical degrees, this kind of methods extends the conducting angle in order to improve the control performance. Unlike the 120-SSC which has only one conducting mode, i.e., two-phase-conducting and one-phase floating mode (Mode I), the wide angle controls are twelve-step control (TSC) strategies that have two conducting modes. Between each step, the system switches from Mode I to three-phase-conducting mode (Mode II) periodically. This kind of method is firstly proposed in [SAH01] where the authors adjust the conducting angle from 120 to 170 electrical degrees. The authors conclude that the 150-TSC and the 165° mode TSC have the most predominant effect on making the current waveform near sinusoidal and they can suppress the 5^{th} order current harmonics by more than 50%. The motor vibration is also much reduced by the wide angle control. In [NOG15], the authors introduce an efficiency measuring procedure and compare the efficiency of different wide angle BLDC control methods. The authors point out that the 150-TSC has the highest efficiency. It should be noticed that only the 150-TSC could achieve symmetrical control among all wide angle BLDC control methods [WAN07]. Besides, with the increasing of the conducting angle, the zero-crossing-point of the back-EMF becomes harder to be detected. Thus, the 150-TSC is considered to be able to achieve the best overall control performance among the wide angle BLDC control methods and is used in this chapter. In [KIM15] [PRO13] [KAN11], different torque ripple suppression methods are employed to the 150-TSC. An adaptive 150-TSC also is proposed in [CHE09] to limit the rising slope of current during the commutation period so that the torque ripple produced by the free-wheeling current can be reduced. However, the existing researches focus mainly on the implementation of 150-TSC strategies. The commutation errors and the optimal stator current angle are rarely considered.

Similar to the BLDC 120-SSC strategies, the commutation errors also exist in the BLDC 150-TSC. Since commutation error problem of BLDC drives has already been discussed in the previous chapter, it is not further presented. In Chapter 5, a commutation error compensation method which uses the d-axis current to determine the phase delay error is proposed. When the d-axis current is reduced to zero, the phase delay error could be eliminated. Although the proposed method provides good results and can be implemented in general inverter controllers, the continuous absolute position signal is needed. In this chapter, an online commutation error compensation strategy for high speed BLDC 150-TSC drives is proposed. The proposed method eliminates the commutation errors by minimizing the stator current magnitude. The

gradient descent optimization (GDO) algorithm is utilized to determine the phase advance angle for minimum current magnitude. A linear adaptive neuron (Adaline) filter is still used to extract the fundamental component of phase current, so that the stator current does not suffer from harmonic problems. The proposed method does not require continuous absolute position signal and does not depend on motor parameter information or additional hardware. The proposed method can be implemented in general inverter controllers. Its effectiveness is verified by simulation results.

6.2 Commutation Error Analysis of High Speed 150-TSC BLDC Drive System

6.2.1 150-TSC BLDC Drive System

The three phase motor resistance and inductance parameters are assumed to be the same in order to simplify the analysis. The Hall sensors are used to detect the rotor position due to low-cost and high-robustness property in the wide speed and load range. The block diagram of a 150-TSC BLDC drive system with a general three-phase inverter is shown in Fig. 6.1.

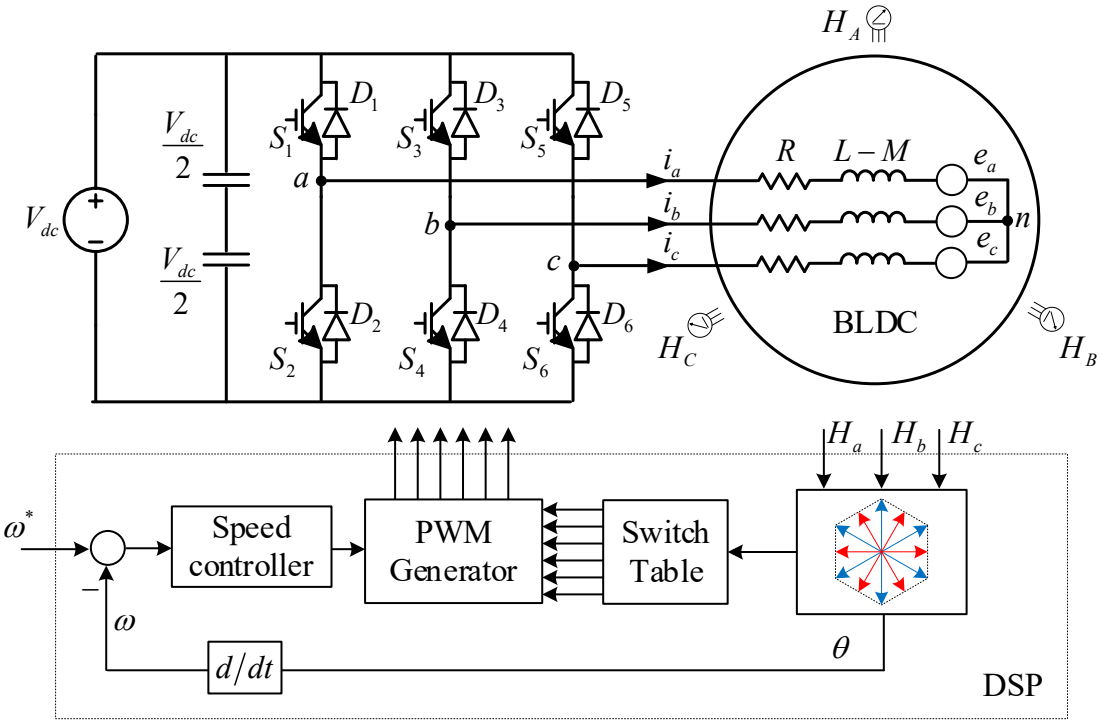


Fig. 6.1. Block diagram of 150-TSC BLDC drive system.

The voltage equations can be expressed as

$$\begin{bmatrix} U_{an} \\ U_{bn} \\ U_{cn} \end{bmatrix} = R \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + (L - M) \frac{d}{dt} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (6\text{-}1)$$

where R is the stator resistance, L and M are the self and mutual winding inductances. $U_{an,bn,cn}$, $I_{a,b,c}$ and $e_{a,b,c}$ are the three-phase supply voltages, phase currents and phase back-EMFs, respectively. The relationships of the voltage vectors, the sector numbers and the conducting modes are shown in Table 6.1 and Fig. 6.2. Mode I and Mode II are presented in blue and red respectively.

Table 6.1 RELATIONSHIP BETWEEN SECTOR NUMBER AND DRIVE SIGNALS

Sector number (N)	Drive signals (S_1- S_6)
I (A+B-C+)	100110
II (A+B-C~)	100100
III (A+B-C-)	100101
IV (A+B~C-)	100001
V (A+B+C-)	101001
VI (A~B+C-)	001001
VII (A-B+C-)	011001
VIII (A-B+C~)	011000
IX (A-B+C+)	011010
X (A-B~C+)	010010
XI (A-B-C+)	010110
VI (A-B-C+)	010110
VII (A~B-C+)	000110

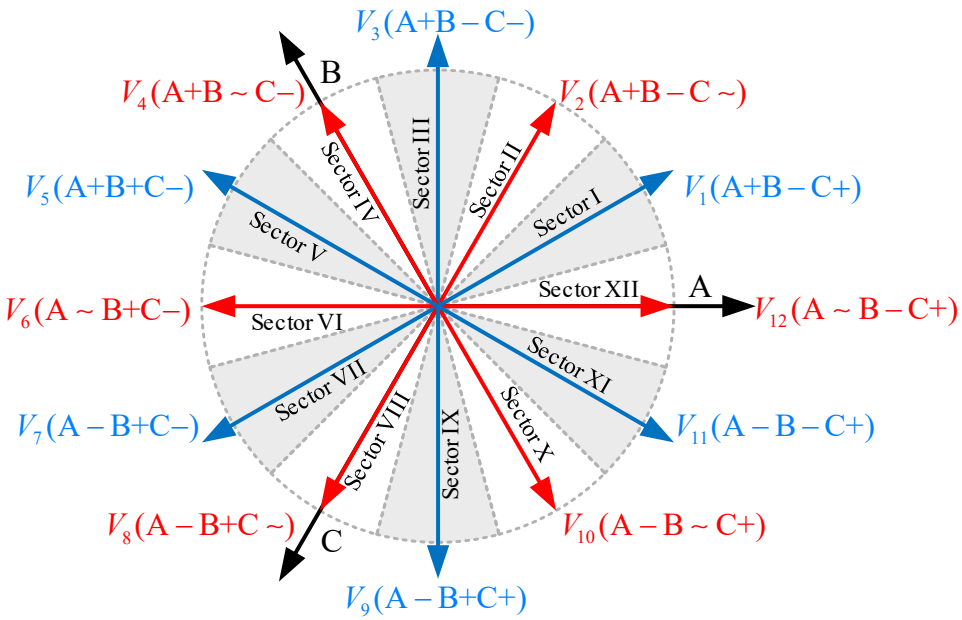


Fig. 6.2. Relationships of the voltage vectors, the sector numbers and the conducting modes of 150-TSC.

Taking Sectors I and II for example. In Sector I, phase A and phase C are both connected to the DC voltage supply while phase B is connected to the ground. Thus, the voltage vector V_1 of Sector I can be expressed as

$$V_1 = \overrightarrow{U_{an}} - \overrightarrow{U_{bn}} + \overrightarrow{U_{cn}} = DV_{dc}e^{j\frac{1\pi}{12}} \tag{6-2}$$

In Sector II, phase A is connected to the DC voltage supply, phase B is connected to the ground while phase C is floating. Thus, the voltage vector V_2 of Sector II can be expressed as

$$V_2 = \overrightarrow{U_{an}} - \overrightarrow{U_{bn}} = \frac{\sqrt{3}}{2}DV_{dc}e^{j\frac{1\pi}{6}} \tag{6-3}$$

The other voltage vectors V_3~V_{12} can also be calculated accordingly. It should be noticed that the supply voltage magnitudes under different conducting modes are not identical as analysed in (6-2) and (6-3). The stator flux linkage variation during different conducting modes can be expressed as

$$\lambda_{uv} = \frac{\sqrt{3}}{2}\frac{V_{dc}}{\omega_e}D_{uv}\theta_{sector} \tag{6-4}$$

$$\lambda_{uvw} = \frac{V_{dc}}{\omega_e} D_{uvw} \theta_{sector}$$

where $\lambda_{uv,uvw}$ and $D_{uv,uvw}$ are the flux linkage variation and duty ratio under two conducting modes respectively. V_{dc} is the supply voltage. θ_{sector} is the interval of each sector. The duty ratios under two conducting modes are modulated so that the stator flux linkage variations in different sectors are identical. The relationship between the duty ratios in different conducting modes can be expressed as

$$\frac{D_{uvw}}{D_{uv}} = \frac{\sqrt{3}}{2} \tag{6-5}$$

6.2.2 Analysis of Commutation Errors

In this chapter, the Hall sensors are used for rotor position detection. For a general BLDC drive system, three Hall sensors that are usually utilised, mounted 120 electrical degrees apart from each others. However, it should be noticed that the BLDC 150-TSC, like other wide angle BLDC controls, requires twelve commutation points. Since the 150-TSC is a symmetrical control and each sector has the same interval of 30 electrical degrees, the twelve commutation points can be easily obtained through the Hall sensors. The line-to-line back-EMFs, the Hall signals and the commutation points considering commutation errors are shown in Fig. 6.3.

It is widely known that there always exists Hall sensor placement errors in practical condition [ALA12]. As shown in Fig. 6.3, the Hall signal errors of three Halls sensors are represented by $\varepsilon_{a,b,c}$, while the ideal and the real Hall signals are illustrated as $H'_{a,b,c}$ and $H_{a,b,c}$ respectively. If the Hall sensor lags behind the ideal position, the error is defined as negative, otherwise, it is positive. The sectors and the corresponding conducting modes can also be defined according to the Hall signals. The relationship between the ideal and real Hall signals and the Hall signal errors can be expressed as

$$H_{a,b,c}{}' = H_{a,b,c} - \varepsilon_{a,b,c} \tag{6-6}$$

If there exists the Hall signal errors, the sectors are then unevenly divided. The balanced operation is solved through the method proposed in [ALA12]. It should be noticed that this method can only lock the commutation points to the one of the Hall sensors with the minimal

Hall signal error. Suppose the Hall sensor H_A has the minimum error, then $\varepsilon_{h\min}$ can be expressed as

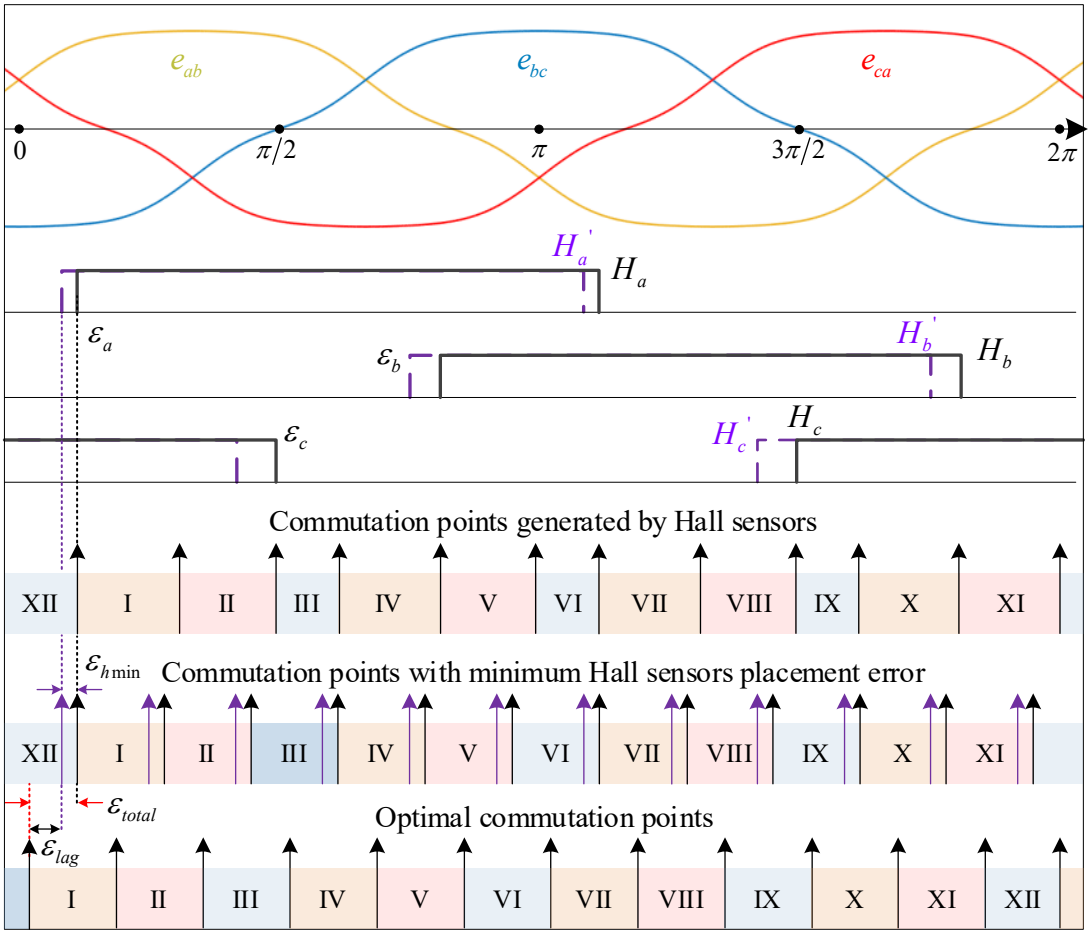


Fig. 6.3. Analysis of commutation errors.

$$\varepsilon_{h\min} = \varepsilon_a \tag{6-7}$$

After the compensation, the commutation points with the minimum Hall signal error, which is marked in black, is still lag behind the commutation points generated by the ideal Hall signals as marked in purple in Fig. 6.3.

Apart from the Hall signal errors, for the BLDC 150-TSC, there will also exist the phase delay error ε_{lag} due to the free-wheeling time caused by the motor inductance [GUC18] as shown in Fig. 6.3. Even if the commutation points are generated by the ideal Hall signals, the phase currents and the phase back-EMFs are still not in phase with each other. For a high speed BLDC 150-TSC, this kind of error cannot be neglected. This means the optimal commutation points are no longer the same as the ones generated by the ideal Hall signals. Thus, the phase advance control is required to move the optimal commutation points ahead. However, it should be

noticed that the phase delay error is hard to theoretically calculate since the free-wheeling time of BLDC 150-TSC depends on multiple factors such as motor speed ω_e, winding resistance R, winding inductance L_s and load T [GUC18]. The phase delay error can be expressed as

$$\varepsilon_{lag} = f(\omega_e, R, L_s, T, \dots) \tag{6-8}$$

The total commutation error ε_{error} can be defined as the combination of the minimum Hall signal error $\varepsilon_{h\min}$ and the phase delay error ε_{lag} as

$$\varepsilon_{error} = \varepsilon_{h\min} + \varepsilon_{lag} \tag{6-9}$$

6.3 Proposed Online Commutation Error Compensation Method

As analysed in the previous section, both the Hall signal error and the phase delay error will lead to inaccurate commutation. In this section, the total commutation error is considered and an optimization method is proposed to achieve the optimal commutation for the BLDC 150-TSC drive system. Rather than detecting or analysing different kinds of commutation error separately, the stator current I_s is used as the criterion to determine the total commutation error as a whole. By reducing the stator current magnitude to the minimum value through phase advance control, the phase current will be in the same phase with the phase back-EMF. The optimal commutation points can thus be obtained. It should be noticed that although the BLDC 150-TSC could achieve a quasi-sinusoidal current waveform, it still contains harmonic current components. Thus, an Adaline is proposed to act as the band-pass filter (BPF). The fundamental phase current is extracted so that the stator current suffers from no harmonic problem. The GDO algorithm is then utilized to determine the phase advance angle by minimizing the stator current. The proposed online commutation optimization method is presented in detail in this section.

6.3.1 Commutation Error Detection

Since the phase delay error is usually hard to obtain theoretically, in this chapter, an indirect method is used to detect the total commutation error ε_{lag}. The space vectors, which are commonly used for the PM motor drive analysis, are considered here. The transformation function $C_{abc}^{\alpha\beta0}$ is used to obtain the current vectors $\overrightarrow{\imath_{\alpha\beta}}$ in the stationary reference frame, and can be expressed as

$$C_{abc}^{\alpha\beta 0} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{6-10}$$

Considering the total commutation error ε_{lag}, the space vectors of stator current $\vec{\imath_s}$, back-EMF $\vec{e}$ and supplied voltage $\vec{u}$ for BLDC 150-TSC are presented in Fig. 6.4, together with the current vectors $\overrightarrow{\imath_{\alpha\beta}}$.

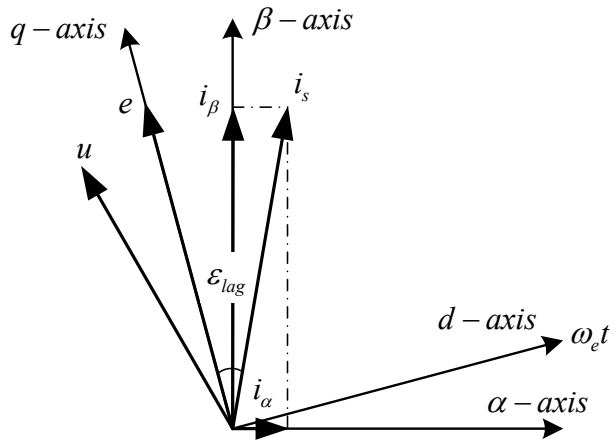


Fig. 6.4. Analysis of space vectors.

According to (6-10) and Fig. 6.4, the relationship between the stator current magnitude I_s and the phase currents $I_{a,b,c}$ can be expressed as

$$I_s = |\vec{\imath_s}| = \sqrt{|\vec{\imath_\alpha}|^2 + \left|\vec{\imath_\beta}\right|^2} = \sqrt{{I_a}^2 + \frac{1}{3}(I_b - I_c)^2} \tag{6-11}$$

After the coordination transformation, the total commutation error can be presented by the deviation between the stator current vector $\vec{\imath_s}$ and the back-EMF vector $\vec{e}$. If there is no commutation error, the current vector will be in the same phase with the back-EMF vector. The magnitude of the stator current will also achieve the minimum value. As shown in (6-11), the stator current magnitude can be calculated directly from the phase currents without using the position signal. Thus, in this chapter, the stator current is chosen as the criterion to determine the total commutation error and generate the optimal phase advance angle.

It should be emphasised again that even though the 150-TSC method could generate quasi-sinusoidal phase current waveforms compared with the traditional 120-SSC method, the phase currents still contain harmonics. If the phase currents are sinusoidal, the stator current magnitude will be a constant value. However, this is not the case. Suppose the actual commutation points are lag behind the optimal ones, the phase and stator current waveforms are presented in Fig. 6.5, while the stator current spectrum under BLDC 150-TSC is shown in Fig. 6.6.

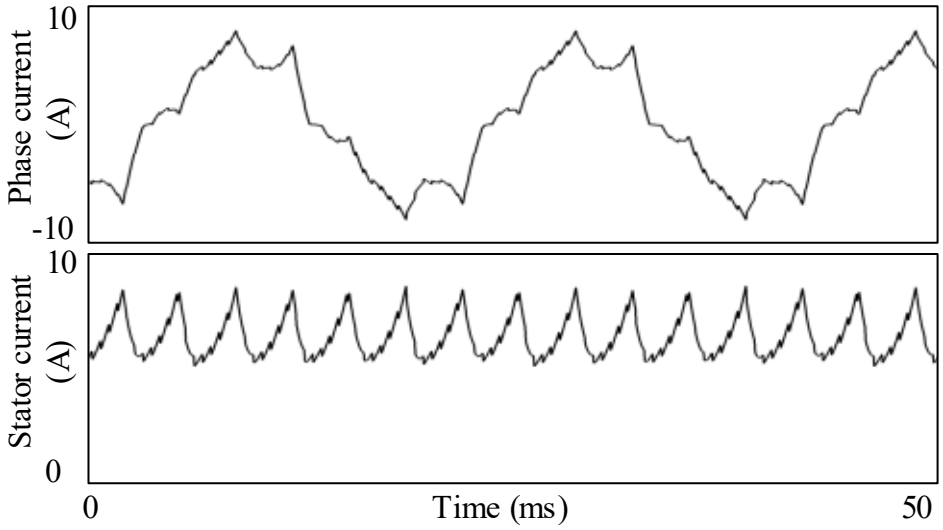


Fig. 6.5. Phase and stator current waveforms under BLDC 150-TSC.

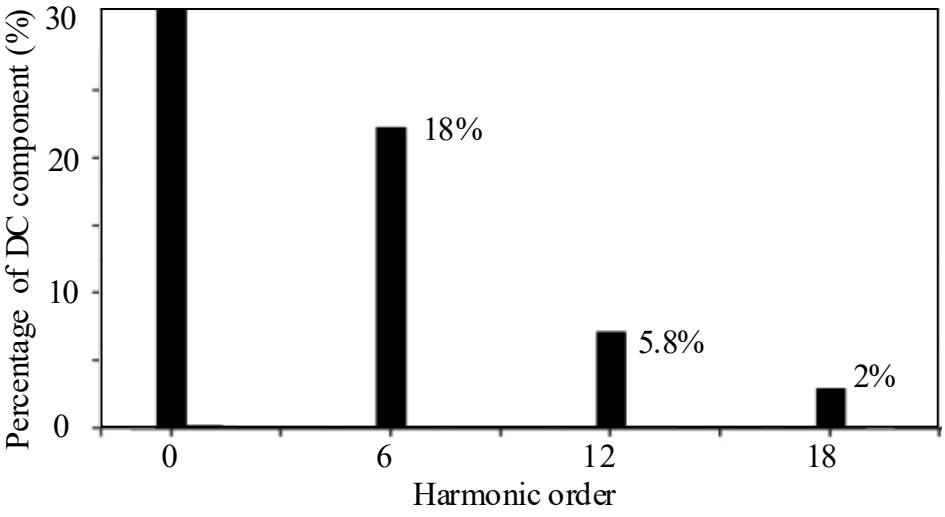


Fig. 6.6. Stator current spectrum under BLDC 150-TSC.

Due to the existence of the phase current harmonics, the stator current also contains harmonics that will cause challenges to stator current magnitude detection and further phase advance angle generation process. In order to solve this problem, the fundamental phase currents should still be extracted first so that the stator current suffers no harmonics problems.

In this chapter, the Adaline is used as the band-pass filter (BPF). The principle is to use the adaptive neurons to let desired frequency signal pass. To act as the single-frequency pass filter, only two neurons are needed whose weights are adaptive tuned online by the least mean square (LMS) or the recursive least square (RLS) algorithms [CIR09]. In this chapter, the LMS algorithm is utilized since the RLS method requires more computations. The block diagram of the Adaline BPF in continuous domain is shown Fig. 6.7, where d, r and y denote the primary, reference inputs and the selected output. The difference between d and y is denoted as error e.

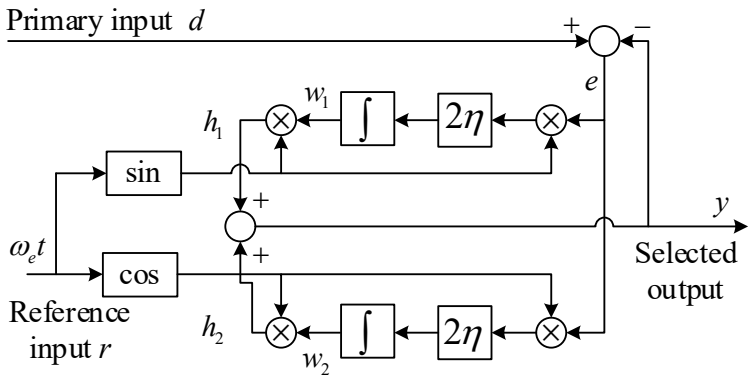


Fig. 6.7. Block diagram of the Adaline BPF.

In order to extract the fundamental current, the reference input which relates with the motor speed related signal is processed by the sine and cosine functions. Then, the weight factors w_1 and w_2 can be expressed as

$$w_1 = \int 2\eta \, sin(\omega_e t) e dt$$
$$w_2 = \int 2\eta \, cos(\omega_e t) e dt \quad (6\text{-}12)$$

where η is the learning rate. h_1 and h_2 can then be expressed as

$$h_1 = sin(\omega_e t) \int 2\eta \, sin(\omega_e t) e dt \quad (6\text{-}13)$$

$$h_2 = cos(\omega_e t) \int 2\eta \, cos(\omega_e t) e dt$$

The Laplace transformation of (6-13) can be expressed as

$$\begin{aligned} H_1(s) &= \frac{2\eta}{4(s + j\omega_e)}[e(s) + e(s + 2j\omega_e)] + \frac{2\eta}{4(s - j\omega_e)}[e(s) + e(s - 2j\omega_e)] \\ H_2(s) &= \frac{2\eta}{4(s + j\omega_e)}[e(s) - e(s + 2j\omega_e)] + \frac{2\eta}{4(s - j\omega_e)}[e(s) - e(s - 2j\omega_e)] \end{aligned} \tag{6-14}$$

Since the output $y = h_1 + h_2$ and the error $e = d - y$, the transfer function $G(s)$ from d to y can thus be expressed

$$G(s) = \frac{Y(s)}{D(s)} = \frac{2\eta s}{s^2 + 2\eta s + \omega_e^2} \tag{6-15}$$

As shown in the analysis, the Adaline can act as a 2nd order BPF whose centre frequency is determined by the reference input. By tuning the learning rate η, the bandwidth of the BPF is also determined. It should be noticed that the η will also determine the learning speed of the Adaline. There exists a trade-off between the passband width and the learning speed when choosing η. If η is small, the passband width becomes narrower at the cost of slow learning speed. In practice, the learning rate is selected according to the practical conditions. In this chapter, the learning rate η is selected as 0.005.

6.3.2 Commutation Optimization Method

After extracting the fundamental phase currents, they are utilized to calculate the stator current. By minimizing stator current magnitude through phase advance control, the optimal commutation points can be obtained. In this chapter, the GDO algorithm [YAN19B] is utilized to determine the phase advance angle θ_{adv}. The schematic of the GDO is shown in Fig. 6.8.

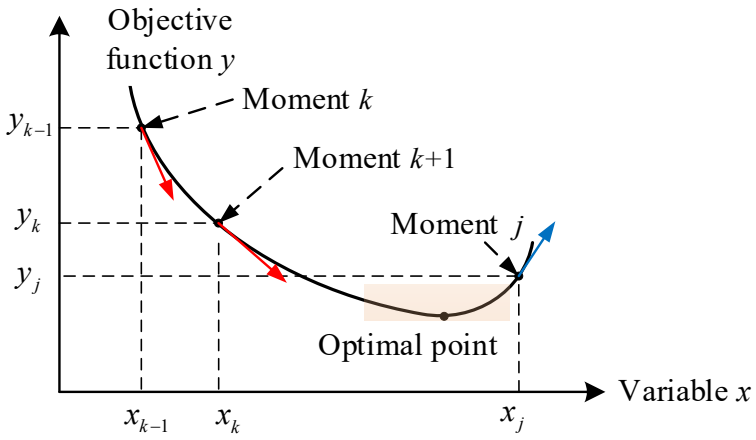


Fig. 6.8. Schematic of the GDO.

The objective function can be expressed as

$$min\, f\,(\theta_{adv}) = I_s \tag{6-16}$$

As shown in Fig. 6.8, the gradient of the objective function f at the kth sample point is used to adjust the phase advance angle at the k+1th sample point while the gradient of function f can be expressed as

$$\nabla = \frac{\partial f}{\partial \theta_{adv}} = \frac{I_s(k) - I_s(k-1)}{\theta_{adv}(k) - \theta_{adv}(k-1)} \tag{6-17}$$

Then, the phase advance angle θ_{adv} can be updated as

$$\theta_{adv}(k+1) = \theta_{adv}(k) - sgn(\nabla)d\theta \tag{6-18}$$

where $sgn()$ is the sign function while $d\theta$ is the step-size that should be chosen considering the practical conditions. Here the '$-$' means the desire direction is the opposite of the gradient. Considering the practical condition, $d\theta$ is selected as 0.4° while the execution frequency of the GDO is set to 50Hz in this chapter. If the gradient is negative as marked in red in Fig. 6.8, then the phase advance angle at the next sample point will increase according to (6-18). Otherwise, the phase advance angle will decrease. It should be noticed that the DC current I_{dc} can also be used for the optimal commutation point detection. When the DC current I_{dc} is reduced to the minimum value, the phase advance angle can be obtained. However, the use of DC current will require additional DC current sensor. Thus, it is not considered in this thesis.

The block diagram of 150-TSC BLDC system with proposed online commutation optimization method is shown in Fig. 6.9. The stator current calculated from the phase currents is utilized to

generate the phase advance angle θ_{adv}. Together with the Hall signals, the optimal commutation points can be obtained.

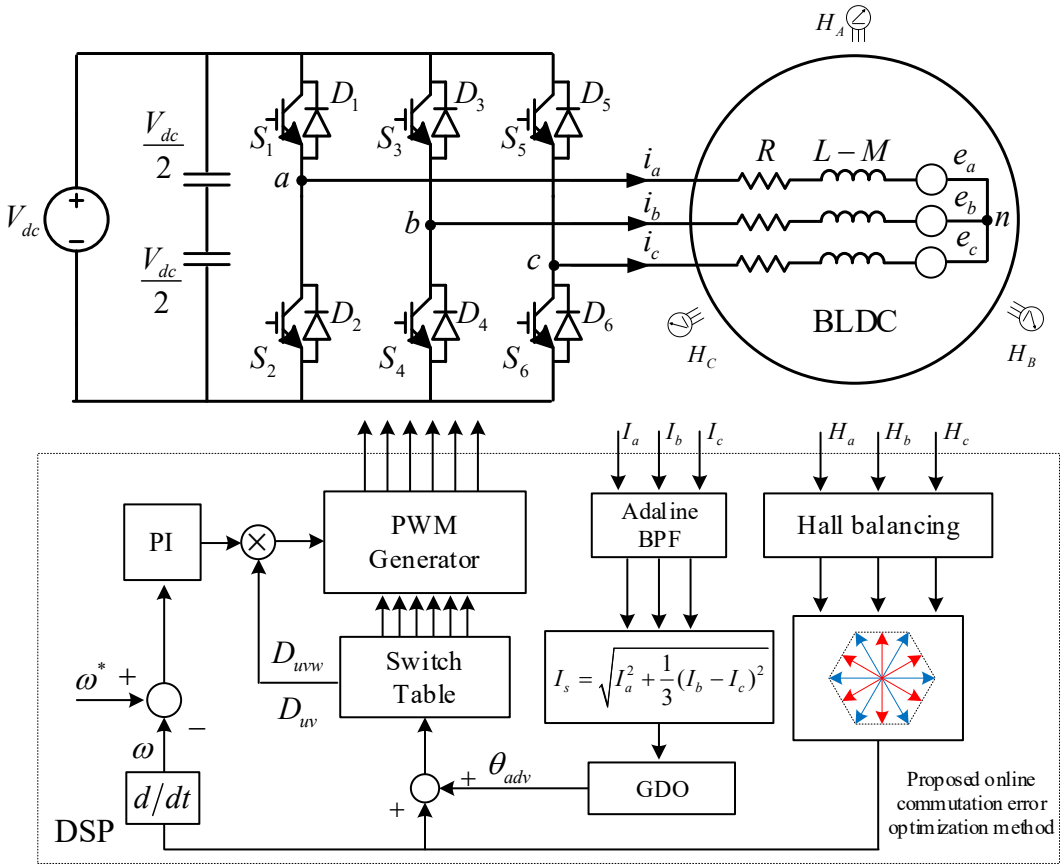
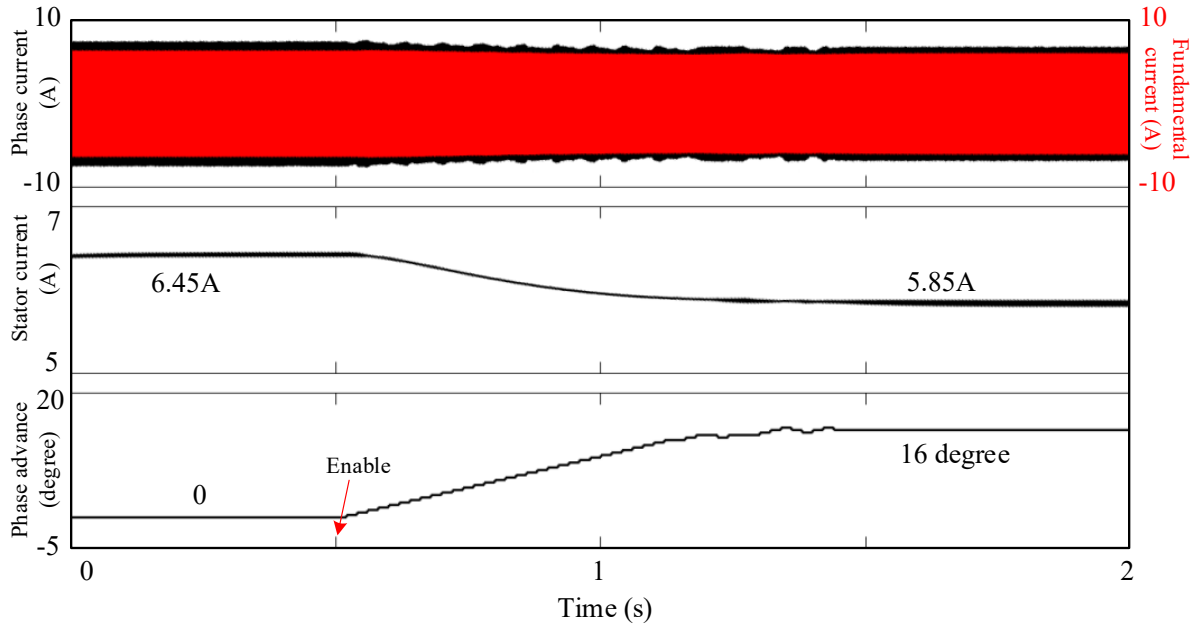


Fig. 6.9. Block diagram of 150-TSC BLDC drive system with proposed online commutation optimization method.

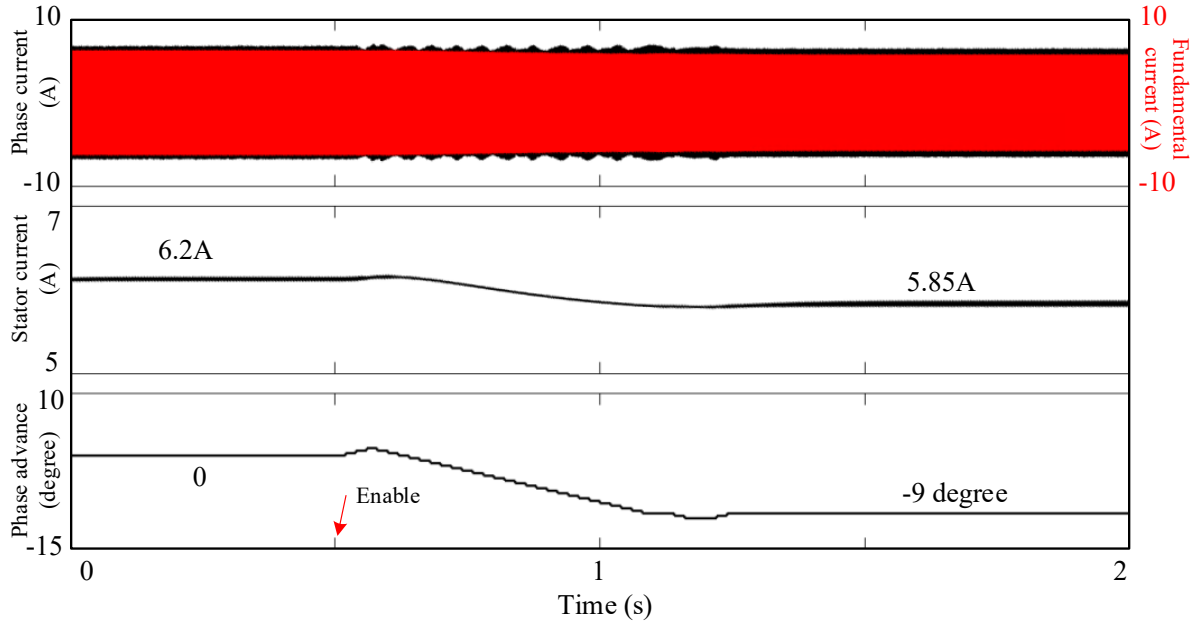
6.4 Simulation Verification

To verify the effectiveness of the proposed commutation compensation method, a simulation model is built in MATLAB/Simulink. The sampling period T_s is set to 50 μs while the switch frequency is set to 20 kHz. It should be also noticed that when the GDO algorithm is used, the desired direction of the gradient is hard to be accurately determined when the load torque is varying. Thus, the proposed method is more suitable to be employed under steady state conditions. Several simulations are undertaken at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) under full load at steady state as shown in Fig. 6.10.

The compensation is enabled at 0.5s so that both the simulation results before and after the proposed commutation optimization method are presented. Suppose the Hall sensor are placed



(a) Commutation points lag behind optimal ones.



(b) Commutation points lead optimal ones.

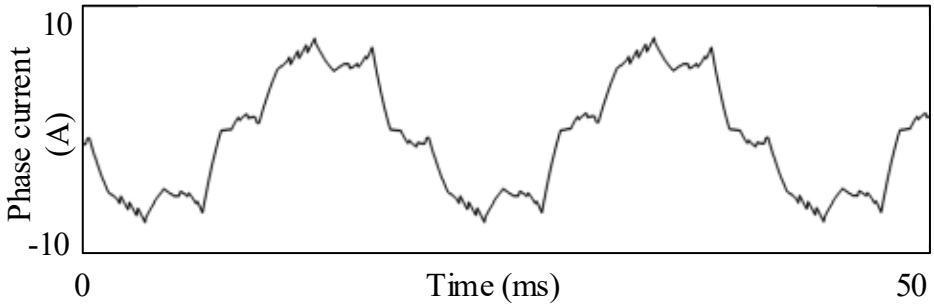
Fig. 6.10. Simulation results at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) under full load before and after proposed online commutation optimization method.

behind the ideal position, the commutation points lag behind the optimal ones. Then, the simulation results are given in Fig. 6.10(a). When the initial commutation points are leading the optimal ones, the corresponding simulation results are given in Fig. 6.10(b). The phase

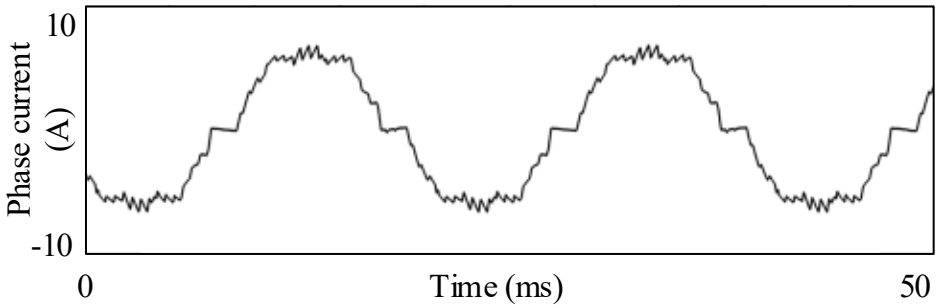
current, the extracted fundamental phase current, the stator current and the phase advance angle are shown from the top to the bottom. The phase current is marked in black while the extracted fundamental current is marked in red.

As shown in Fig. 6.10, the fundamental phase current can be extracted by the Adaline BPF so that stator current contains only DC component. After the proposed online commutation optimization method is enabled, the stator current is minimized by employing proper phase advance angle. If the commutation points lag behind the optimal ones, as shown in Fig. 6.10(a), the phase advance angle increases gradually. Otherwise, if the commutation points already lead the optimal commutation points, the phase advance angle will decrease until the stator current reaches the minimum value. As can be seen from the simulation result, the proposed method can achieve optimal commutation.

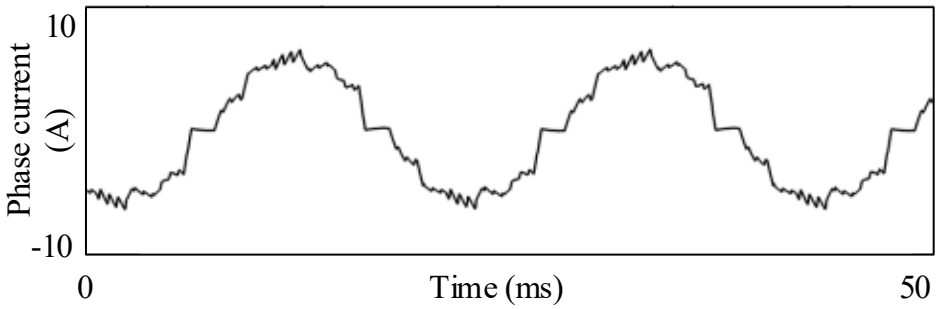
The phase current waveforms and spectra under different conditions are presented in Fig. 6.11. When the commutation points lag behind the optimal ones as shown in Fig. 6.11(a), the current waveform has a high peak-to-peak (P-P) value of 16A. The phase current also suffer from large harmonics. The magnitude of the fundamental current is 6.5A under this condition while the current total harmonic distortion (THD) is 21.5%. If the commutation points lead the optimal ones, the current harmonic problem becomes less severe. However, the magnitude of the fundamental current is still 6.2A as shown in Fig. 6.11(b). When the proposed commutation optimization method is used, the optimal commutation could be achieved. The magnitude of the fundamental current is largely reduced to 5.8A while the current THD decreases nearly half to 12% as shown in Fig. 6.11(c). A quasi-sinusoidal current waveform with low harmonics can be generated by the 150-TSC with the proposed method. As shown in the simulation results, the control performance is improved with the proposed method. Overall, the effectiveness of the proposed online commutation optimization method is verified through simulation results.



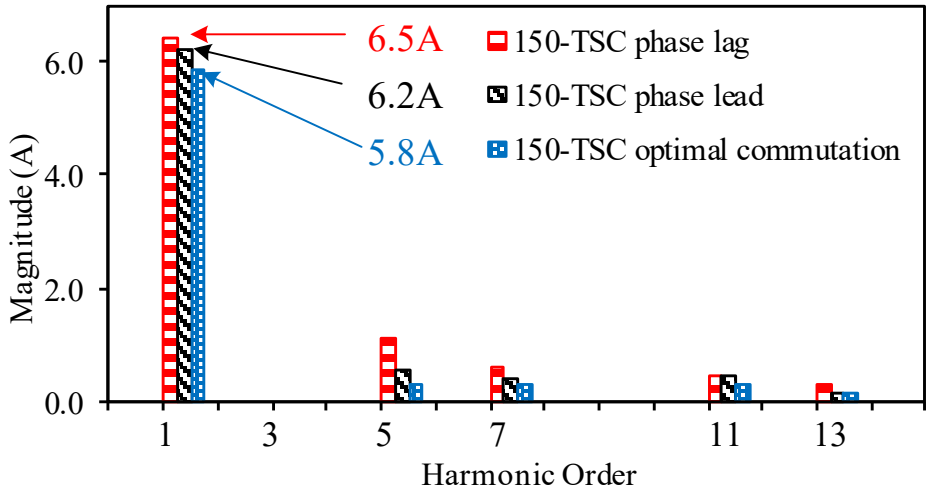
(a) Commutation points lag behind optimal ones under 150-TSC.



(b) Commutation points lead optimal ones under 150-TSC.



(c) Optimal commutation under 150-TSC.



(d) Current spectra.

Fig. 6.11. Simulation results of phase current waveforms and spectra at $\omega_e = 1000\pi$ rad/s ($f_e = 500$ Hz) under full load.

6.5 Conclusion

In this chapter, a novel commutation error compensation strategy for high speed BLDC 150-TSC drives is proposed. The stator current is chosen as the criterion to determine the total

commutation error. The GDO algorithm is utilized to determine the phase advance angle so that the optimal commutation signals can be obtained. The Adaline BPF is also proposed to extract stator current from harmonics. The proposed online commutation optimization method can be implemented in general inverter controllers. The control performance of the system could be improved and a quasi-sinusoidal current waveform with low THD could be generated with the proposed BLDC 150-TSC. The effectiveness of this method is verified by both simulation and experimental results.

Compared with the method based on d-axis current proposed in the previous chapter, no absolute position signal is needed for the stator current based method. However, it should be noticed since the GDO algorithm is used, the desire direction of the gradient is hard to be accurately determined when the load torque is varying. Thus, the proposed method is more suitable to be employed under steady state conditions.

CHAPTER 7

GENERAL CONCLUSIONS AND FUTURE WORK

7.1 General Conclusions

This thesis has presented a comprehensive investigation into control strategies for high speed PM brushless motor drives, considering both brushless AC (BLAC) drives and brushless DC (BLDC) drives. The key contributions of this thesis can be summarised as follows:

- The current harmonic problem becomes more severe for high speed BLAC drives considering the low switching-to-fundamental frequency ratio (SFFR) and low motor inductance. In Chapter 2 and Chapter 3, various non-ideal factors, including inverter nonlinearity effect and non-sinusoidal back-electromotive force (back-EMF) have been analyzed while different current harmonic compensation methods are proposed;
- The commutation errors have a direct influence on the control performance of high speed BLDC drives. In Chapter 4, the position signal error is thoroughly analyzed. A Hall signal balancing method is proposed to deal with the position signal error problem together with a novel PWM generation scheme. In Chapter 5 and Chapter 6, the phase delay error is investigated and compensated. The compensation method proposed in Chapter 5 can achieve high control performance at the cost of precise absolute position requirement. The compensation method proposed in Chapter 6 can reduce the control complexity at the cost of decreased transient control performance.

Several novel control strategies are proposed for the first time. Some findings and conclusions are detailed below.

7.1.1 BLAC control strategies

For BLAC drives, sinusoidal current waveforms are preferable since the current harmonics decrease the lifetime of the motor and undermine the stability of the operation. In ideal cases, the current waveforms can be considered to be the same as the sinusoidal reference commands. However, practical motors and drives have to consider non-ideal factors, such as inverter nonlinearity effect and non-sinusoidal back-EMF. If not properly compensated, these distortions caused by non-ideal factors will eventually result in current harmonics. Thus, it is desirable to develop current harmonics suppression method.

The inverter nonlinearity effect is inevitable for practical BLAC drives which will cause $6n\pm1^{th}$ order distortion, see (2-15). To solve this, an inverter nonlinearity compensation method based on the analysis and minimization of current harmonics in the synchronous reference frame is firstly presented. The magnitudes of current harmonics can be obtained through simple signal processing algorithms, see (2-15). However, it is noticed that with the increase of the motor speed, the current distortion becomes more severe even if the proposed inverter nonlinearity compensation method is employed, Fig. 2.18. This phenomenon is caused by the other non-ideal factors such as non-sinusoidal back-EMFs. It is known that the effect of inverter nonlinearity is almost irrelevant with motor speed, while voltage distortions caused by the non-sinusoidal back-EMF components increase with the motor speed, see (3-5). Based on the analysis, the maximum voltage distortions caused by the two non-ideal factors in both the d-axis and the q-axis can be approximated as shown in Table 7.1.

Table 7.1 MAXIMUM VOLTAGE DISTORTIONS CAUSED BY DIFFERENT NON-IDEAL FACTORS

Voltage distortion caused by	d-axis	q-axis
Back-EMF	$\omega(k_2+k_5+k_7)$	$\omega(k_2+k_5-k_7)$
Inverter nonlinearity	$\frac{48}{35\pi}\frac{T_{dt}}{T_{pwm}}V_{dc}$	$\frac{8}{35\pi}\frac{T_{dt}}{T_{pwm}}V_{dc}$

Since the relationship between the back-EMF distortion and the inverter nonlinearity distortion changes with the motor speed, the operation speed is defined by three ranges.

- In Range I, the voltage distortions caused by non-sinusoidal back-EMF are smaller than that caused by inverter nonlinearity in both the d-axis and the q-axis;
- In Range III, the voltage distortions caused by non-sinusoidal back-EMF are larger than that caused by inverter nonlinearity in both the d-axis and the q-axis
- The rest speed range is defined as Range II.

The qualitative analysis of the relationship between the voltage distortions caused by the inverter nonlinearity and the non-sinusoidal back-EMF is shown in Fig. 7.1. As shown in the figure, in Range I, the inverter nonlinearity effect acts as the dominant reason for current distortion while in Range III, the back-EMF harmonics are the main reason. However, in Range II, these two factors are coupled together, and it is hard to separate one from another.

Nevertheless, it is known that both the back-EMF harmonics and the inverter nonlinearity effect introduce periodic distortions. If these two factors are considered as a whole, as long as voltage distortion can be estimated, the current harmonics can be well compensated by adding a proper feedforward compensation voltage in the synchronous reference frame. Thus, the current harmonics suppression method that has the ability to compensate different non-ideal factors together is investigated.

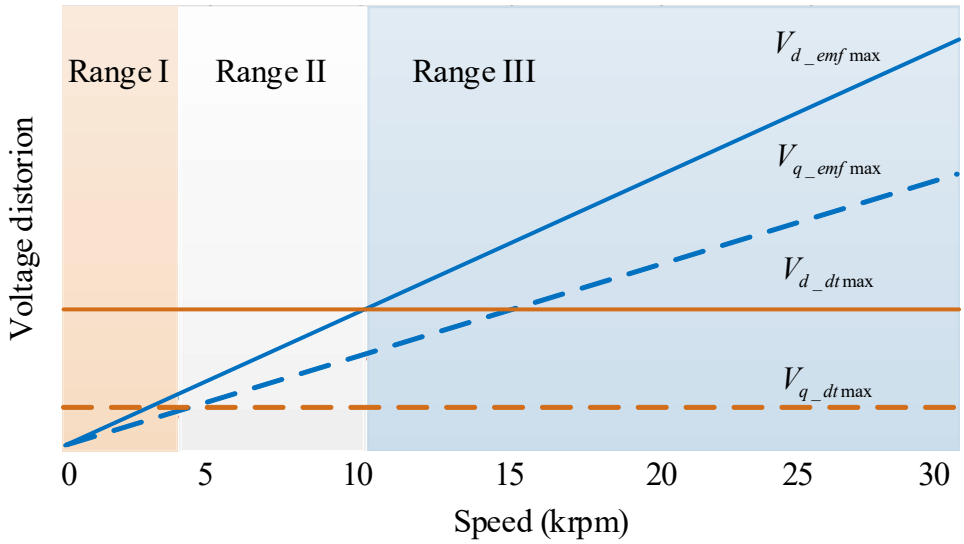


Fig. 7.1. Relationship between the voltage distortions caused by the inverter nonlinearity and the non-sinusoidal back-EMF.

The voltage equations of BLAC drives in the synchronous reference frame considering different non-ideal factors can be expressed as

$$V_{dq} = V_{dq}^{*} + \Delta V_{dq} = E + I_{dq} Z_{dq} \tag{7-1}$$

where V_{dq}^{*} is the reference voltage command, ΔV_{dq} is the overall voltage distortion. V_{dq} and I_{dq} are the voltage and current in the synchronous reference frame, respectively. As shown in (7-1), as long as the voltage distortion ΔV_{dq} is eliminated by adding a proper feedforward compensation voltage V_{ff_dq}, see (3-16), the sinusoidal current will be achieved, as shown in Fig. 3.6. An adaptive feedforward compensation voltage generation method is proposed in this thesis. With the help of least-mean-square (LMS) algorithm, the compensation voltages can be obtained without the knowledge of any motor parameters. The control system with the proposed current harmonics suppression method is presented in Fig. 3.7. It is shown in the results that the proposed method can present good performance under both steady and transient

states, Fig. 3.23 and Fig. 3.24.

The comparison between two current harmonics suppression methods are given in Table 7.2. As can be seen, the adaptive current harmonics compensation method proposed in Chapter 3 is superior to the one proposed in Chapter 2 at the cost of relatively complex control algorithm. However, it should be noticed that the computation requirement is not a burden for most of the controllers nowadays. Thus, the method proposed in Chapter 3 can be used in wide applications. For the applications where the computation requirement is strictly restricted or where the inverter nonlinearity effect play a dominant role, the method proposed in Chapter 2 can still achieve a good performance due to its simple algorithms.

Table 7.2 COMPARISON BETWEEN CURRENT HARMONICS SUPPRESSION METHODS

Method proposed in	Advantages and *disadvantages*
Chapter 2	a. Simple algorithms and easily implementation *b. Only consider inverter nonlinearity* *c. Limited applications*
Chapter 3	a. Consider different non-ideal factors b. Wide applications and able to compensate any periodic distortions *c. Relatively complex algorithms*

7.1.2 BLDC control strategies

In this thesis, the commutation errors of high speed BLDC drives are also thoroughly analysed. In Chapter 4, the position signal errors that can lead to unbalanced operation is firstly considered. The effects of misaligned Hall signal errors, which are caused by the Hall sensor misplacements, and the uneven Hall signal errors, which are caused by the threshold effect of the Hall sensors, are both analysed. A commutation balancing method is presented in Fig. 4.6. Great efforts are also required to compensate the PWM update delay (see Fig. 4.4) under high speed BLDC drives. Thus, a novel PWM generation scheme is presented with the help of logical operators as shown in Fig. 4.7. The PWM update delay can be eliminated with the proposed PWM generation scheme.

After achieving balanced control, the effect of phase delay error (see Fig. 5.5), which is caused by the free-wheeling time of BLDC drives, is then considered. Since the phase delay error is

related with several factors, such as motor speed ω_e, winding resistance R, winding inductance L_s, and load condition (see (5-5)), it is hard to be theoretically calculated. In Chapter 5, the relationship between the phase delay error and the d-axis current is presented, see (5-7). In this way, a phase delay error compensation method based on reducing the d-axis current is proposed. The optimal control can be achieved when the d-axis current is reduced to zero. Since current waveforms the BLDC drives are not sinusoidal and the currents contain a large amount of motor speed related frequency harmonics, a LMS based Adaline filter is also introduced so that the d-axis current can be precisely obtained without any deviation, as shown in Fig. 5.10 and Fig. 5.11. By employing the proposed method, the phase delay can be successfully eliminated, and the peak-to-peak current can be reduced by as large as 20%. The implementation does not rely on the knowledge of any motor parameters and additional current and voltage sensors.

One potential limit of the d-axis current based phase delay error compensation method is the use of continuous absolute position signal. Besides, the traditional six-step BLDC control strategies also suffer from current harmonics which may cause large torque ripples. Thus, the wide angle twelve-step BLDC drives (see Fig. 6.2) are investigated and a phase delay error compensation method based on the stator current is then proposed. The stator current can be calculated directly from the phase current (see (6-11)) without the continuous absolute position signal. In order to reduce the stator current to the minimum magnitude, the gradient descent optimization (GDO) algorithm is used. It is shown that when the phase delay error is compensated under wide angle twelve-step BLDC drives, a quasi-sinusoidal current waveform with low current harmonics can be generated. However, it should be noticed that since GDO algorithm is employed, the compensation method based on the stator current is more suitable for steady state operation. If the loaded torque varies dramatically during the operation, the optimal phase advance angle is then hard to be determined precisely.

The composition between two phase delay compensation methods are given in Table 7.3.

Table 7.3 COMPARISON BETWEEN PHASE DELAY COMPENSATION METHODS

Method based on	Advantages and *disadvantages*
D-axis current	a. Good steady and dynamic performance b. Fast compensation *c. Require continuous absolute position signal*

Stator current	a. No continuous absolute position signal requirement *b. Limited dynamic performance* *c. Sensitive to varying load torque*

7.2 Future Works

Based on the investigation in this thesis, some future works could be proposed as follows:

- Investigation of the current harmonics compensation method for BLAC drives with simpler control algorithm

In Chapter 3, an Adaline based current harmonics suppression method is proposed for high speed BLAC drive. Although the proposed method can achieve high control performance, the realization of LMS algorithm is still challenging for some low cost applications where the computation capability of the control system is extremely limited. Thus, current harmonics compensation method with simpler control algorithm should be further analysed.

- Investigation of the control strategies to achieve high performance switch between BLAC and BLDC drives

In this thesis, BLAC drive is used for the low and medium speed range while BLDC drive is utilized for the high speed operation in order to achieve overall high control performance. However, the switch process between the BLAC and BLDC drives should be further considered and investigated. Currently, the speed command is kept at constant during the switch. Nevertheless, since the current commands for BLAC and BLDC drives under same load and speed condition are different, the directly drive mode switching will cause an inevitable speed jump. In the future research, more attention should be paid focusing on the drive mode switch process to achieve a smooth switch between the BLAC and BLDC drives.

- Investigation of the performance of wide angle BLDC control with different conducting angles and online conducting angle modulation methods

In Chapter 6, the BLDC 150-TSC is investigated to achieve a quasi-sinusoidal current waveform and reduce the current harmonics. Nevertheless, the current research still cannot draw the conclusion on the optimal commutation angle for the wide angle BLDC control under different load and speed condition. Thus, it is worthy investigating this problem theoretically.

It is also important to further provide online conducting angle modulation methods to achieve optimal control at different operation conditions.

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APPENDIX

EXPERIMENTAL SYSTEM SETUP

The experimental system is constructed based on a TMS320F28335 digital signal processor (DSP) control board. A general three phase voltage source inverter (VSI) which is composed by the IGBT power module is used as the power stage. A DC power source is used for power supply. The host PC is used for information exchange and debugging. A SPM slotted motor loaded with a dynamometer is used for investigation. The whole experimental system is shown in Fig. A.1.

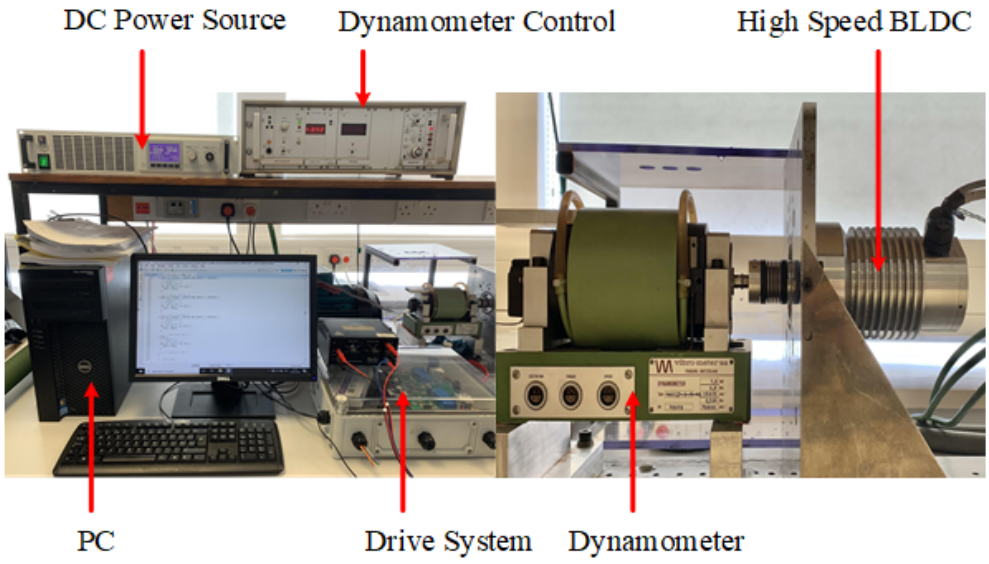
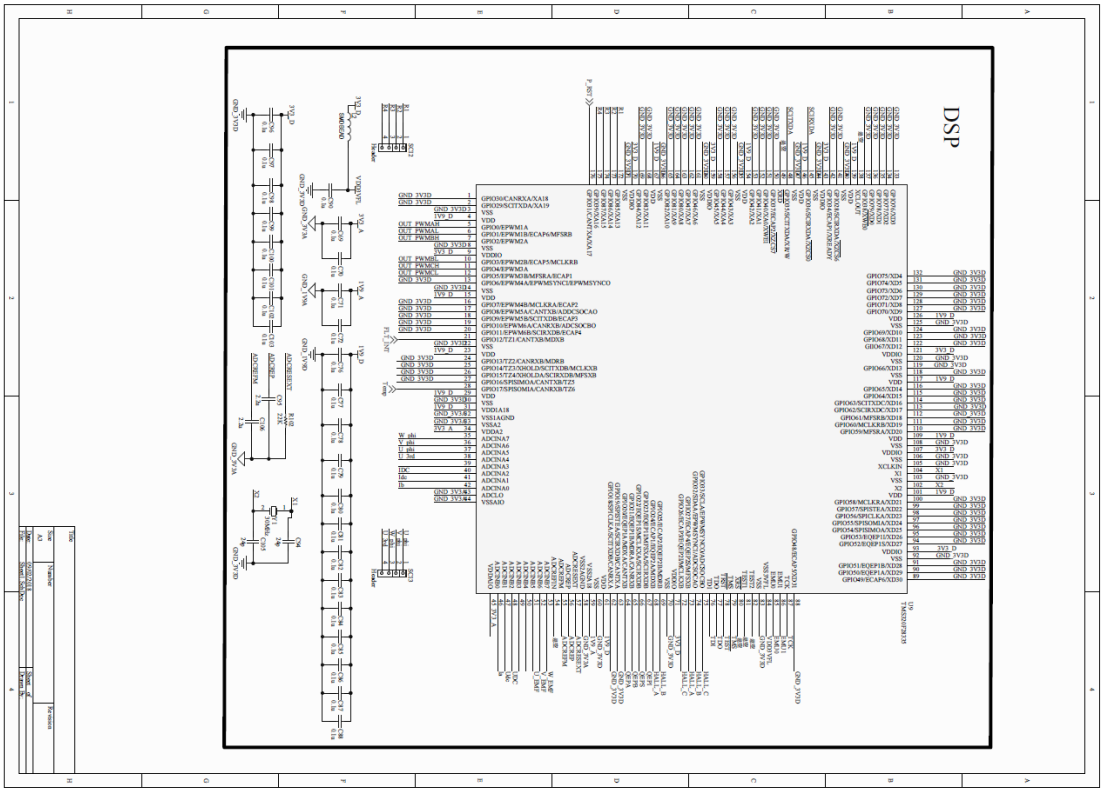
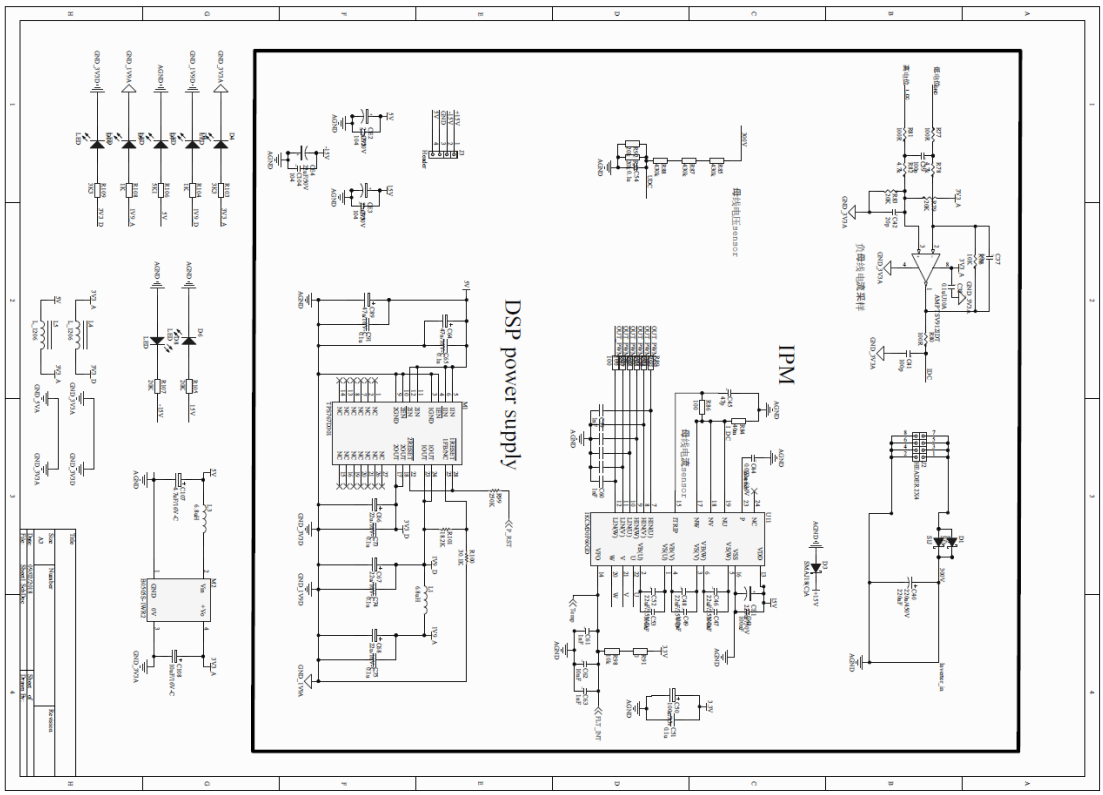


Fig. A.1. Experimental system.

A.1 Control Board

The Texas Instrument DSP TMS320F28335 is chosen as the main processing chip. The DSP communicates with PC through parallel printer port. The three phase VSI is built by a controlled integrated-power-system (IPM) chip provide by Infineon so that no additional drive circuits are needed. Current sensors LA25-P are used to measure phase currents. The measured current signals should be processed by amplifiers before connected with the DSP. The Hall signal processer is designed to obtain position signals. Additional power supply chips, communication chips, AD/DA conversion chips are also needed. The schematic of control system is shown in Fig. A.2.


DSP


DSP power supply
IPM

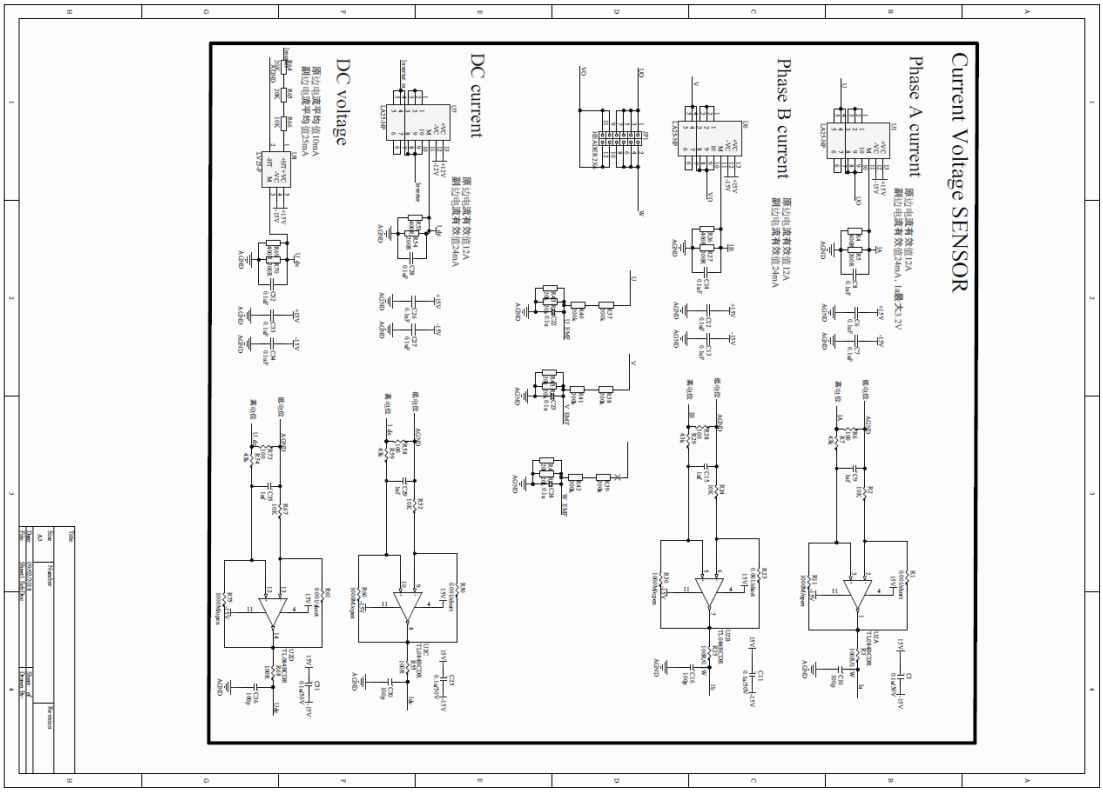


Fig. A.2. Schematic of control system.

The designed PCB board has two layers. The PCB layout is shown in Fig. A.3.

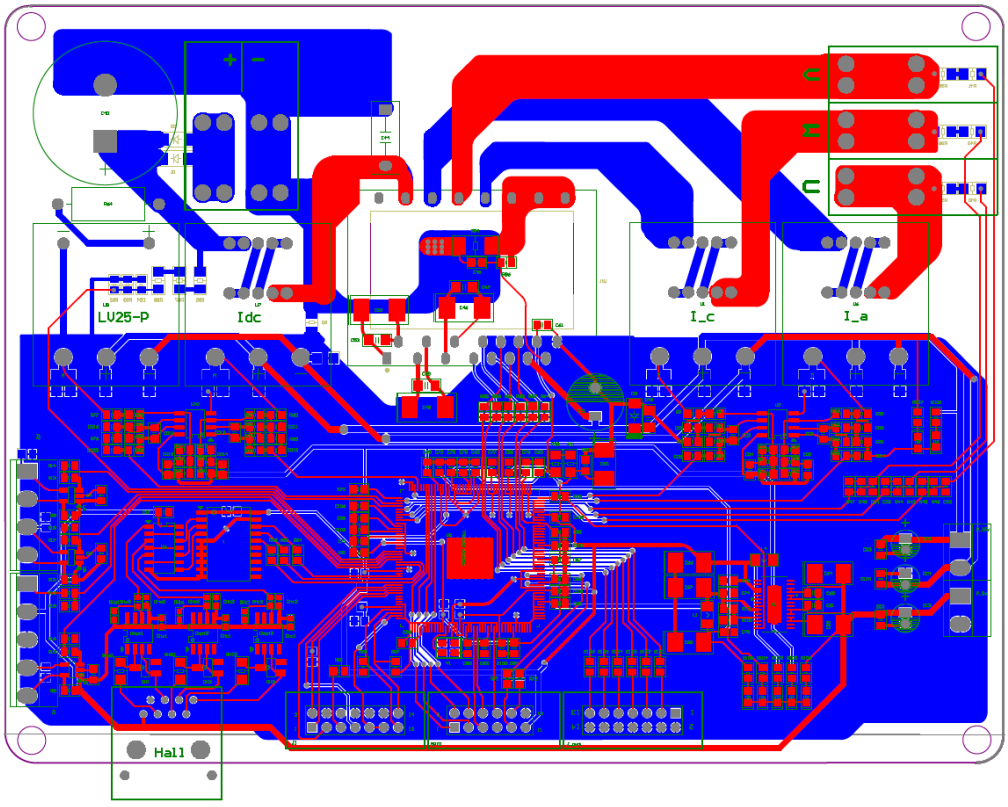
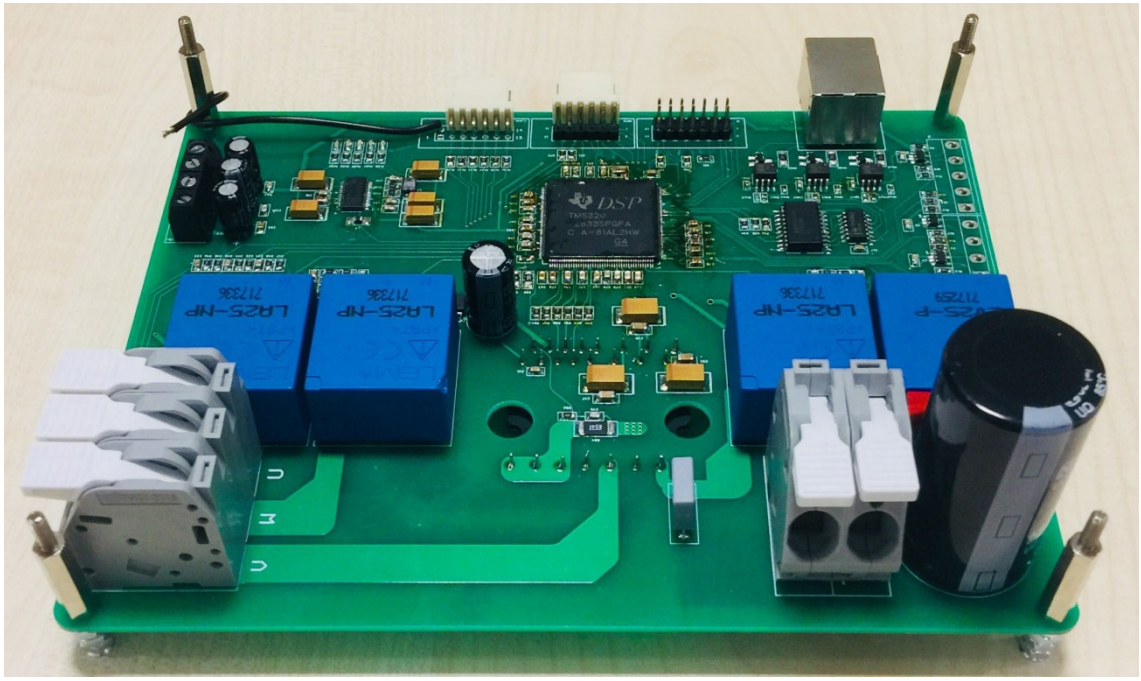
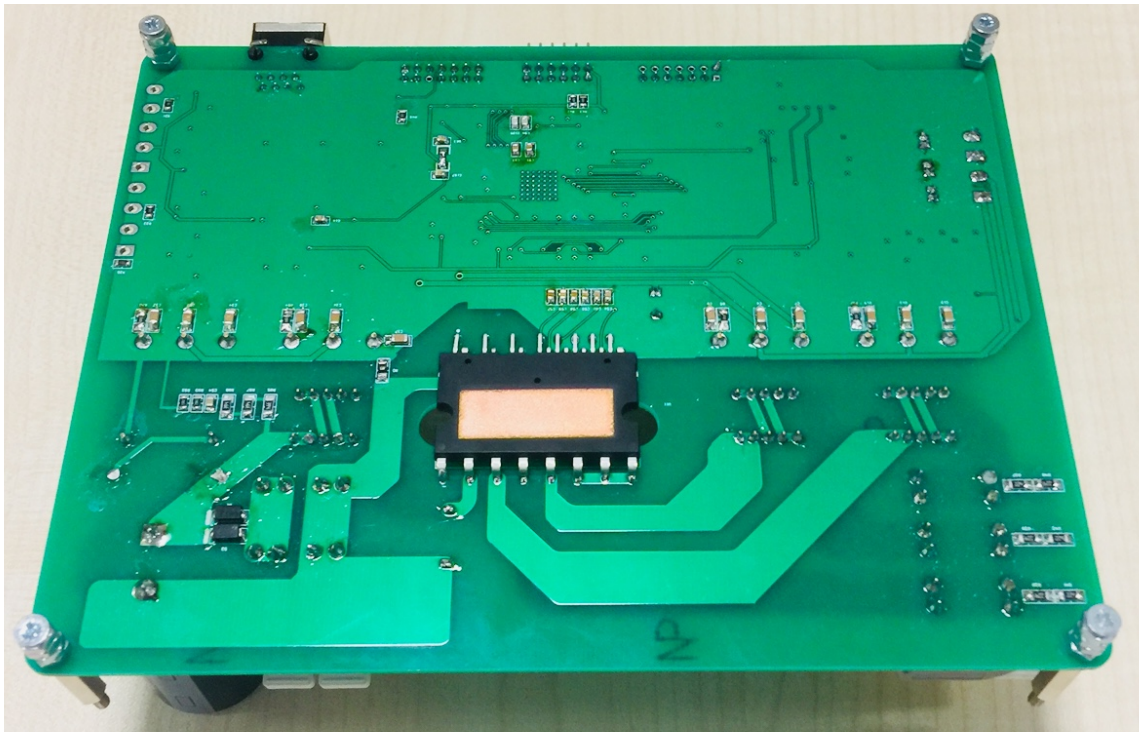


Fig. A.3. PCB layout of the drive system.

The two-layer control board is prototyped as shown in Fig. A.4.



(a) Top layer



(b) Bottom layer

Fig. A.4. Control board prototype.

A.2 Control Algorithm Implementation

The software control algorithms of both BLAC and BLDC drives include one main function and two interrupting service routines (ISRs), i.e. eCAP ISR and ADC ISR. The flow chart of the control algorithm is shown in Fig. A.5. The main function includes the initialization task and a control loop which contains the protection algorithm.

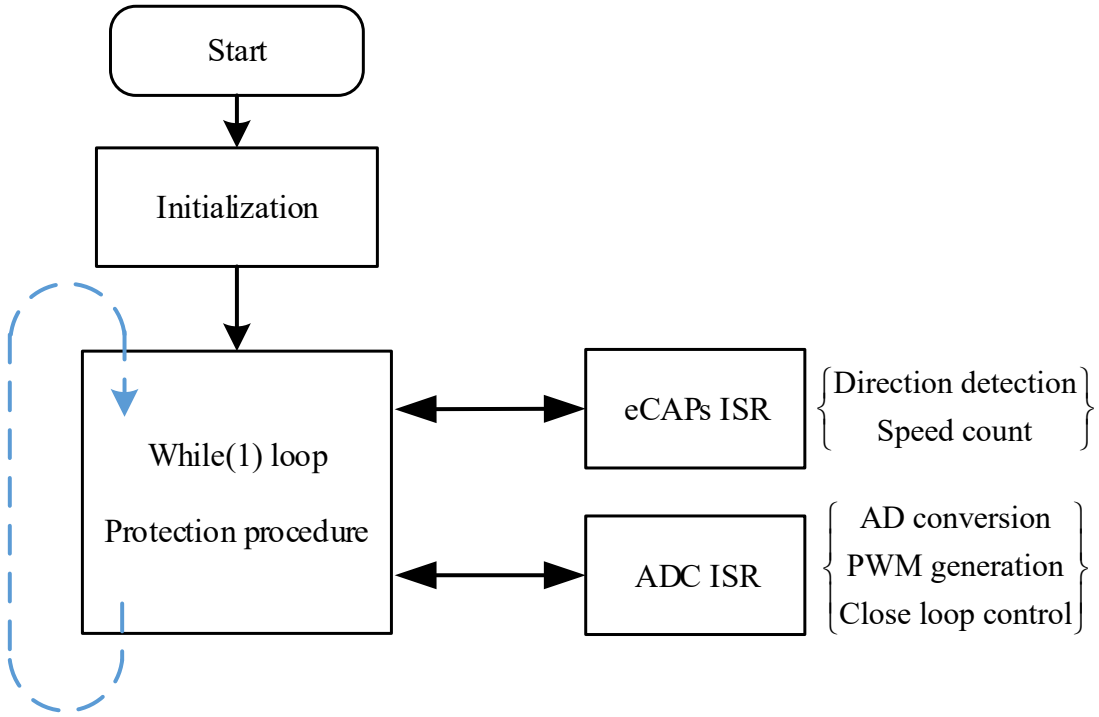


Fig. A.5. Flow chart of control system.

The eCAP ISR and ADC ISR are activated by external Hall signals and internal ePWM counter respectively. eCAP ISR is used to detect the rising and falling edges of Hall signals and thus detecting the direction and calculating the motor speed. ADC ISR is activated every ePWM counter period. The ADC ISR contains AD conversion, PWM generation and close loop control algorithm. The priority of eCAP ISR is set to be higher than that of ADC ISR.

A.2.1 eCAP ISR

Three eCAP modules in the DSP are used to detect both the rising and the falling edges of the Hall signals A, B and C. Continuous mode control is selected so that each eCAP can detect different events. The DSP allows up to four capture events while here in this control system, only two events are needed. The rising edge of Hall signal is captured as Capture Event 1 while the falling edge is captured as Capture Event 2. The capture number is reset every time after

Capture Event 2. The overflow flag output is also enabled for protection. The allocation of DSP pins and eCAP modules are shown in Table A.1 as below.

Table A.1. ALLOCATION OF DSP PINS AND ECAP MODELS

Hall of Phase	A	B	C
Pin No.	72	69	68
eCAP module No.	eCAP3	eCAP2	eCAP1
CPU interrupt No.	4	4	4
PIE interrupt No.	3	2	1

The flow chart of eCAP3 ISR is shown in Fig. A.6 as example.

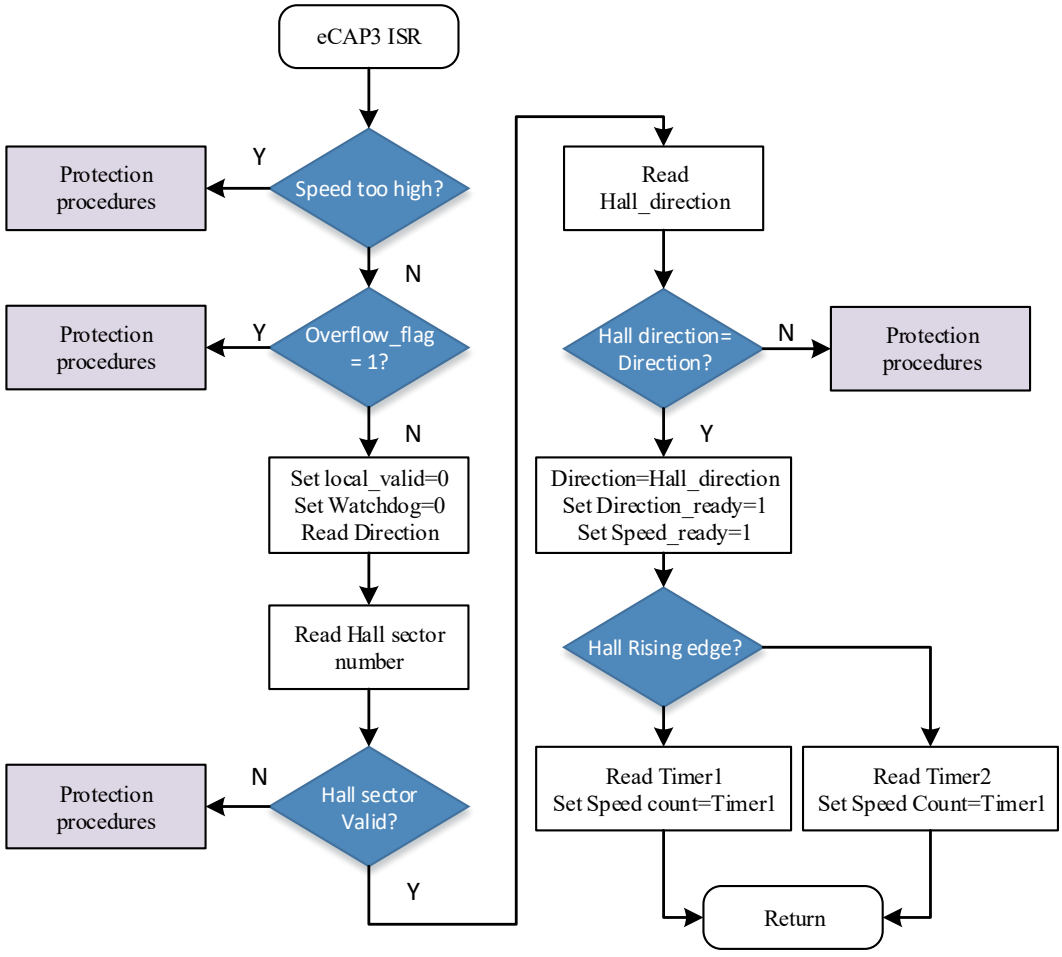


Fig. A.6. Flow chart of eCAP ISR.

The eCAP ISRs are activated by every rising and falling edges of input Hall signals. One eCAP module is used for one input Hall signal. Thus, for each module, the ISR is activated by every 180 electrical degrees. The captured timer counts of all three eCAP modules will be used which means the speed count register can be updated every 60 electrical degrees.

A.2.2 ADC ISR

The ADC ISR is the main part of algorithm, which is activated when the counter of ePWM module is equal to zero. The ADC ISR mainly contains AD conversion, speed calculation, speed regulator and PWM generation. Three ePWM modules, i.e. ePWM5, ePWM3 and ePWM1, are used while only ePWM5 is enabled to activate the interrupt service. The allocation of DSP pins and ePWM modules are shown in Table A.2.

Table A.2. ALLOCATION OF DSP PINS AND EPWM MODELS

Switch	S_1	S_2	S_3	S_4	S_5	S_6
Pin No.	17	18	11	12	5	6
ePWM module No.	ePWM5		ePWM3		ePWM1	
CPU interrupt No.	1		N.A.		N.A.	
PIE interrupt No.	1		N.A.		N.A.	

When the ADC ISR is activated, the signals are detected from ADC pins on the DSP. Simultaneous mode is selected so that signals in both ADC module A and module B can be obtained at the same time. In this control system, the phase current, phase voltage, DC current and DC voltage are detected while the allocation of DSP pins and ADC modules are shown in Table A.3.

Table A.3. ALLOCATION OF DSP PINS AND ADC MODELS

Type of data	I_a	I_c	I_{dc}	U_{dc}	U_a	U_b	U_c
Pin No.	42	46	41	47	49	51	53
ADC module No.	A0	B0	A1	B1	B3	B5	B7

The ADC ISR flow chart of BLAC control is shown in Fig. A.7.

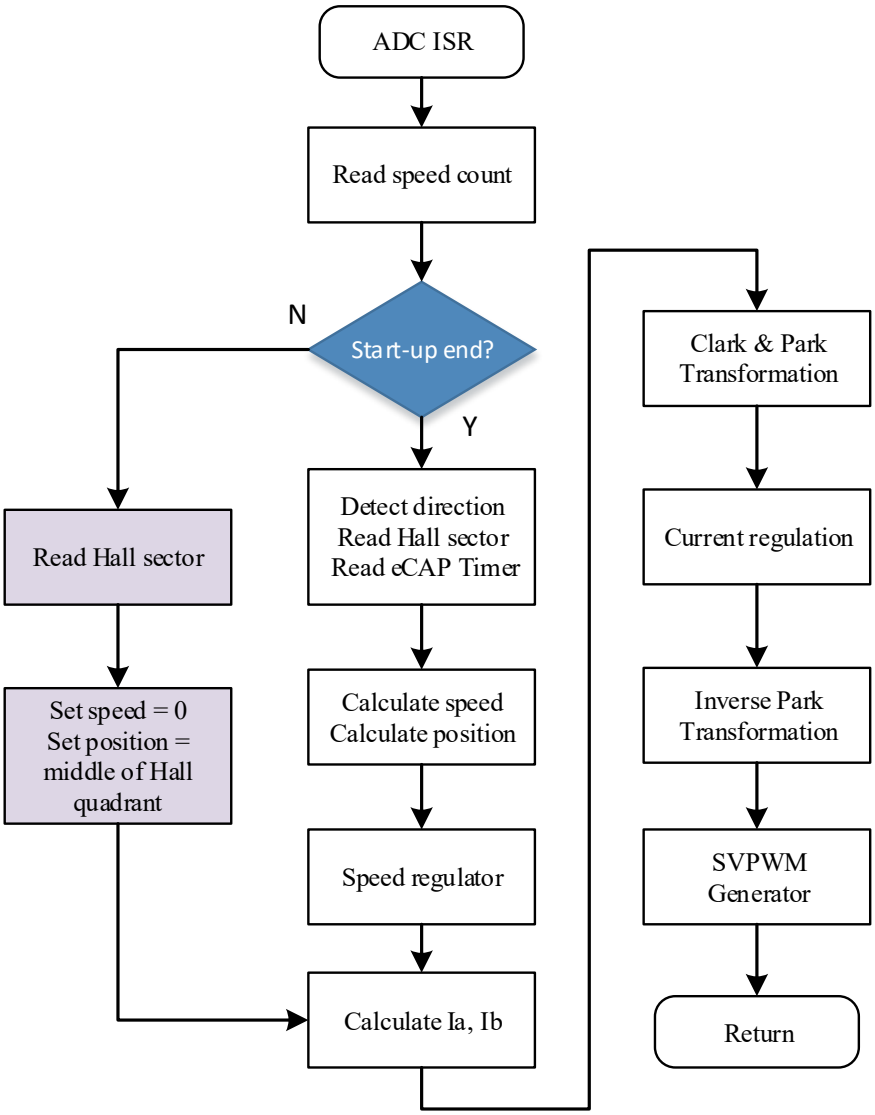


Fig. A.7. ADC ISR flow chart of BLAC control.

For BLAC control, the eCAP timer is read in each interrupt service. Together with the speed count, the absolute position information of the motor is obtained. During start-up process, the position cannot be calculated precisely. Thus, if the motor speed does not reach the pre-set threshold value, the position is set as the middle of Hall quadrant.

The ADC ISR flow chart of BLDC control is shown in Fig. A.8. The eCAP timer is no longer needed when BLDC control is used. Similar to the BLAC drive, a start-up process is also required based on the detected Hall sector.

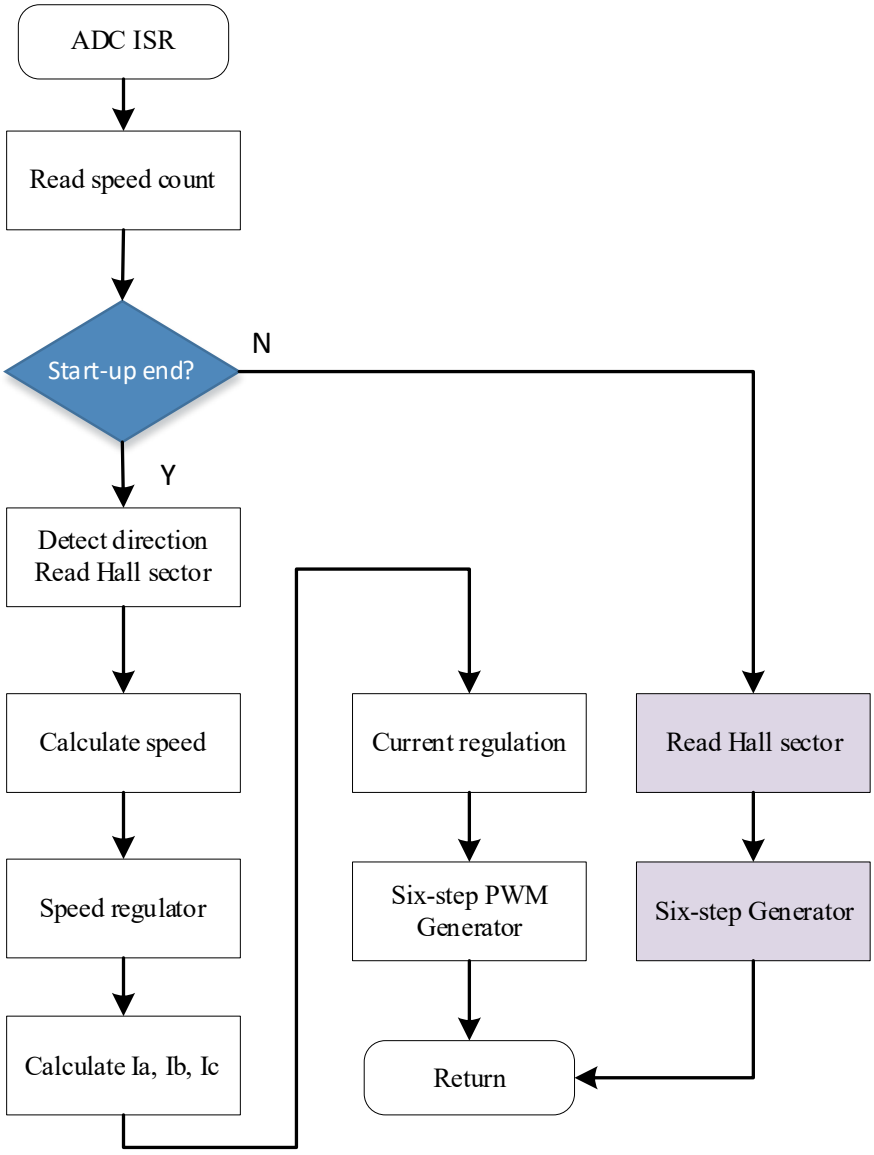


Fig. A.8. ADC ISR flow chart of BLDC control.

A.2.3 Current and Voltage Measurement

As discussed in the previous part, three Hall effect current sensors are used to measure both the phase and DC currents while one Hall effect voltage sensor is placed next to the input port to measure the DC voltage. Since all these components have different input/output connection methods, great attention should be paid to these measurement techniques. Besides, the output signals should also consider the voltage input limitation of DSP.

Current transducer LA25-NP is chosen for current measurement while its working principle is shown in Fig. A.9. This transducer has a maximum primary root mean square (RMS) value of

36A. Since the rated current of the motor is about 5A, the number of primary turns is chosen to be three so that the nominal primary and output currents are 8A and 24mA, respectively.

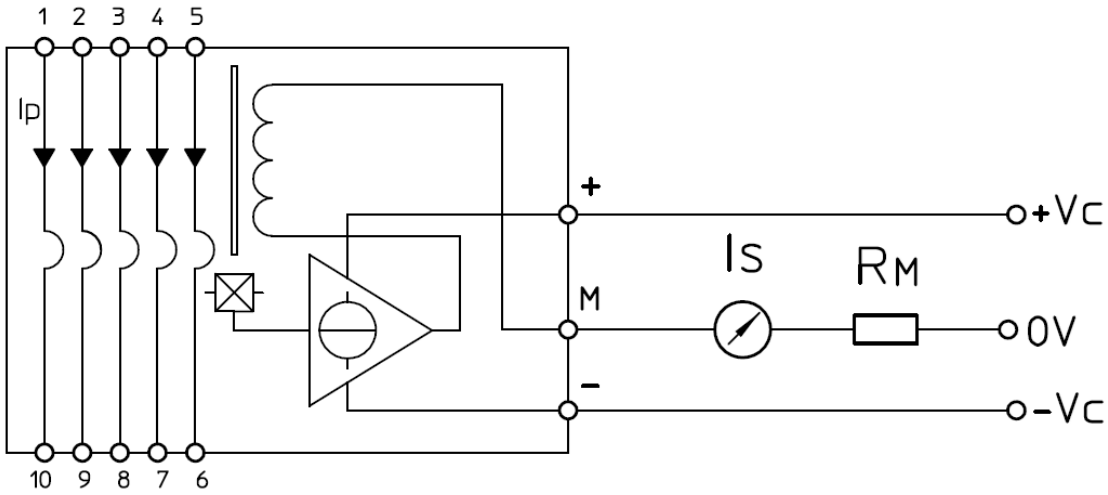


Fig. A.8. Working principle of current sensor LA25-NP.

The connection of LA25-NP is shown in Fig. A.9. The output of current transducer is connected to a resistor R_M of 200Ω. Thus, the nominal primary current and output voltage are 8A and 4.8V.

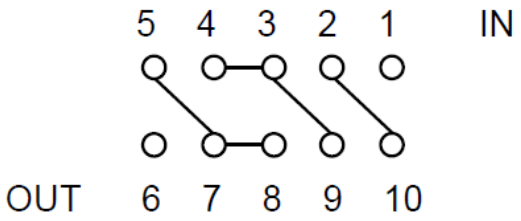


Fig. A.9. Connection of LA25-NP.

Since the ADC modules of DSP has a voltage limitation of 3V, the output voltage is then processed by an amplifier circuit. In summary, the relationship between the primary current and the ADC input voltage can be expressed as

$$V_{adc\_current\_i} = 0.15 I_{current\_i} + 1.65 \quad \text{(A-1)}$$

Voltage transducer LV25 is also used for voltage measurement while its working principle is shown in Fig. A.10. This transducer has nominal primary RMS value of 10mA while its measuring range is between -14mA to 14mA. The primary current is determined by both the input voltage and the external resistor R_1. For voltage measurement, a current proportional to

the measured voltage must be passed through R_1 which is installed in series with primary circuit. In this control system, the value of R_1 is chosen as 20kΩ.

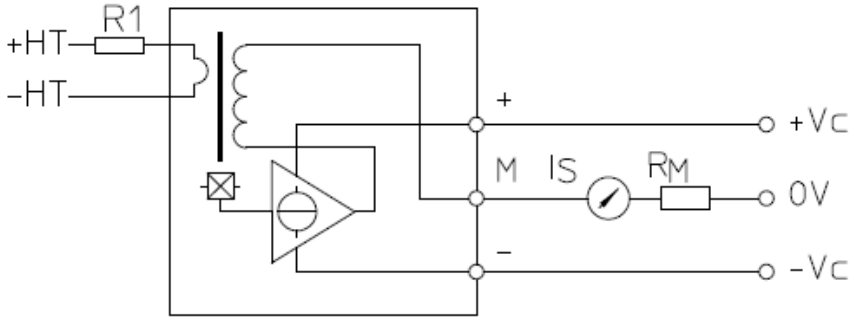


Fig. A.10. Working principle of voltage sensor LV25.

The nominal secondary current is 25mA while the output of voltage transducer is also connected to a resistor R_M of 200Ω. An amplifier circuit which is identical to the current sensing one is used for further signal processing. The relationship between the sensing voltage and the ADC input voltage can be expressed as

$$V_{adc\_Voltage} = \frac{V_{DC}}{160} + 1.65 \qquad \text{(A-2)}$$

The major parameters of the control system are listed in Table A.3

Table A.3 CONTROL SYSTEM PARAMETERS

Parameters	Value
DSP instruction cycle (frequency)	6.67 ns (150M Hz)
PWM frequency	20k Hz
Sampling frequency	20k Hz
ADC resolution	12 bits
ADC conversion time	80 ns

A.3 Tested Motor

The tested motor is a three phase SPM slotted motor. The cross section of the motor is shown in Fig. A.11.

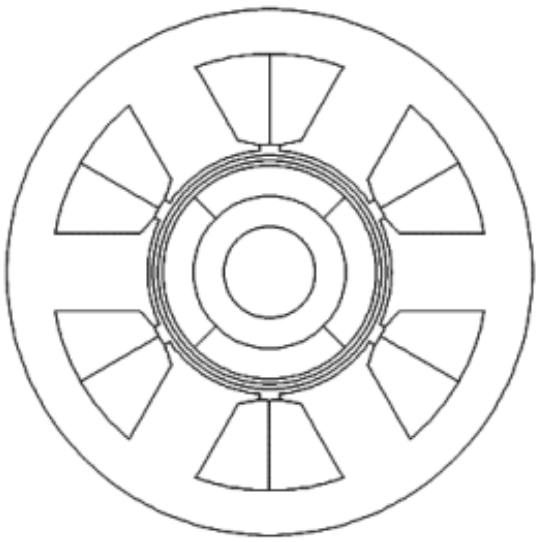


Fig. A.11. Machine cross section.

The stator and rotor of the tested motor are shown in Fig. A.12 and Fig. A.13

Fig. A.12 Stator of the tested motor.

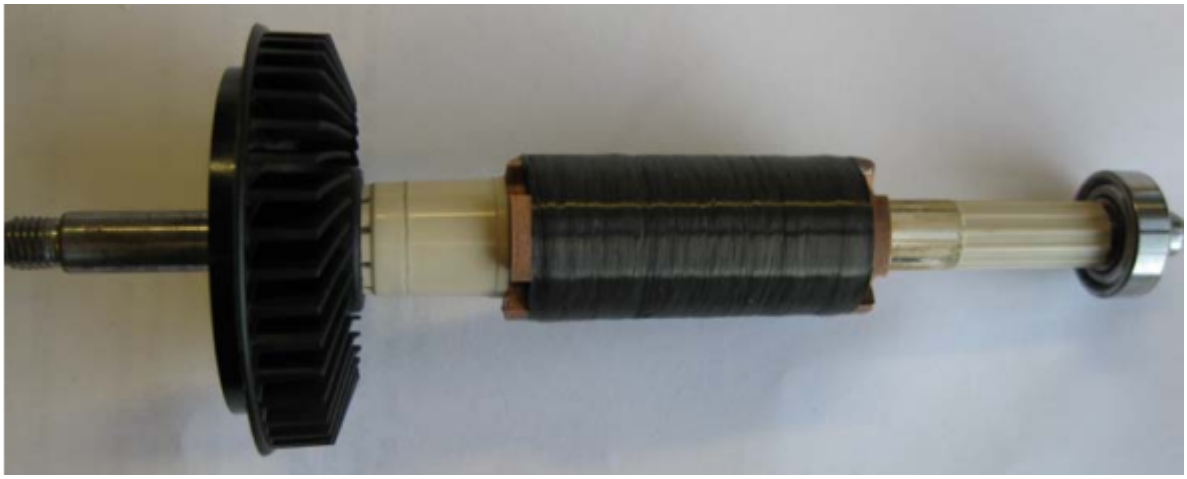


Fig. A.13. Rotor of the tested motor.

The major parameters of the tested motor are listed in Table A.4.

Table A.4 MOTOR PARAMETERS

Parameters	Value
Number of stator slots	6
Number of rotor poles	4
Phase resistance	0.43Ω
Phase self inductance	0.439 mH
Phase mutual inductance	-0.219 mH
Stator outer radius	51.8 mm
Stator inner radius	24mm
Rotor outer radius	21 mm
Core length (stator)	53.1 mm
Core length (rotor)	42 mm
Airgap length	1.5mm