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Droop Control of Parallel-Operated Inverters

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Abstract

Several critical issues for the droop control of parallel-operated inverters are addressed in this thesis, including the power quality, the parallel operation of inverters with different types of output impedance, the power sharing, the voltage and frequency regulation, as well as the current limiting.

The power quality can be improved by properly designing the inverter output impedance, which is often inductive (L-inverter) or resistive (R-inverter). In this thesis, it is designed, for the first time, to be capacitive (C-inverter) to reduce the voltage total harmonic distortion (THD). Then, the C-inverter is developed to be with the virtual resonant impedance (Improved C-inverter) to further improve the power quality. It is well-known that the form of the droop controller is determined by the type of the inverter output impedance. Usually, $P \sim \omega$ and $Q \sim E$ droops are used for L-inverters, while $P \sim E$ and $Q \sim -\omega$ droops are used for R-inverters. To enable the parallel operation of C-inverters, $P \sim -\omega$ and $Q \sim -E$ droops are adopted. After that, to enable the parallel operation of inverters with any type of output impedance having a phase angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad, a universal droop control strategy is presented.

The voltage and frequency regulation along with the current limiting are handled together with the power sharing during the development of the droop controller. To remove the trade-off between the power sharing and the voltage and frequency regulation, a droop control method that adopts the structure of the robust droop controller and utilizes the transient droop characteristic is proposed. To effectively limit the current, while maintaining accurate power sharing, together with tight voltage and frequency regulation, a current droop controller (CDC) is developed. The small signal stability is analysed to theoretically support the development of proposed droop controllers.

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Chapter 1

Introduction

1.1 Motivations

An inverter is an electrical device that converts dc power into ac power. It has been widely used in many energy-related applications, such as uninterrupted power supplies, induction heating, air conditioning, variable-frequency drives, vehicle-to-grid, high-voltage dc transmission, reactive static compensators. Recently, the distributed generations and renewable energy sources, e.g., photovoltaic arrays, variable speed wind turbines, marine turbines, and combined cycle plants, as well as distributed energy storages, e.g., fuel cells, flywheels, hydrogen, supercapacitors and compressed-air energy storage, are becoming increasingly popular (Zhong and Hornik, 2013; DOE; Carrasco et al., 2006). As shown in Figure 1.1, inverters are often operated in parallel to integrate them into the microgrid, which is now a very active research area (Fang et al., 2012). When inverters are connected in parallel, high power and/or low cost applications can be achieved. Besides, the inverter system with parallel modules can provide high reliability by $n+1$ redundancy. In these applications, it is critical to achieve high power quality, accurate load sharing, good voltage and frequency regulation, as well as effective current limiting.

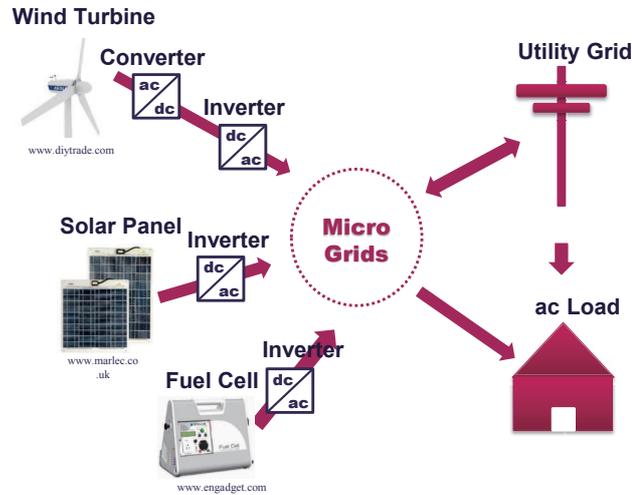


Figure 1.1: Inverters applied in microgrids.

The power quality is often described by parameters and terminologies that express the harmonic pollution, load unbalance and reactive power. The harmonic pollution is often characterized by the the total harmonic distortion (THD), which is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. The lower the THD, the better the power quality. Because of the pulse-width-modulation, the switching, and the nonlinear load, harmonic components inevitably exist in inverter output voltages and currents. They can cause problems, such as overloading of capacitors, unacceptable disturbances on the power supply, unnecessary resonance in the impedance network, degradation of conductors and insulating material in motors and transformers (Lundquist, 2001). The main power quality problem investigated in this thesis is the voltage THD. According to industrial regulations, the voltage THD should be lower than 5% (Hornik and Zhong, 2011; Yousefpoor et al., 2012).

The sharing accuracy has been a main driving force in the research area of parallel inverters for a long time (Li and Kao, 2009; Guerrero et al., 2006b; Lee et al., 2010). Inverters should share loads proportionally according to the ratio of their power ratings. Meanwhile, the magnitude and the frequency of the output voltage should be regulated to meet the demands of loads. The better the voltage regulation, the closer the load could be working to their rated regime. Moreover, the current has to be limited to protect the equipments, especially when a sudden load change or a short-circuit occurs.

1.2 Outline of the Thesis

The thesis is organised as follows. In Chapter 2, the basic principle of the inverter operation is firstly illustrated. Then, existing methods for the improvement of the power quality and droop controllers for the parallel operation of inverters are discussed. After that, the method of the small signal stability analysis is briefly introduced.

In order to improve the power quality, a new type of inverter called the C-inverter has been proposed in Chapter 3. It is achieved via an inductor current feedback through an integrator, of which the time constant is the desired output capacitance. The value of the output capacitance could be optimised so that the THD of the load voltage is minimised. Compared to R-inverters or L-inverters, C-inverters can achieve lower voltage THD.

As the droop control strategy has different forms for inverters with different types of output impedance, a robust droop controller proposed in (Zhong, 2013b) is further developed for C-inverters in Chapter 4. When applied on the parallel-operated C-inverter system, this controller is able to share the load proportionally and accurately, while maintaining good voltage and frequency regulation.

In Chapter 5, the C-inverter proposed in Chapter 3 has been developed to be with the virtual resonant impedance, which is called the Improved C-inverter. It is achieved via a feedback of the inductor current through a transfer function, which is actually the expression of a resonant impedance topology consisting of inductors and capacitors. The parameters of the virtual resonant impedance can be optimised to simultaneously minimise the voltage harmonic components at different specified frequencies. Improved C-inverters are able to achieve lower load voltage THD than C-inverters.

In spite of the development of the droop controller in Chapter 4, the parallel operation of inverters with different types of output impedance is still a challenge, as the droop control strategy is of different forms. However, for large-scale utilization of distributed generations and renewable energy sources, these inverters will inevitably be operated in parallel. In Chapter 6, a universal droop controller has been proposed for inverters with any type of output impedance having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad.

Another challenge is the trade-off between the power sharing and the regulation of the load voltage and the frequency. In Chapter 7, a controller that adopts the structure of the robust droop controller and utilizes the transient droop characteristics has been presented.

It is able to achieve accurate proportional power sharing while maintaining the inverter output amplitude and frequency at the nominal values.

Droop controllers studied in the previous chapters are all about the control of the power. However, even if the power is controlled, the current is still not limited. In Chapter 8, a new droop control method named current droop controller is proposed. It is based on a new current calculation unit, which only needs the angle of the load voltage to obtain the active and reactive currents. These currents are then used as the control variables to limit the current RMS value. To make the controller robust to numerical errors, disturbances, component mismatches and parameter drifts, the structure of the robust droop controller is adopted. It is able to achieve faster response during the load change and is able to better limit the current RMS value at the steady state. Meanwhile, accurate load sharing, good voltage and frequency regulation are maintained.

Finally, in Chapter 9, the main conclusions of the thesis are summarised and further research is proposed.

1.3 Major Contributions

First, the inverter output impedance has been designed for better power quality. Inverters are often with inductive output impedance because of the filter inductor or with resistive output impedance in some low-voltage applications. The general understanding is that R-inverters are better than L-inverters because resistive output impedance makes the compensation of harmonics easier. However, when the inverter output impedance is designed to be capacitive, some special characteristics are revealed. The virtual capacitance can be designed to minimize the voltage harmonic component at a certain harmonic order, or to minimize the voltage THD. Moreover, when it is designed to be the virtual resonant impedance, the parameters could be designed to simultaneously minimise the voltage harmonic components at many different harmonic orders, and thus further minimize the voltage THD.

Secondly, droop controllers are developed for the parallel operation of C-inverters and for inverters with different types of output impedance. It is well known that the droop control strategy has different forms when inverters have different types of output impedance. Thus, after C-inverters are proposed, the robust droop controller proposed in (Zhong, 2013b)

is further developed to enable their parallel operation. After that, in order to enable the parallel operation of inverters with different types of output impedance, a universal droop control principle has been proposed. It has been shown that the robust droop controller for R-inverters actually offers one way to implement this principle. In other words, it is actually a universal droop controller that can be applied to any practical inverter having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad.

Thirdly, a droop controller without voltage and frequency variations has been proposed. A critical merit of the droop controller is to achieve accurate power sharing without communication. However, when the communication is not adopted, droop controllers normally have a trade-off between the power sharing and the regulation of the load voltage and the frequency. To solve this problem, a droop controller adopting the structure of the robust droop controller (Zhong, 2013b) and utilizing the transient droop characteristics (Guerrero et al., 2005) is proposed. This controller can achieve proportional power sharing while maintaining the load voltage and frequency at the nominal values without communication between parallel connected inverters. This means that the voltage drop caused by the inverter output impedance will be automatically compensated.

Fourthly, a current droop controller for current limiting has been presented. With the power droop controllers, the currents are normally not limited when a sudden load change or short-circuit occurs. To handle this problem, the current should be directly controlled instead of the power. A new current calculation unit has been proposed to obtain the active and the reactive currents. It only needs the angle of the load voltage, which is obtained by a PLL block. Then these currents are used as the control variables of the droop controller. The structure of the robust droop controller is adopted to make the controller robust to numerical errors, disturbances, component mismatches and parameter drifts. Compared with the power droop controller, this controller is able to achieve faster response during the load change and is able to limit the current RMS value at the steady state better. It can also achieve accurate load sharing, good voltage and frequency regulation.

1.4 List of Publications

1. Q.-C. Zhong and Y. Zeng, "Control of inverters via a virtual capacitor to achieve capacitive output impedance," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5568–5578, Oct. 2014.
2. Y. Zeng and Q.-C. Zhong, "A droop controller achieving proportional power sharing without output voltage amplitude or frequency deviation," in *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2014, pp. 2322–2327.
3. Q.-C. Zhong and Y. Zeng, "Parallel operation of inverters with different types of output impedance," in *Proc. of 39th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Nov. 2013, pp. 1398–1403.
4. Q.-C. Zhong and Y. Zeng, "Can the output impedance of an inverter be designed capacitive?" in *Proc. of the 37th Annual IEEE Conference of Industrial Electronics (IECON)*, 2011, pp. 1220–1225.
5. Q.-C. Zhong and Y. Zeng, "Universal Droop Control of Inverters with Different Types of Output Impedance", *IEEE Access*, vol. 4, pp. 702–712, 2016.

Chapter 2

Literature Review

2.1 Principle of Inverter Operation

An inverter is an electrical device that converts the dc power into the ac power (Prince, 1925), where Figure 2.1 shows an example.

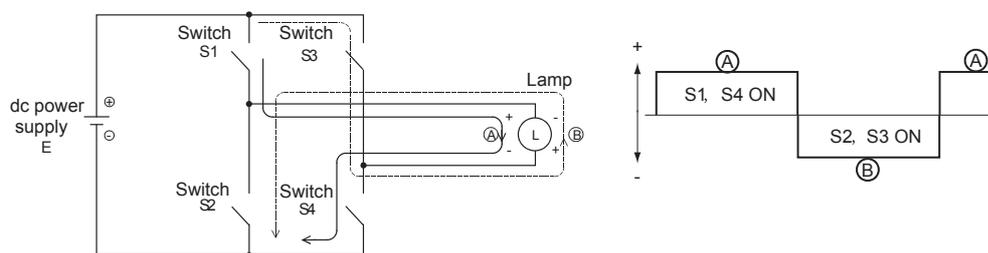


Figure 2.1: The method for dc/ac conversion (Mitsubishi, 2015).

As can be seen, when S1&S4, and S2&S3 are alternatively turned ON and OFF, the current that flows through and the voltage across the load change the direction between A and B, and the dc power is converted to the ac power. According to the type of the dc supply, inverters can be divided into current-source inverters (CSI) (Phillips, 1972) and voltage-source inverters (VSI) (Merritt, 1964; Gumaste and Slemon, 1981). According to the type of the inverter output, inverters can be divided into current-controlled inverters (Nabae et al., 1986) and voltage-controlled inverters (Chen and Chu, 1995). As shown in Figure 2.1, the inverter output voltage waveform can be square wave. It can also be modified square/sine wave, near-sine wave, or multi-level wave (Zhong and Hornik, 2013). Besides, according to the number of output voltage phases, inverters can be divided into

single-phase inverter, three-phase inverter, and multi-phase inverter. This thesis focuses on the control of single-phase voltage-controlled VSI, and the output voltage is expected to be purely sinusoidal with minimal harmonic components.

When S1&S4, and S2&S3 are periodically turned ON and OFF, the inverter output voltage changes its direction periodically. Then, the total time for one cycle is the period of the output voltage, and the inverse of the period is the frequency. Besides, as shown in Figure 2.2, if S1&S4, and S2&S3 are not always ON in the corresponding half cycle, then the average amplitude of the ac inverter output voltage would be lower than the amplitude of the dc power voltage. The shorter the ON period, the lower the average amplitude.

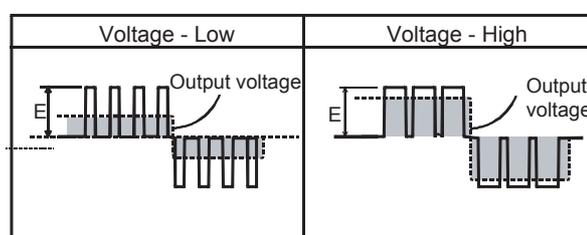


Figure 2.2: The method for voltage regulation (Mitsubishi, 2015).

Thus, by controlling the pulse width, the frequency and amplitude of the inverter output voltage could be controlled. This method is called Pulse Width Modulation (PWM). It has been widely used in the control of switching devices. There are many different PWM techniques (Holmes et al., 2003; Holtz, 1992; Asiminoaei et al., 2008; Holtz, 1994; Wong et al., 2001; Lascu et al., 2007; 2009; Cetin and Ermis, 2009; Zhang et al., 2013b). In order to get a desired sinusoidal voltage, a special modulation method called sinusoidal PWM (SPWM) (Boys and Walton, 1985; Oliveira et al., 2007; Tamyurek, 2013; Narimani et al., 2015) is usually adopted. As shown in Figure 2.3, the desired reference voltage (modulating signal) is firstly compared with a triangular carrier wave, which results in the chopped square waveform (pulses). Note that the modulating signal is usually purely sinusoidal; the carrier frequency, i.e. the switching frequency, is normally much higher than the modulation frequency. According to the averaging theory (Khalil, 2001), as long as the switching frequency is high enough, the average of the pulses over one switching period would be able to well approximate the original signal (Zhong and Hornik, 2013).

Then, the pulses are amplified to control the stage of the switches to generate the in-

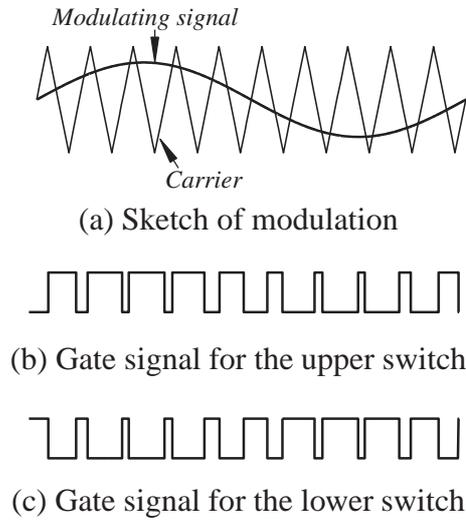


Figure 2.3: SPWM for a single-phase inverter (Zhong and Hornik, 2013).

verter output voltage with the same shape. In order to avoid short-circuit, the upper and the lower switches of the same leg need to be operated in a complementary way. The harmonic components of the generated square wave voltage are mainly located at the multiples of the switching frequency, and could be automatically filtered by the inverter low-pass output filter. The low frequency components of the voltage contain a replica of the modulating signal, which indicates that the fundamental frequency of the output voltage is the same as the reference one (A.M.Gole, 2000). The amplitude of the inverter output voltage can be controlled by the amplitude modulation index, which is the ratio between the modulation amplitude and carrier amplitude. Therefore, the inverter output voltage can be controlled by the modulating signal.

2.2 Power Quality Improvement

Harmonic components that degrade the power quality inevitably exist in the inverter output voltage because of the PWM method, the switching, and the nonlinear load. To improve the power quality, the inverter output filter is normally adopted, the output impedance of the inverter should be carefully designed, and many control schemes have been proposed.

2.2.1 Inverter Output Filter

A filter is often installed between the inverter and the load to filter out the harmonics and to recover the desired voltage. Various filters are available, including passive power filters (PPFs) (Das, 2004; Chang et al., 2006; Hamadi et al., 2010; Illindala and Venkataramanan, 2012; Wu et al., 2013; Yang and Le, 2015), active power filters (APFs) (Asiminoaei et al., 2008; Luo et al., 2009; Vodyakho and Mi, 2009; Bhattacharya et al., 2012; Acuna et al., 2014; Alfonso-Gil et al., 2015) and hybrid APFs (HAPFs) (Flores et al., 2009; Ostroznik et al., 2010; Shuai et al., 2011; Lam et al., 2014). APFs and HAPFs often mitigate some of the disadvantages of passive filters, such as fixed compensation performance and system resonance (Luo et al., 2009). However, from the economic view, PPFs are often regarded as a better choice (Das, 2004). The most commonly used passive inverter filters are LC filters and LCL filters, as shown in Figure 2.4. Here, the equivalent series resistances (ESR) of the inductor and the capacitor, which are usually small values, are ignored. While the LC filter is widely used for the inverter with local load, the LCL filter is widely used for the grid-connected inverter. This thesis focuses on the parallel operation of inverters with local load, which adopts LC filter as the inverter output filter, as shown in Figure 2.4(a).

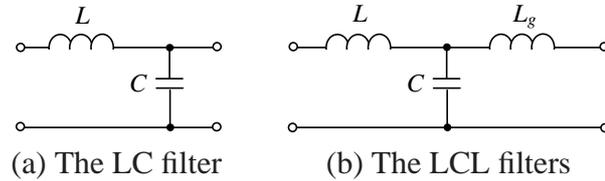


Figure 2.4: The circuit model of the passive power filter.

The cut-off frequency f_c of the LC filter is

$$f_c = \frac{1}{2\pi\sqrt{LC}}. \quad (2.1)$$

It is able to filter out the harmonics located at frequencies higher than f_c . However, it causes a resonance that would magnify the harmonic current components at approximately f_c and could lead the load voltage THD to be high. Thus, f_c should be positioned outside the area where the major current harmonic components locate. Meanwhile, f_c should be much lower than the switching frequency f_{sw} to filter out the switching harmonics. Moreover, it has to be high enough to provide enough bandwidth for the controller. Usually, it can be

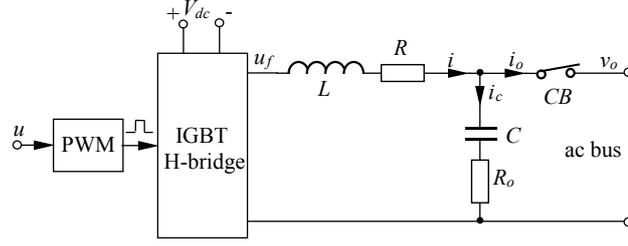
chosen as $\frac{1}{3} \sim \frac{1}{2}$ of f_{sw} (Hatua et al., 2012; Zhong and Hornik, 2013), i.e.,

$$\frac{f_{sw}}{3} \leq f_c \leq \frac{f_{sw}}{2}. \quad (2.2)$$

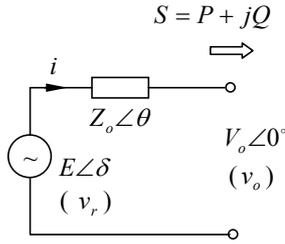
Many approaches have been proposed for passive LC filter design. A systematic and generalised design methodology was proposed for second-order output filters that generates sinusoidal voltages through space-vector modulation (Michels et al., 2006). It provides a methodology to determine the maximum cut-off frequency of the filter that ensures specification of the highest admissible THD in the output voltages. However, this algorithm is complex and only applicable in some limited situations. The impact of the output filter design on both cost and efficiency of the UPS filter was studied by adopting Pareto analysis to obtain the cost-losses trade-off curves (Pasterczyk et al., 2009). However, its models are based on material and thermal analysis and thus rather complex. To achieve lossless damping, an active damping method was proposed, where virtual resistance is multiplied by the individual capacitor currents at the resonant frequency and subtracted from the source voltages (Hatua et al., 2012). Note that the virtual resistor offers an effective way to avoid the trade-off between resonance damping and energy efficiency (Singer, 1991; Dahono et al., 2001). Moreover, cost function of the filter has been defined for the convenience of the filter design (Dewan and Ziogas, 1979; Dewan, 1981b; Kim et al., 2000). In this chapter, some guidelines are given for the selection of the filter inductor and capacitor (Zhong and Zeng, 2011; 2014).

2.2.2 Design of Inverter Output Impedance

Usually, the inverter output impedance is inductive because of the output filter inductor and/or the highly inductive line impedance. In low-voltage applications, the line impedance is predominantly resistive (Li and Kao, 2009). Since control strategies can be used to change the output impedance, it can be easily forced to be resistive (Guerrero et al., 2005; 2004; 2008; 2007; 2006a), resistive-inductive (Yao et al., 2011; Yang et al., 2014; Tao et al., 2015), or of other types (Matas et al., 2010; Kim et al., 2011; He and Li, 2012b; Zhang et al., 2013a; Wang et al., 2014; Tao et al., 2015). It has been pointed out that the inverter output impedance plays an important role in power sharing (Guerrero et al., 2005). In this thesis, it would be designed for improving the power quality.



(a) Descriptive circuit



(b) Simplified model with terminal voltage v_o and terminal current i

Figure 2.5: A model of the single-phase inverter.

Different types of inverter system models are available (Kerkman et al., 1991; Holtz and Quan, 2002; Krutikova et al., 2007; Avelar et al., 2012; Rasheduzzaman et al., 2014; Liu et al., 2015), including experimental, time and frequency domain models. Usually, the frequency domain model is adopted for the convenience of the power quality analysis. Figure 2.5 shows an inverter, which consists of a single-phase H-bridge inverter powered by a dc source, and an LC filter. The control signal u is converted to a PWM signal to drive the H-bridge. According to averaging theory (Khalil, 2001), the average of u_f over a switching period is the same as u , i.e. $u \approx u_f$. Different PWM techniques and the associated switching effect play an important role in inverter design (Neacsu, 2008; Manias et al., 1987; Wu et al., 2011), but from the control point of view the PWM block and the H-bridge can be ignored when designing the controller, see e.g. (Zhong, 2013b; Patel and Agarwal, 2008; Sun, 2011; Matas et al., 2010). In particular, this is true when the switching frequency is high enough.

As shown in Figure 2.5(a), the output impedance of an inverter is defined at the terminal with the load voltage v_o and the filter inductor current i . Then, the inverter can be modelled as shown in Figure 2.5(b) as the series connection of a voltage reference v_r and the output impedance Z_o . This is equivalent to regarding the filter capacitor as a part of the load

(Zhong, 2013b).

According to Figure 2.5(a), ignoring the ESR of the inductor,

$$u_f = sLi + v_o. \quad (2.3)$$

Since the average of u_f over a switching period is approximately the same as u ,

$$v_r = u \approx sLi + v_o \quad (2.4)$$

and

$$v_o \approx v_r - Z_o(s) i \quad (2.5)$$

with

$$Z_o(s) = sL \quad (2.6)$$

where v_r is the reference voltage, $Z_o(s)$ is the output impedance. As can be seen, the output impedance Z_o is inductive when no controller is adopted.

As shown in Figure 2.6, the control strategy could be adopted to change the inverter output impedance to be resistive (Guerrero et al., 2005; 2007; Zhong, 2013b).

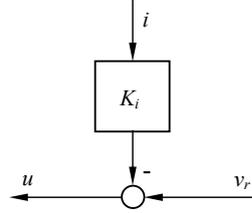


Figure 2.6: A controller to achieve the R-inverter.

According to Figure 2.6,

$$u = v_r - K_i i. \quad (2.7)$$

Then,

$$v_r - K_i i \approx sLi + v_o \quad (2.8)$$

which gives the output impedance $Z_o(s)$

$$Z_o(s) = K_i + sL. \quad (2.9)$$

This is equivalent to connect a virtual resistor K_i in series with the filter inductor L . If K_i is big enough, then the effect of the inductor sL is not significant and the output impedance can be made nearly purely resistive at the fundamental frequency, i.e., roughly

$$Z_o(s) \approx K_i. \quad (2.10)$$

If the effect of K_i is almost the same as the effect of the inductor sL , the output impedance would be resistive and inductive at the fundamental frequency, i.e., roughly

$$Z_o(s) \approx K_i + sL. \quad (2.11)$$

Arguably, the R-inverter is better than the L-inverter (Guerrero et al., 2005; 2004; 2008; 2007; 2006a) because its impedance does not change with the frequency and the effect of nonlinear loads (harmonic current components) on the voltage THD can be compensated more easily. In this thesis, the inverter output impedance would be designed to be capacitive and optimised to minimize the load voltage THD (Zhong and Zeng, 2011; 2014).

2.2.3 Design of Control Schemes

Many control methods have been presented to improve the power quality (Zhan et al., 2006; Mohamed et al., 2012; Khadkikar, 2013; Kumar and Mishra, 2014). Several feedback control schemes, e.g. deadbeat or hysteresis controllers (Timbus et al., 2006; Blaabjerg et al., 2006), have been proposed for inverters to reduce the THD. However, these controllers alone cannot eliminate the periodic distortion caused for example by non-linear loads. To eliminate the periodic distortion, a simple learning control method named repetitive control theory (Hara et al., 1988) is adopted. It is a closed-loop system using the internal model principle (Francis and Wonham, 1975). This system has a large gain at the fundamental and all harmonic frequencies, and thus can handle a large amount of harmonics at the same time. Repetitive control has already been successfully used in many applications to gain very low THD, including grid-connected inverters (Hornik and Zhong, 2011; 2010b) and constant-voltage constant-frequency (CVCF) PWM inverters (Ye et al., 2007; 2006; Wang et al., 2007; Zhang et al., 2008; Chen et al., 2008; Tzou et al., 1999). Many other strategies are also available to obtain low THD in the microgrid voltage (Hornik and Zhong, 2010b;

Weiss et al., 2004) and/or the current sent to and from the grid (Hornik and Zhong, 2010a; 2011; Zhong, 2013a).

For parallel-operated inverters, the power quality problem could be addressed together with the load sharing problem, for example, via injecting a harmonic voltage according to the output harmonic current (Borup et al., 2001) or via introducing a voltage feedback loop (Zhong et al., 2011; Zhong, 2013a). In this thesis, the inverter output impedance is designed to improve the power quality, and the droop controller is developed for accurate load sharing, good voltage and frequency regulation (Zhong and Zeng, 2011; 2014).

2.3 Parallel Operation of Inverters

A key method for the parallel operation of inverters is the droop control (Guerrero et al., 2005; 2007; Barklund et al., 2008; Mohamed and El-Saadany, 2008; Guerrero et al., 2011; Tuladhar et al., 1997; Majumder et al., 2010; Brabandere et al., 2007; Zhong and Weiss, 2011; Guzman et al., 2014), which is able to maintain accurate load sharing, excellent voltage and frequency regulation. It is widely used in conventional power generation systems (Diaz et al., 2010). Its advantage is that no external communication mechanism is needed among the inverters (Tuladhar et al., 1997; Chandorkar et al., 1993). This enables good sharing for linear and/or nonlinear loads (Tuladhar et al., 1997; 2000; Borup et al., 2001; Coelho et al., 2002; Guerrero et al., 2004; 2006a; Hu et al., 2014). In some cases, external communication means are still adopted for load sharing (Chen et al., 2010) and restoring the microgrid voltage and frequency (Guerrero et al., 2009; 2011).

The equal sharing of linear and nonlinear loads were intensively investigated and high accuracy of equal sharing can be achieved (Guerrero et al., 2005; 2007; Borup et al., 2001; Guerrero et al., 2004; 2006a). A control method was presented in (Borup et al., 2001) for equal power sharing of two three-phase power converters with harmonic compensation connected in parallel. A wireless load-sharing controller was proposed in (Guerrero et al., 2007) for islanding parallel inverters in an ac-distributed system. A configuration is proposed in (Shahparasti et al., 2012) for equal sharing of parallel uninterruptible power supplies (UPSs) based on Z-source inverters (ZSIs), which has removed some limitations of the conventional parallel UPSs. Another control strategy achieved equal power sharing

by drooping the virtual flux instead of the load voltage (Hu et al., 2014).

Many control schemes for proportional power sharing were also presented (Tuladhar et al., 2000; He and Li, 2012a; Guzman et al., 2014). A voltage bandwidth droop control was used to share nonlinear loads in (Tuladhar et al., 1997). For accurate proportional load sharing, a small signal injection method was proposed to improve the reactive power sharing accuracy (Tuladhar et al., 2000), which can also be extended to harmonic current sharing. An important contribution was made in (Guerrero et al., 2005; 2004), where a droop controller for inverters with resistive output impedance was proposed for sharing linear and nonlinear loads (Guerrero et al., 2007; 2006a). In (He and Li, 2012a), the reactive power control error was first obtained and then a slow integration term was adopted for reactive power sharing. Besides, in the application of ac microgrids with utility grid connection, centralized control techniques with strong communication among parallel operated inverters were used, such as the master/slave operation (Zhao et al., 2012; Farhadi and Mohammed, 2014). To avoid the communication, a power sharing strategy was presented in (Guzman et al., 2014), which is based on the field-programmable gate array (FPGA) implementation of the adaptive linear neuron with frequency-locked loop (ADALINE&FLL). Besides, a voltage control loop with a direct droop scheme and a power control loop with a complementary inverse droop scheme were implemented for dispatchable sources and nondispatchables ones of the microgrid, respectively (Guzman et al., 2014). However, inverters controlled by the these droop controllers should have the same per-unit output impedance over a wide range of frequencies. To handle this problem, a robust droop controller for R-inverter (Zhong, 2013b), which is robust to numerical errors, disturbances, component mismatches and parameter drifts, was proposed. This controller can achieve accurate power sharing, while maintaining good regulations of the load voltage and the frequency.

The concept of the droop control is from the rotating generators, whose frequency and active power are closely interconnected. As shown in Figure 2.7, when the load torque increases while the prime mover torque remains the same, the rotational speed and directly the frequency will decrease, and vice versa. The droop controller is trying to achieve the frequency reduction with increased load in a controlled and stable manner.

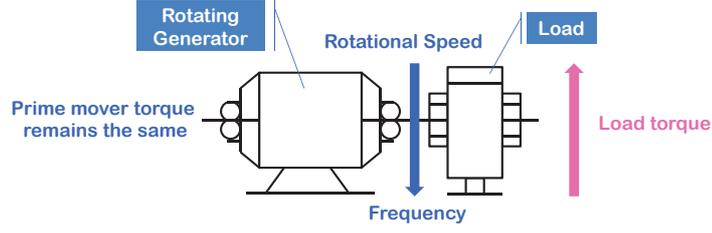


Figure 2.7: The concept of the droop controller.

2.3.1 Conventional Droop Controller

As shown in Figure 2.5(b), an inverter can be modelled as a reference voltage source with an output impedance Z_o . The real power P and the reactive power Q dispatched to the terminal via the output impedance Z_o are

$$P = \left(\frac{EV_o}{Z_o} \cos \delta - \frac{V_o^2}{Z_o} \right) \cos \theta + \frac{EV_o}{Z_o} \sin \delta \sin \theta \quad (2.12)$$

$$Q = \left(\frac{EV_o}{Z_o} \cos \delta - \frac{V_o^2}{Z_o} \right) \sin \theta - \frac{EV_o}{Z_o} \sin \delta \cos \theta \quad (2.13)$$

where δ is the phase difference between the supply and the terminal, θ is the angle of the inverter output impedance, E is the RMS value of the inverter source voltage, V_o is the RMS value of the load voltage v_o .

For L-inverters, $\theta = 90^\circ$. Then

$$P = \frac{EV_o}{Z_o} \sin \delta \quad \text{and} \quad Q = \frac{EV_o}{Z_o} \cos \delta - \frac{V_o^2}{Z_o}.$$

When δ is small,

$$P \approx \frac{EV_o}{Z_o} \delta \quad \text{and} \quad Q \approx \frac{E - V_o}{Z_o} V_o$$

and roughly,

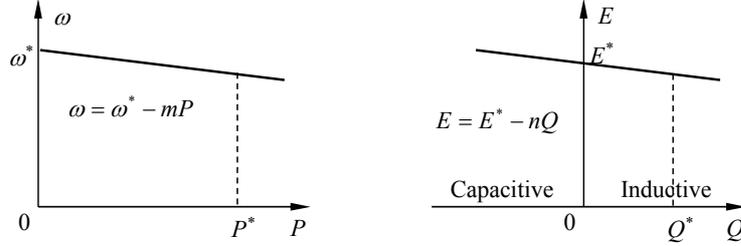
$$P \sim \delta \quad \text{and} \quad Q \sim V_o.$$

Hence, the conventional droop control strategy takes the form

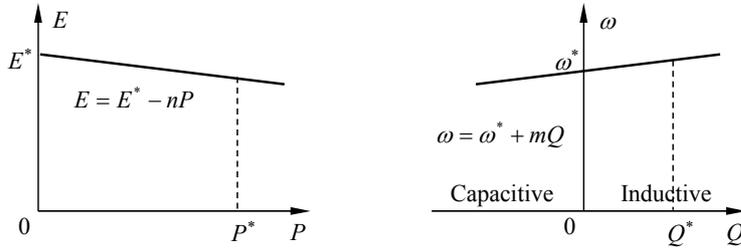
$$E = E^* - nQ \quad (2.14)$$

$$\omega = \omega^* - mP \quad (2.15)$$

where E^* is the rated RMS voltage of the inverter, ω^* and ω are the rated and measured system line frequency, n and m are the droop coefficients. This strategy is sketched in Figure 2.8(a).



(a) For the L-inverter



(b) For the R-inverter

Figure 2.8: Droop controllers for the L-inverter and the R-inverter.

For R-inverters, $\theta = 0^\circ$. Then

$$P = \frac{EV_o}{Z_o} \cos \delta - \frac{V_o^2}{Z_o} \quad \text{and} \quad Q = -\frac{EV_o}{Z_o} \sin \delta.$$

When δ is small,

$$P \approx \frac{E - V_o}{Z_o} V_o \quad \text{and} \quad Q \approx -\frac{EV_o}{Z_o} \delta$$

and, roughly,

$$P \sim V_o \quad \text{and} \quad Q \sim -\delta.$$

Hence, the conventional droop control strategy takes the form

$$E = E^* - nP \tag{2.16}$$

$$\omega = \omega^* + mQ. \tag{2.17}$$

This is sketched in Figure 2.8(b). It is obvious that the droop control strategy has different

forms for L-inverters and R-inverters, and thus would have a different form for C-inverters. In this thesis, the output impedance of the inverter was designed to be capacitive, and the droop controller was further developed for the parallel operation of C-inverters (Zhong and Zeng, 2011; 2014).

2.3.2 Robust Droop Controller

Conventional droop controllers rely on the accurate tuning of the control parameters as there is not a mechanism that is robust against numerical errors, disturbances, component mismatches and parameter drifts, etc. (Zhong, 2013b). These controllers require that all the inverters have the same per-unit output resistance over a wide range of frequencies. A significant breakthrough has been made in (Zhong, 2013b), where a robust droop controller has been proposed to achieve accurate sharing of real power and reactive power at the same time, while maintaining the load voltage and the frequency within the desired range.

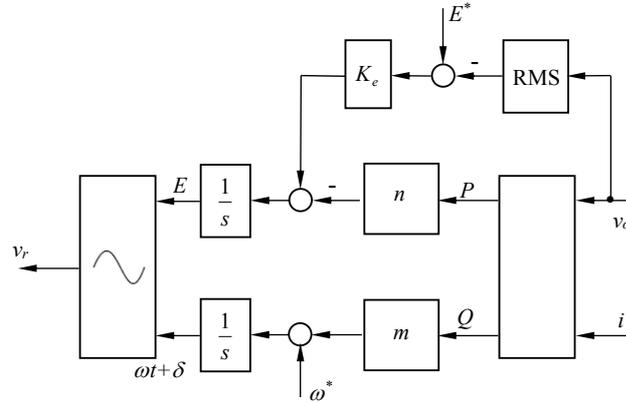


Figure 2.9: The robust droop controller for the R-inverter (Zhong, 2013b).

As shown in Figure 2.9,

$$\dot{E} = K_e(E^* - V_o) - nP \quad (2.18)$$

$$\omega = \omega^* + mQ. \quad (2.19)$$

It is able to share both real power and reactive power accurately even if the per-unit output impedance are not the same and/or there are numerical errors, disturbances and noises

because, at the steady state, there is

$$nP = K_e(E^* - V_o). \quad (2.20)$$

This means

$$nP = \text{constant} \quad (2.21)$$

as long as K_e is the same for all inverters. This guarantees the accurate sharing of active power in proportion to their ratings. As long as the system is stable, which leads to the same frequency, the reactive power can be guaranteed as well (Zhong, 2013b). According to (2.20), the load voltage is

$$V_o = E^* - \frac{nP}{K_e E^*} E^*. \quad (2.22)$$

It can be maintained within the desired range via choosing a big K_e . Hence, the control strategy also has very good capability of voltage regulation.

In this thesis, the structure of the robust droop controller has been adopted to make the proposed controllers robust to the numerical errors, disturbances, component mismatches and parameter drifts.

2.3.3 Droop Controller for R_L -inverters

Another problem is the parallel operation of the inverters with different types of output impedance. As is well known, the droop control strategy has a different form if the inverter has a different type of output impedance and, so far, it is impossible to operate inverters with different types of output impedance, e.g. inductive and capacitive, in parallel. The inverter output impedance in most of the cases (around the fundamental frequency) is inductive but can also be resistive (Guerrero et al., 2005; Zhong, 2013b), capacitive (Zhong and Zeng, 2011; 2014), resistive-inductive (R_L -inverters) (Brabandere et al., 2007; Yao et al., 2011; Bevrani and Shokoochi, 2013; Khan et al., 2013; Sun et al., 2014b; Karimi-Ghartemani, 2015) or resistive-capacitive (R_C -inverters). However, accurate knowledge of the inverter output impedance is usually not available a priori. Therefore, several identification methods have been proposed, such as a fundamental impedance identification method with online real-time calculation capability (Sun et al., 2014a), which requires many transformations. Even if the inverter output impedance is known, as droop controllers change the form when

the inverter output impedance changes the type (Zhong and Hornik, 2013), it would be still impossible to operate these inverters in parallel, which is inevitable for large-scale utilization of distributed generations and renewable energy sources.

In the literature, there have been some attempts to find droop controllers that work for more general cases (Brabandere et al., 2007; Yao et al., 2011; Bevrani and Shokoohi, 2013; Khan et al., 2013; Sun et al., 2014b; Karimi-Ghartemani, 2015). An orthogonal linear rotational transformation matrix was adopted to modify the active power and the reactive power so that, for L-, R- and R_L -inverters, the power angle could be controlled by the modified active power and the inverter voltage could be controlled by the modified reactive power (Brabandere et al., 2007). However, the ratio of R/X needs to be known, where R and X are the resistance and inductance of the inverter output impedance, respectively. A different droop control method added a virtual complex impedance to redesign the angle of the new output impedance to be approximately $\pi/4$, so that the droop form could be fixed (Yao et al., 2011). Nevertheless, the virtual complex impedance needs to be carefully designed. A generalized droop controller (GDC) based on an adaptive neuro-fuzzy interface system (ANFIS) was developed in (Bevrani and Shokoohi, 2013) to handle a wide range of load change scenarios for L-, R- and R_L -microgrids, but resulted in a very complicated structure. Additionally, an active power and reactive power flow controller, which took into account all cases of the R–L relationship, was proposed for three-phase pulse width modulated voltage source inverters (Khan et al., 2013). But the phase shift needs to be obtained for its power transformation. Moreover, an adaptive droop control method was proposed based on the online evaluation of power decoupling matrix (Sun et al., 2014b), which was obtained by the ratio of the variations of the active power and the reactive power under a small perturbation on the voltage magnitude. Recently, an integrated synchronisation and control strategy was proposed to operate single-phase inverters in both grid-connected and stand-alone modes (Karimi-Ghartemani, 2015). However, all these controllers only work for L-, R- and R_L inverters (R_L -controller), but not for C-, or R_C -inverters.

In this thesis, a droop controller for C-, R- and R_C -inverters (R_C -controller) is firstly proposed. Then a universal droop controller that, for the first time, can be applied to L-, R-, C-, R_L - and R_C -inverters has been presented.

2.3.4 Voltage and Frequency Regulation

Despite these improvements, droop controllers have a trade-off between the power sharing and the regulation of the load voltage and frequency. Then, a question arises: Is it possible to have accurate power sharing without any load voltage or frequency deviation? There has been some research on this problem. Excellent equal power sharing is obtained without deviations in either the amplitude or the frequency of the inverter reference voltage in (Guerrero et al., 2005) via adjusting the output impedance value and the load voltage frequency. Nevertheless, it can not avoid the voltage drop caused by the inverter output impedance, which means that the load voltage amplitude still has a deviation from the nominal one. In fact, the larger the load current and the inverter output impedance, the further the load voltage amplitude deviates. Besides, this controller does not work for proportional active power sharing, where the ratio is not 1:1.

To solve these problems, in this thesis, a droop controller adopting the structure of the robust droop controller (Zhong, 2013b) and utilizing the transient droop characteristics (Guerrero et al., 2005) is proposed. This controller can achieve proportional power sharing while maintaining the load voltage amplitude and frequency at the nominal values.

2.3.5 Current Limiting

Most droop controllers take the power as the control variable. However, even if the power is controlled, the current is still not limited when a sudden load change or short-circuit occurs. A possible solution is to directly control the active and the reactive currents (Brabandere et al., 2007; Liu et al., 2012; Khodadoost Arani et al., 2013). In (Brabandere et al., 2007), the active and the reactive currents were obtained according to the voltage difference between the reference ac voltage sources and the grid voltage across virtual complex impedance. A method proposed in (Liu et al., 2012) calculated the active and the reactive currents based on the calculation of active and reactive power. However, both these two methods need the ratio of the real inverter output resistance over reactance. Another method presented in (Khodadoost Arani et al., 2013) used the amplitude and phase angle of the load current, as well as the power angle of the load voltage to obtain the active and the reactive currents. However, two Fourier blocks are needed and all the inverters have to have the same per-unit output resistance.

In this thesis, a current droop controller based on a simple but effective current calculation unit and with the structure of the robust droop controller is proposed. It is able to achieve faster response during the load change and is able to better limit the current RMS value at the steady state. Meanwhile, accurate load sharing, good voltage and frequency regulation are maintained.

2.3.6 Stability Analysis

The dynamic characteristics and the stability of the parallel-operated inverter system can be obtained by the small signal stability analysis after the linearisation around the equilibrium point (Al Haddad et al., 1987; Coelho et al., 2002; Wang and Freitas, 2008; Liu et al., 2009; Wen et al., 2015). Take L-inverters with the conventional droop controller (2.14) and (2.15) for example, and considering the measuring block of the power, around the equilibrium point, the linearised droop controller is

$$\Delta E(s) = -\frac{\omega_f n}{s + \omega_f} \Delta Q(s) \quad (2.23)$$

$$\Delta \omega(s) = -\frac{\omega_f m}{s + \omega_f} \Delta P(s). \quad (2.24)$$

where ω_f is the cut-off frequency of the measuring filter. So in the time domain, these correlations are

$$\Delta \dot{E} = -\omega_f \Delta E - \omega_f n \Delta Q \quad (2.25)$$

$$\Delta \dot{\omega} = -\omega_f \Delta \omega - \omega_f m \Delta P. \quad (2.26)$$

Then, the expressions for active and reactive power (2.12) and (2.13) could be combined with (2.25) and (2.26), and then the characteristic equation for the whole system can be obtained. Based on the characteristic equation, the dynamic characteristics and the system stability could be analysed. In this thesis, the small signal stability analysis has been used to study the stability of the inverter system with proposed droop controllers.

Chapter 3

C-inverters: Inverters with Capacitive Output Impedance

The voltage THD can be improved by investigating the role of the output impedance (Dewan, 1981a; Wu et al., 2012; 2013; Gomez Jorge et al., 2012). Mainstream inverters have inductive output impedance at low frequencies because of the filter inductor. The output impedance of an inverter can also change with the control strategy adopted (Guerrero et al., 2005; 2007; 2004; He and Li, 2012b; Zhang et al., 2013a). The general understanding is that R-inverters are better than L-inverters because resistive output impedance makes the compensation of voltage harmonics easier. Some questions arise immediately. For example, 1) Is it possible to have inverters with capacitive output impedance? 2) If so, what are the advantages, if any? 3) If so, how to achieve parallel operation for such inverters?

In this chapter, a simple but effective control strategy is proposed to design the output impedance of an inverter to be capacitive (Zhong and Zeng, 2011; Zhong and Hornik, 2013). Then, the control parameter (i.e. the output capacitance) is designed to guarantee the stability and, furthermore, optimised to minimise the THD of the load voltage. Moreover, detailed analyses are carried out to provide guidelines for selecting the filter components for C-inverters. Note that the typically-needed voltage loop to track a voltage reference (Guerrero et al., 2007; 2005; Ryan et al., 1997) is not adopted, which reduces the number of control parameters and the complexity of the controller. Simulation and experimental results are presented to demonstrate the feasibility and performance of C-inverters and the guidelines for the component selection. It is shown that, with the same hardware, the lowest voltage THD is obtained when the inverter is designed to be a C-inverter.

Note that the output impedance of an inverter can be defined at different terminals that have different pairs of voltage and current and hence can be different. In this chapter, the output impedance of an inverter is defined at the terminal with the load voltage and the filter inductor current. In order to avoid confusion, the output impedance that takes into account the effect of the filter capacitor and the control strategy is called the overall output impedance. At low frequencies, for which the major voltage harmonics are concerned, the overall output impedance is more or less the same as the output impedance without considering the filter capacitor.

The rest of the chapter is organised as follows. A controller is proposed in Section 3.1 to force the output impedance of an inverter to be capacitive and the stability is analysed. The control parameter is optimised to minimise the voltage THD in Section 3.2 and guidelines for selecting the filter components are provided in Section 3.3. Simulation and experimental results are presented in Section 3.4 and 3.5, followed by conclusions and discussions made in Section 3.6.

3.1 Design of C-inverters

3.1.1 Implementation

The inverter can be modelled as shown in Figure 2.5(b) as the series connection of a voltage reference v_r and the output impedance Z_o . Here, the controller shown in Figure 3.1 is proposed to make the output impedance of an inverter capacitive.

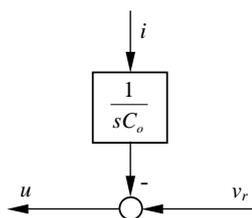


Figure 3.1: A controller to achieve the C-inverter.

The following two equations hold for the closed-loop system consisting of Figure 2.5(a) and Figure 3.1:

$$u = v_r - \frac{1}{sC_o}i \quad \text{and} \quad u_f = (R + sL)i + v_o \quad (3.1)$$

where R is the ESR of the inductor, which is normally small but not exactly 0. Since the average of u_f over a switching period is the same as u , there is (approximately)

$$v_r - \frac{1}{sC_o}i = (R + sL)i + v_o \quad (3.2)$$

which leads to

$$v_o = v_r - Z_o(s) \cdot i \quad (3.3)$$

with the output impedance $Z_o(s)$ given by

$$Z_o(s) = R + sL + \frac{1}{sC_o}. \quad (3.4)$$

As a result, the integrator block $\frac{1}{sC_o}$ is added virtually to the original output impedance of the inverter. This is equivalent to connecting a virtual capacitor C_o (inside the inverter) in series with the filter inductor L . It is worth noting that the original filter capacitor C is still required. Although the virtual capacitance introduced by the feedback changes the output impedance within the bandwidth of the controller, the switching noises are often far beyond the reach of this control and an LC filter is still needed to suppress switching noises. The impact of the control strategy is on the change of the inverter dynamics, with some practical implications discussed in the rest of this section.

If the capacitor C_o is chosen small enough, the effect of the inductor ($R + sL$) is not significant and the output impedance can be made nearly purely capacitive around the fundamental frequency, i.e., roughly

$$Z_o(s) \approx \frac{1}{sC_o}. \quad (3.5)$$

Hence, the virtual capacitor C_o resonates with the filter inductor L at a frequency higher than the fundamental frequency, which is able to reduce the harmonic voltage dropped on the filter inductor caused by the current harmonics. This allows C-inverters to achieve better voltage quality than R- and L- inverters without additional hardware cost.

3.1.2 Stability of the Current Loop

When the controller is implemented digitally, the effect of computation and PWM conversion can be approximated by a one-step delay e^{-sT_s} , where T_s is the sampling period.

Hence, the approximate block diagram of the current loop can be derived as shown in Figure 3.2(a). The corresponding open-loop transfer function is

$$L(s) = \frac{1}{sC_o} \frac{1}{sL + R} e^{-sT_s} \quad (3.6)$$

which has a pole at $s = 0$ but does not have any unstable poles in the right-half-plane of the s -domain. A typical Nyquist plot of such systems is shown in Figure 3.2(b). In order to make sure that the system is stable, according to the well-known Nyquist theorem, the plot should not encircle the critical point $(-1, 0)$. Assume that the plot crosses the real axis for the first time at the frequency ω_0 , then ω_0 satisfies

$$-\frac{\pi}{2} - \text{atan} \frac{\omega_0 L}{R} - \omega_0 T_s = -\pi. \quad (3.7)$$

In other words, ω_0 can be found as the first positive number from 0 that satisfies

$$\frac{R}{\omega_0 L} = \tan(\omega_0 T_s). \quad (3.8)$$

At this frequency, the loop gain $\frac{1}{\omega_0 C_o \sqrt{\omega_0^2 L^2 + R^2}}$ should be less than 1. In other words, the loop is stable if

$$\frac{1}{C_o} < \omega_0 \sqrt{\omega_0^2 L^2 + R^2}. \quad (3.9)$$

It can be easily seen that

$$0 < \omega_0 < \frac{\pi}{2T_s}. \quad (3.10)$$

Hence, the current loop is stable if

$$\frac{1}{C_o} < \frac{\pi}{2T_s} \sqrt{\left(\frac{\pi L}{2T_s}\right)^2 + R^2} \quad (3.11)$$

of which the right-hand side is about $(\frac{\pi}{2T_s})^2 L$ for small $R \approx 0$. In other words, the loop is stable if the capacitance C_o or the sampling frequency $f_s = \frac{1}{T_s}$ is chosen large enough so that the sampling frequency f_s is larger than four times the resonant frequency $\frac{1}{2\pi\sqrt{LC_o}}$ with L , which can be easily met without any problem. Note that R is not exactly zero in reality, which helps maintain the stability of the loop.

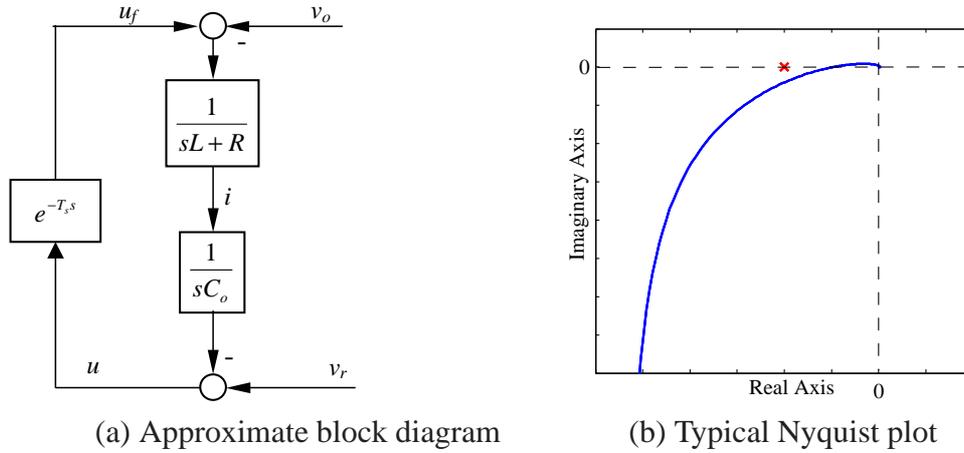


Figure 3.2: The current loop.

3.1.3 DC Offset in the System

Because of the presence of the integrator $\frac{1}{sC_o}$, any dc offset in the current i , e.g. that caused by the conversion process or faults in the system, would lead to a dc offset in the load voltage. To avoid this problem, some simple mechanisms can be adopted. For example, the integrator $\frac{1}{sC_o}$ can be reset when the inductor current passes zero if the offset exceeds a given level. Alternatively, the integrator $\frac{1}{sC_o}$ can be slightly modified as $\frac{1}{sC_o + \varepsilon}$ with a negligible positive number $\varepsilon \approx 0$. This is equivalent to putting a large resistor $\frac{1}{\varepsilon}$ in parallel with C_o , which does not change the performance at non-dc frequencies.

3.2 Optimisation of the Voltage Quality

Voltage harmonics mainly come from two sources: the inverter because of the pulse-width-modulation, the switching, and the non-linear loads/grid (Zhong and Hornik, 2013). Even when a purely sinusoidal voltage supply is provided, non-linear loads will generate harmonic currents, which then cause harmonic voltages because of the inverter output impedance. According to (3.3), in order to obtain low THD for v_o , there are two options: one is to make sure that the reference voltage v_r is able to provide the right amount of harmonic voltages to compensate the harmonic voltage dropped on the output impedance, and the other is to keep v_r clean and maintain a small output impedance Z_o over the range of the major harmonic current components. The first option has been widely investigated in the literature, e.g. by using the repetitive control strategy (Hornik and Zhong, 2011; Tzou

et al., 1999; Hornik and Zhong, 2010b; Chen et al., 2008; Garcia-Cerrada et al., 2007; Zhou and Wang, 2003; Zhou et al., 2009; Costa-Castello et al., 2004; Escobar et al., 2008) or by harmonics injection (Borup et al., 2001). However, the second option has not been fully explored and will be studied in details in this chapter. Strictly speaking, the second option should lead to a small output impedance but this fact has not been well understood.

Assume that the output current of the inverter is

$$i = \sqrt{2} \sum_{h=1}^{\infty} I_h \sin(h\omega t + \phi_h) \quad (3.12)$$

where ω is the system frequency. Then the amplitude of the h -th harmonic voltage dropped on the output impedance is $\sqrt{2} I_h |Z_o(jh\omega)|$. Moreover, assume that the voltage reference v_r is clean and sinusoidal and is described as

$$v_r = \sqrt{2} E \sin(\omega t + \delta). \quad (3.13)$$

Then the fundamental component of the load voltage is

$$v_1 = \sqrt{2} E \sin(\omega t + \delta) - \sqrt{2} I_1 |Z_o(j\omega)| \sin(\omega t + \phi_1 + \theta) \quad (3.14)$$

$$= \sqrt{2} V_1 \sin(\omega t + \beta) \quad (3.15)$$

with

$$V_1 = \sqrt{E^2 + I_1^2 |Z_o(j\omega)|^2 - 2EI_1 |Z_o(j\omega)| \cos(\phi_1 + \theta - \delta)} \quad (3.16)$$

$$\beta = \arctan\left(\frac{\omega |Z_o(j\omega)| \sin(\phi_1 + \theta - \delta)}{I_1 |Z_o(j\omega)| \cos(\phi_1 + \theta - \delta) - E}\right). \quad (3.17)$$

The sum of all harmonic components in the load voltage is

$$v_H = \sqrt{2} \sum_{h=2}^{\infty} I_h |Z_o(jh\omega)| \sin(h\omega t + \phi_h + \angle Z_o(jh\omega)). \quad (3.18)$$

It is clear that v_1 and v_H do not affect each other. v_1 is determined by the clean reference voltage, the fundamental current and the output impedance at the fundamental frequency. v_H is determined by the harmonic current components and the output impedance at the harmonic frequencies.

According to the definition of THD, the THD of the load voltage is

$$\text{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2 |Z_o(jh\omega)|^2}}{V_1} \times 100\%. \quad (3.19)$$

Hence, the THD is mainly affected by the output impedance at harmonic frequencies. As a result, it is feasible to optimise the design of the output impedance at harmonic frequencies to minimise the THD of the load voltage.

For the C-inverter designed in the previous section, according to (5.3), there is

$$|Z_o(jh\omega^*)|^2 = R^2 + (h\omega^*L - \frac{1}{h\omega^*C_o})^2 \quad (3.20)$$

where ω^* is the rated angular system frequency. In order to minimise the THD of the load voltage, the virtual capacitor C_o should be chosen to minimise

$$\sum_{h=2}^{\infty} I_h^2 |Z_o(jh\omega^*)|^2 \quad (3.21)$$

because the fundamental component V_1 can be assumed to be almost constant. This is equivalent to

$$\min_{C_o} \sum_{h=2}^{\infty} i_{1h}^2 (h\omega^*L - \frac{1}{h\omega^*C_o})^2 \quad (3.22)$$

where $i_{1h} = \frac{I_h}{I_1}$ is the normalised h -th harmonic current I_h with respect to the fundamental current I_1 . Depending on the distribution of the harmonic current components, different strategies can be obtained.

Assume that the harmonic current is negligible for the harmonics higher than the N -th order (with an odd number N). Then C_o can be found via solving (3.22). Define

$$f(C_o) = \sum_{h=2}^N i_{1h}^2 (h\omega^*L - \frac{1}{h\omega^*C_o})^2. \quad (3.23)$$

Then C_o needs to satisfy

$$\frac{df(C_o)}{dC_o} = 2\sum_{h=2}^N i_{1h}^2 (h\omega^*L - \frac{1}{h\omega^*C_o}) \frac{1}{h\omega^*C_o^2} = 0 \quad (3.24)$$

which is equivalent to

$$\sum_{h=2}^N i_{1h}^2 (L - \frac{1}{(h\omega^*)^2 C_o}) = 0. \quad (3.25)$$

Hence,

$$\sum_{h=2}^N i_{1h}^2 L = \frac{1}{(\omega^*)^2 C_o} \sum_{h=2}^N \frac{i_{1h}^2}{h^2} \quad (3.26)$$

and the optimal capacitance can be solved as

$$C_o = \frac{1}{(\omega^*)^2 L} \frac{\sum_{h=2}^N \frac{i_{1h}^2}{h^2}}{\sum_{h=2}^N i_{1h}^2} \quad (3.27)$$

which is applicable for any current i with a known harmonic profile. The corresponding $f(C_o)$ is

$$f_{min}(C_o) = (\omega^* L)^2 \sum_{h=2}^N i_{1h}^2 \left(h - \frac{1}{h} \frac{\sum_{h=2}^N i_{1h}^2}{\sum_{h=2}^N \frac{i_{1h}^2}{h^2}} \right)^2. \quad (3.28)$$

Hence, the THD of v_o is in proportion to the inductance L of the inverter LC filter. A small L does not only reduce the cost, size, weight and volume of the inductor but also improves the voltage quality. However, a small L leads to a high $\frac{di}{dt}$ for the switches and large current ripples. See the guidelines of selecting the components in the next section for details. Moreover, since $\frac{1}{C_o} \sim L$, a small L leads to a small gain for the integrator, which is good for the stability of the current loop.

If the distribution of the harmonic components is not known, then it can be assumed that the even harmonics are 0, which is normally the case, and the odd harmonics are equally distributed. As a result, the optimal C_o can be chosen, according to (3.27), as

$$C_o = \frac{1}{(\omega^*)^2 L} \frac{\sum_{h=3,5,7,\dots,N} \frac{1}{h^2}}{(N-1)/2}. \quad (3.29)$$

This can be written as

$$C_o = \frac{1}{(\omega^*)^2 L} \frac{1}{(N-1)/2} \left(\frac{1}{3^2} + \frac{1}{5^2} + \dots + \frac{1}{N^2} \right) \quad (3.30)$$

where $(N-1)/2$ is the number of terms in the summation. The corresponding $f(C_o)$ is

$$f_{min}(C_o) = (\omega^* L)^2 \sum_{h=3,5,7,\dots,N} \left(h - \frac{1}{h} \frac{(N-1)/2}{\sum_{h=3,5,7,\dots,N} \frac{1}{h^2}} \right)^2. \quad (3.31)$$

If a single h -th harmonic component is concerned, then the optimal C_o is

$$C_o = \frac{1}{(h\omega^*)^2 L}. \quad (3.32)$$

This forces the impedance at the h -th harmonic frequency close to 0 and hence no voltage at this frequency is caused, assuming $R = 0$. According to the stability analysis carried out in the previous section, the current loop is stable in this case if $(h\omega^*)^2 L < (\frac{\pi}{2T_s})^2 L$, or in other words if $f_s > 4hf^*$, where $f^* = \frac{\omega^*}{2\pi}$ is the rated system frequency.

3.2.1 Case I: To Minimise the 3rd and 5th Harmonic Components

In most cases, it is enough to consider the 3rd and 5th harmonics only. This gives the optimal capacitance

$$C_o = \frac{17}{225(\omega^*)^2 L}. \quad (3.33)$$

As a result, the output impedance is

$$Z_o(j\omega) = R + j\omega^* L \left(\frac{\omega}{\omega^*} - \frac{225}{17} \frac{\omega^*}{\omega} \right). \quad (3.34)$$

The gain factor $\frac{\omega}{\omega^*} - \frac{225}{17} \frac{\omega^*}{\omega}$ of the imaginary part with respect to the normalised frequency $\frac{\omega}{\omega^*}$ is shown in Figure 3.3. It changes from negative to positive at approximately $\frac{\omega}{\omega^*} = 3.638$. At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j \frac{208}{17} \omega^* L \approx -j12.23 \omega^* L. \quad (3.35)$$

It is nearly purely capacitive as expected because R is normally smaller than $\omega^* L$.

3.2.2 Case II: To Minimise the 3rd Harmonic Component

In this case, the optimal C_o is

$$C_o = \frac{1}{(3\omega^*)^2 L} \quad (3.36)$$

and the corresponding impedance is

$$Z_o(j\omega) = R + j\omega^* L \left(\frac{\omega}{\omega^*} - \frac{9\omega^*}{\omega} \right). \quad (3.37)$$

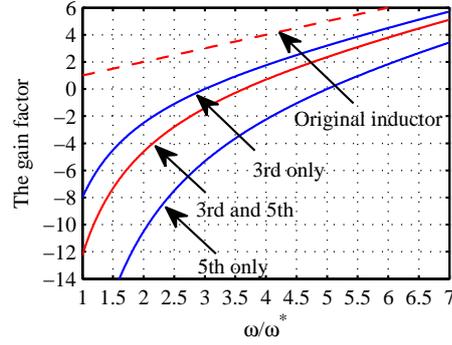


Figure 3.3: The gain factors to meet different criteria.

The gain factor $\frac{\omega}{\omega^*} - \frac{9\omega^*}{\omega}$ of the imaginary part with respect to the normalised frequency $\frac{\omega}{\omega^*}$ is also shown in Figure 3.3. It changes from negative to positive at $\omega = 3\omega^*$. At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j8\omega^*L \approx -j8\omega^*L \quad (3.38)$$

which is nearly purely capacitive as well.

3.2.3 Case III: To Minimise the 5th Harmonic Component

In this case, the optimal C_o is

$$C_o = \frac{1}{(5\omega^*)^2L} \quad (3.39)$$

and the corresponding impedance is

$$Z_o(j\omega) = R + j\omega^*L\left(\frac{\omega}{\omega^*} - \frac{25\omega^*}{\omega}\right). \quad (3.40)$$

The gain factor $\frac{\omega}{\omega^*} - \frac{25\omega^*}{\omega}$ of the imaginary part with respect to the normalised frequency $\frac{\omega}{\omega^*}$ is also shown in Figure 3.3. It changes from negative to positive at $\omega = 5\omega^*$. At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j24\omega^*L \approx -j24\omega^*L. \quad (3.41)$$

This is nearly purely capacitive as well.

3.3 Component Selection

3.3.1 Selection of the Filter Inductor L

As discovered in the previous section, the smaller the filter inductor, the smaller the output impedance and better the voltage quality. Thus, it is better to have a small output inductor than a big one. This leaves the selection of the filter inductor to meet the requirement on the allowed current ripples only. According to (Wu et al., 2012), it is recommended that the current ripples should satisfy

$$0.15 \leq \frac{\Delta I}{I_{ref}} \leq 0.4 \quad (3.42)$$

with

$$\Delta I = \frac{U_{dc}}{4Lf_s} \quad (3.43)$$

where ΔI is the inductor current ripple and I_{ref} is the rated peak current at the fundamental frequency. Thus, the inductor should be chosen to satisfy

$$\frac{5U_{dc}}{8f_s I_{ref}} \leq L \leq \frac{5U_{dc}}{3f_s I_{ref}}. \quad (3.44)$$

This could be applied to analyse the impact on the dc-bus voltage. For example, assume that L is selected to achieve the maximum current ripple of $0.4I_{ref}$. Moreover, . assume that the peak of the h -th harmonic current reaches 50% of I_{ref} . Then the voltage drop of the h -th harmonic current on the inductor is $h\omega^* \frac{5U_{dc}}{8f_s I_{ref}} \times \frac{I_{ref}}{2} = \frac{5h\omega^*}{16f_s} U_{dc}$. In other words, the maximum increase of the required dc bus voltage is $\frac{5h\omega^*}{16f_s} \times 100\%$. For $h = 5$, $f_s = 10$ kHz and $\omega^* = 100\pi$ rad/sec, this is 4.9% so it is not demanding at all and there is no need to take any special action when determining the dc bus voltage.

3.3.2 Selection of the Filter Capacitor C

The main function of the LC filter is to attenuate the harmonics generated by the PWM conversion and the H-bridge via re-producing the control signal u , especially the harmonics around the switching frequency f_s . When there is no load, the transfer function between u_f and v_o is

$$H(s) = \frac{1}{s^2LC + 1}. \quad (3.45)$$

Indeed, the virtual capacitor C_o does not change the role of the LC filter in suppressing the switching noises because the actual output voltage u_f generated by the inverter is still passed through the LC filter. The cut-off frequency f_c can be found from

$$|H(j2\pi f_c)| = \frac{1}{|1 - (2\pi f_c)^2 LC|} = \frac{1}{\sqrt{2}} \quad (3.46)$$

as

$$f_c = \frac{1}{2\pi\sqrt{LC}} \sqrt{\sqrt{2} + 1} \quad (3.47)$$

which is about 1.5 times of the resonant frequency $\frac{1}{2\pi\sqrt{LC}}$. Since it is very close to the resonant frequency, it is reasonable to use the resonant frequency when selecting the components. The overall output impedance $Z(s)$ after taking into account the filter capacitor:

$$Z(s) = \frac{Z_o(s) \frac{1}{sC}}{Z_o(s) + \frac{1}{sC}} = \frac{Z_o(s)}{sCZ_o(s) + 1}. \quad (3.48)$$

At low frequencies, one has

$$Z(s) \approx Z_o(s) = R + sL + \frac{1}{sC_o} \quad (3.49)$$

and at high frequencies,

$$Z(s) \approx \frac{1}{sC}. \quad (3.50)$$

This actually verifies that the definition of the output impedance Z_o without considering the filter capacitor C does not materially affect the analysis at low frequencies. Defining the output impedance at the terminal with the load voltage and the filter inductor current is simply to facilitate the presentation.

For conventional inverters, which are mainly L-inverters, $Z(s)$ is inductive at low frequencies. Hence, the overall output impedance $Z(s)$ changes its type from inductive to capacitive at the resonant frequency. However, according to (5.26), the overall output impedance $Z(s)$ for the C-inverters designed above is

$$Z(s) = \frac{sL + R + \frac{1}{sC_o}}{s^2 LC + sCR + \frac{C}{C_o} + 1}. \quad (3.51)$$

It is capacitive at both low frequencies ($\frac{1}{sC_o}$) and high frequencies ($\frac{1}{sC}$). In order to bet-

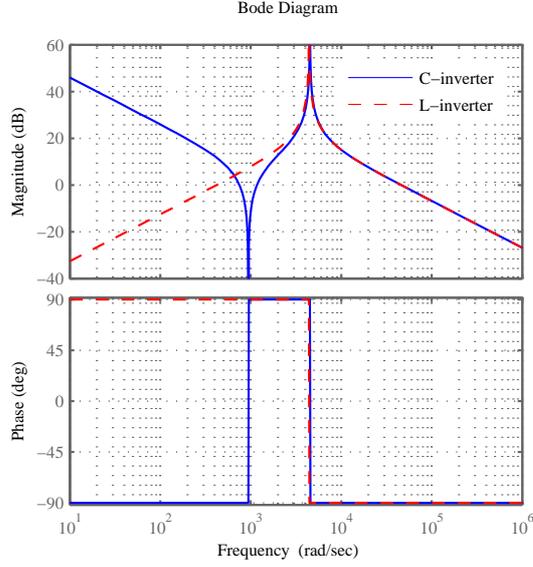


Figure 3.4: The overall output impedance of an L-inverter and a C-inverter after taking into account the filter capacitor C .

ter demonstrate this, the Bode plots of the overall output impedance of typical L- and C-inverters are shown in Figure 3.4. This figure is obtained with the parameters of the experiment given in Section 3.5, and C_o is set to reduce the 3rd load voltage harmonic component. The output impedance of the C-inverter is capacitive over a wide range of both low and high frequencies and is inductive only over a small range of mid-frequencies. There is a series resonance between L and C_o , in addition to the parallel resonance between L and C , which is slightly changed because of C_o . The output impedance of the L-inverter is inductive for low frequencies up to the resonant frequency of the filter and capacitive for the frequencies above.

The optimisation of the voltage quality discussed in the previous subsection is achieved via tuning the series resonance between L and C_o . Since the load current i_o may include a large amount of harmonic components, especially when the load is nonlinear, the parallel resonance between L , C and C_o should be considered when designing the filter. According to (3.51), the parallel resonant frequency f_r can be obtained as

$$f_r = \frac{1}{2\pi} \sqrt{\frac{C+C_o}{LCC_o}} = \frac{1}{2\pi\sqrt{LC}} \sqrt{\frac{C}{C_o} + 1}. \quad (3.52)$$

With the same L and C , the resonance frequency f_r of C-inverters is higher than, but very

close to, that of the corresponding L-inverter or R-inverters, which is $\frac{1}{2\pi\sqrt{LC}}$, because C_o is often much larger than C . In order to avoid amplifying some harmonic current components, the resonance frequency f_r is recommended to be chosen between 10 times the line frequency ω^* and half of the switching frequency f_s (Wu et al., 2012). Hence, f_r is often far away from the harmonics to be eliminated by designing C_o . Indeed, if C_o is designed to eliminate the h -th harmonic, then according to (3.52), there is

$$f_r = \frac{1}{2\pi\sqrt{LC_o}} \sqrt{\frac{C_o}{C} + 1} = \frac{h\omega^*}{2\pi} \sqrt{\frac{C_o}{C} + 1}. \quad (3.53)$$

That is, the resonant frequency is $\sqrt{\frac{C_o}{C} + 1}$ times the harmonic frequency $h\omega^*$ under control. If $\sqrt{\frac{C_o}{C} + 1} > 3$, then $f_r > \frac{3h\omega^*}{2\pi}$ and it is over 9 times the system frequency ω^* even for $h = 3$. Hence, it is recommended to select f_r to satisfy

$$\frac{3h\omega^*}{2\pi} \leq f_r \leq \frac{1}{2}f_s \quad (3.54)$$

that is to select the parallel resonant frequency between three times of the harmonic frequency under control and half of the switching frequency. Accordingly, it is recommended to select the filter capacitor C to satisfy

$$\frac{3h\omega^*}{2\pi} \leq \frac{h\omega^*}{2\pi} \sqrt{\frac{C_o}{C} + 1} \leq \frac{1}{2}f_s$$

or, equivalently,

$$\frac{C_o}{\left(\frac{\pi f_s}{h\omega^*}\right)^2 - 1} \leq C \leq \frac{1}{8}C_o. \quad (3.55)$$

3.4 Simulation Results

Simulations were carried out with MATLAB 2013a, toolboxes such as Simulink and Simscape were extensively used. The solver used in the simulations was ode23 with a relative tolerance of 10^{-3} and the sampling time is $1\mu\text{F}$. More detailed information can be found in Appendix A. The single-phase inverter was powered by a 350 V dc voltage supply. The switching frequency is 10 kHz and the system frequency is 50 Hz. The rated load voltage is 230 V and the rated peak current is chosen as 40 A. Thus the rated apparent power of

the inverter is 6.5 kVA. The load is a full-bridge rectifier loaded with an LC filter (2.2 mH, 150 μ F) and a resistor $R_L = 30\Omega$, as shown in Figure A.2. An extra load consisting of a 200 Ω resistor and a 22 mH inductor in series was connected at $t = 2$ s, and disconnected at $t = 9$ s to test the transient response of C-inverters, R-inverters and L-inverters. The inverter reference voltage was generated by the robust droop controller proposed in (Zhong and Zeng, 2011), which is shown in Figure 4.3 and Figure A.4. The parameters of the robust droop controller were chosen as $n_i = 6.3 \times 10^{-4}$, $m_i = 3.4 \times 10^{-5}$ and $K_e = 10$.

According to (3.44), the filter inductor should be chosen between 0.55 mH and 1.46 mH. To make the load voltage THD small, the inductor is chosen as 0.55 mH. The virtual capacitor C_o is chosen to be 1400 μ F to reduce the 3rd and 5th harmonics. According to (3.55), the filter capacitor C should satisfy

$$1.84 \mu\text{F} \leq C \leq 174 \mu\text{F}, \quad (3.56)$$

from which the filter capacitor was selected as $C = 20 \mu\text{F}$.

Simulation results of the C-inverter with $C_o = 1400 \mu\text{F}$, together with a R-inverter with $Z_o = 4\Omega$ and an L-inverter designed according to the current feedback controller proposed in (Zhong, 2013b) with $K_i = 4$ and $K_i = 0$, respectively, are shown in Figure 3.5. When the extra load was connected/disconnected, all these inverters were able to respond fast and reach the steady state quickly and smoothly. It can be seen that the transient responses of the C-inverter and the L-inverter were better than the one of the R-inverter. For the C-inverter and the L-inverter, it takes approximately 0.02 s for the active power P to arrive at the steady state after the extra load is connected. While for the R-inverter, it takes approximately 0.2 s, which is approximately 9 times slower.

As shown in Table 3.1, the C-inverter achieved the lowest load voltage THD among the three types of inverters. When the extra load was disconnected, the voltage THD of the C-inverter was approximately 3.5%, while the ones of the R-inverter and the L-inverter were approximately 8.7% and approximately 4.5%, respectively. When the extra load was connected, the voltage THD of the C-inverter was decreased to be approximately 3%, while the ones of the R-inverter and the L-inverter were approximately 8.3% and approximately 4%, respectively.

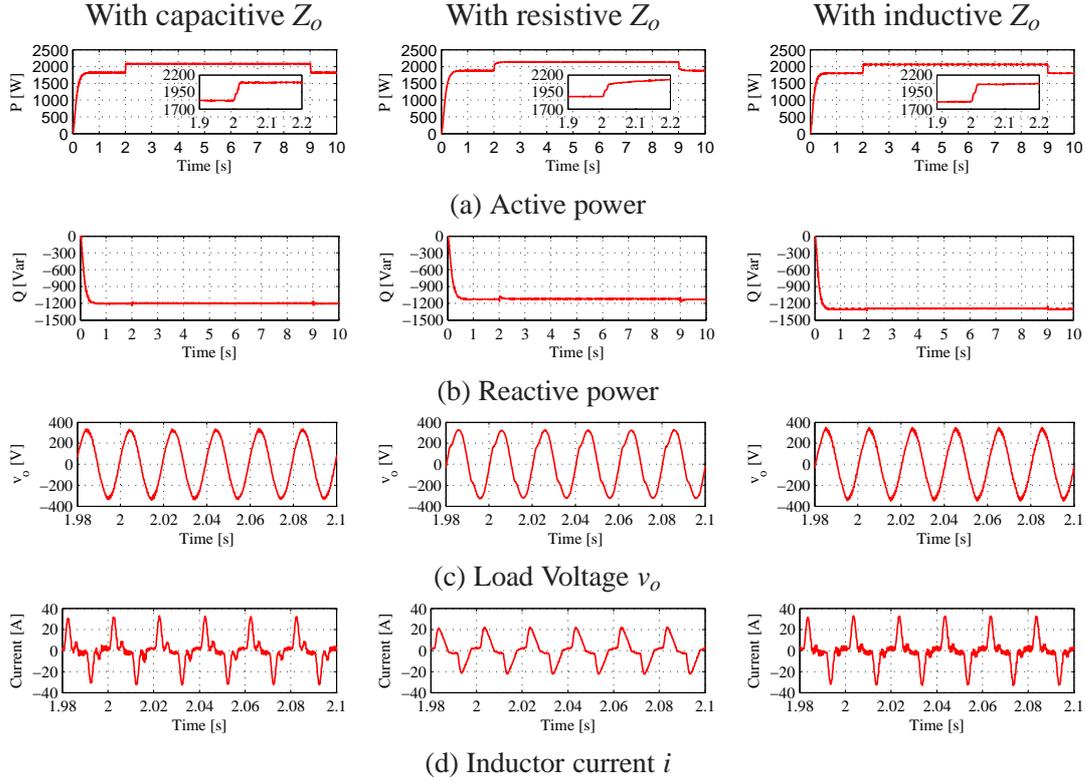


Figure 3.5: Simulation results with the extra load consisting of a 200Ω resistor and a 22 mH inductor in series connected at $t = 2\text{ s}$ and disconnected at $t = 9\text{ s}$: using the C-inverter with $C_o = 1400\mu\text{F}$ to reduce the 3rd and 5th harmonics (left column), using the R-inverter with $K_i = 4$ (middle column) and using the L-inverter (right column).

Table 3.1: THD of v_o of the C-inverter, the R-inverter and the L-inverter (%)

Type of inverter	C-	R-	L-
THD of v_o with extra load disconnected	3.5	8.7	4.5
THD of v_o with extra load connected	3	8.3	4

3.5 Experimental Results

To further validate the feasibility and performance of the proposed C-inverters, experiments were carried out on a test rig consisting of three single-phase inverters powered by three separate dc voltage supplies, as shown in Figure B.1(a). More detailed information can be found in Appendix B. The simulation and the experiment were of different voltage levels. While the simulation focused on the response of the inverter when a load change occurred, the experiment focused on the harmonic values and THD of v_o . In this chapter, only one of the three inverters of the experimental setup is used. This inverter is powered by a 180 V dc voltage supply, which is obtained from the non-regulated diode rectifier. The switching

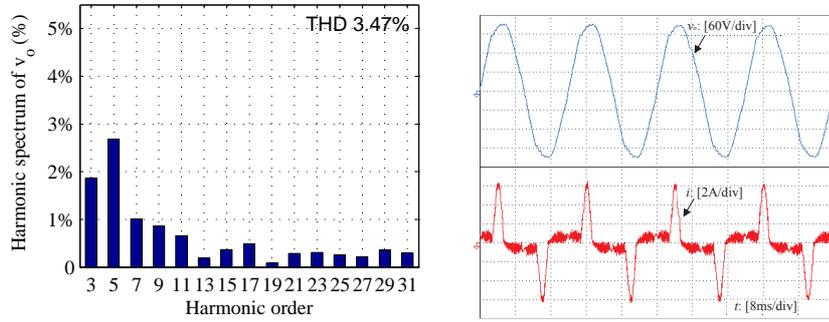
frequency is 10 kHz and the system frequency is 50 Hz. The rated load voltage is 110 V and the rated peak current is 8 A. The load is a full-bridge rectifier loaded with an LC filter (2.2 mH, 150 μ F) and a resistor $R_L = 200\Omega$.

According to (3.44), the filter inductor should be chosen between 1.41 mH and 3.75 mH. The on-board filter inductor 2.2 mH falls into this range. Three different cases with the virtual capacitor C_o chosen to reduce the 3rd harmonic, the 5th harmonic, and both the 3rd and 5th harmonics, respectively, were tested. The corresponding virtual capacitance C_o is 512 μ F, 184 μ F and 348 μ F, respectively. According to (3.55), the filter capacitor C should satisfy

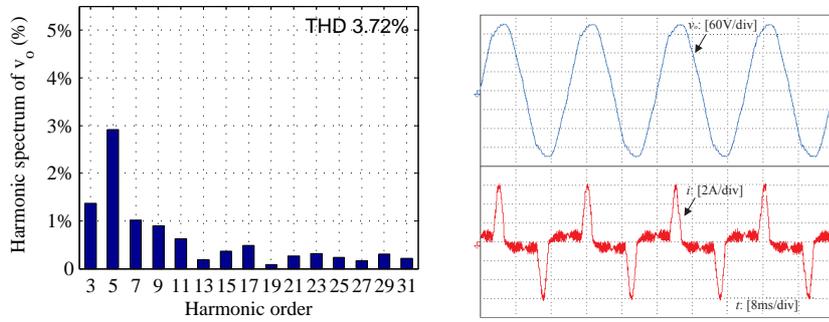
$$0.46\mu F \leq C \leq 23\mu F. \quad (3.57)$$

The on-board filter capacitor $C = 10\mu F$ falls into this range. The corresponding resonant frequency is 1131 Hz for the case with $h = 5$ and 1083 Hz for the case with $h = 3$, which leaves enough room for a normal switching frequency, e.g. 5kHz. The inverter reference voltage was also generated by the robust droop controller (Zhong and Zeng, 2011) shown in Figure 4.3, and the parameters of the robust droop controller were chosen as $n_i = 3.4 \times 10^{-3}$, $m_i = 3.9 \times 10^{-4}$ and $K_e = 10$.

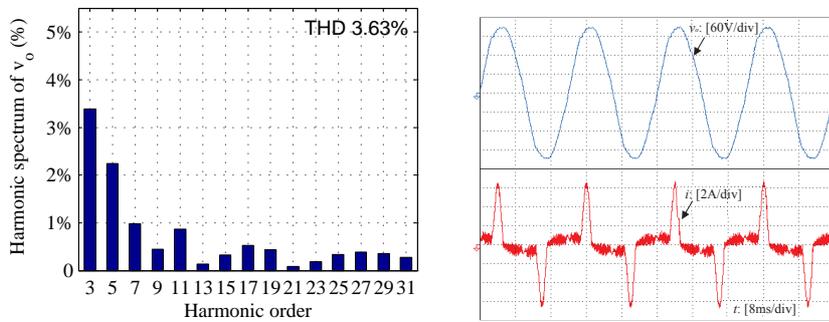
The experimental results are shown in Figure 3.6, together with those from an R-inverter with $Z_o = 4\Omega$ and an L-inverter designed according to the current feedback controller proposed in (Zhong, 2013b) with $K_i = 4$ and $K_i = 0$, respectively, for comparison. When the inverter was designed to have capacitive output impedance to reduce the effect of the 3rd and 5th harmonics, the 3rd harmonic was reduced by about 50% from the case of the L-inverter and by about 65% from the case of the R-inverter, and the 5th harmonic was reduced by about 30% and 18%, respectively. The THD was reduced by about 40% and 50%, respectively. When the inverter was designed to have capacitive output impedance to minimise the effect of the 3rd harmonic, the 3rd harmonic was reduced by 63% from the case of the L-inverter and by 74% from the case of the R-inverter, respectively. The THD was reduced by about 36% and by 47%, respectively. When the inverter was designed to have capacitive output impedance to minimise the effect of the 5th harmonic, the 5th harmonic was reduced by 41% from the case of the L-inverter and by 31% from the case of the R-inverter, respectively. The THD was reduced by about 37% and 48%, respectively. Apparently, C-inverters performed much better than the R- and L-inverters. Moreover, the



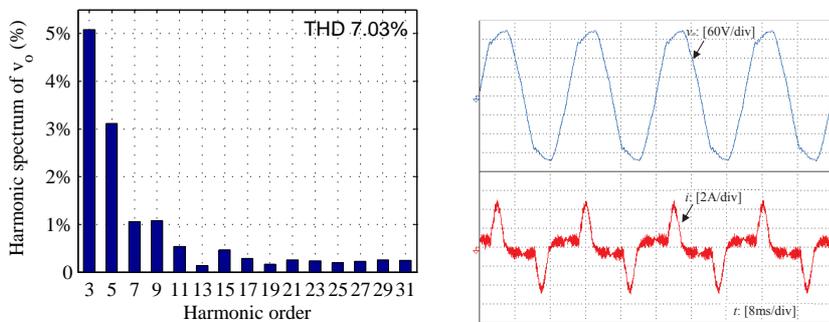
(a) C-inverter with $C_o = 348 \mu\text{F}$ to reduce the 3rd and 5th harmonics



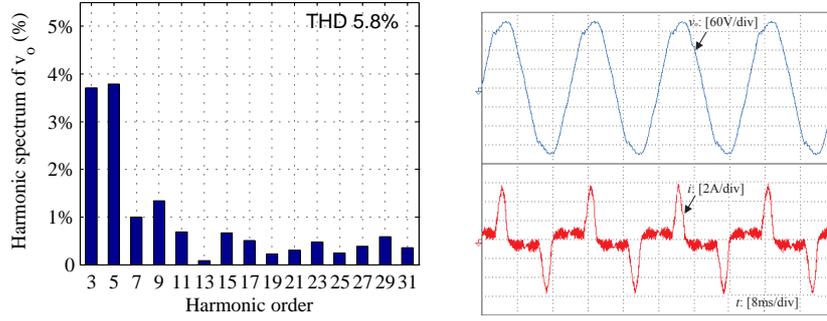
(b) C-inverter with $C_o = 512 \mu\text{F}$ to reduce the 3rd harmonic



(c) C-inverter with $C_o = 184 \mu\text{F}$ to reduce the 5th harmonic



(d) R-inverter with $K_i = 4$



(e) L-inverter

Figure 3.6: Experimental results: harmonic distribution of the load voltage (left column), load voltage and inductor current (right column).

THD is the lowest when C_o is designed to optimise the 3rd and 5th harmonics than to optimise these two separately. This is because the major harmonic components of the load voltage are the 3rd and 5th harmonics, as can be seen from Figure 3.6(e).

Table 3.2: Percentage harmonic values and THD of v_o (%)

Harmonic Order	3rd and 5th	3rd	5th	R-inverter	L-inverter
3	1.86	1.37	3.39	5.08	3.70
5	2.69	2.91	2.24	3.11	3.79
7	1.01	1.02	0.98	1.05	0.99
9	0.86	0.89	0.44	1.08	1.34
11	0.66	0.63	0.86	0.54	0.69
13	0.18	0.18	0.14	0.13	0.08
15	0.37	0.36	0.32	0.47	0.66
17	0.48	0.48	0.52	0.28	0.51
19	0.09	0.08	0.43	0.17	0.22
21	0.28	0.26	0.08	0.25	0.30
23	0.31	0.31	0.18	0.24	0.47
25	0.26	0.23	0.33	0.19	0.24
27	0.21	0.16	0.38	0.23	0.38
29	0.35	0.30	0.35	0.26	0.58
31	0.30	0.21	0.27	0.24	0.36
THD	3.47	3.72	3.63	7.03	5.8

The recorded average RMS values of the load voltage are 109.7V for the R-inverter, 110.2V for the L-inverter and 109.8V for C-inverters, which shows the excellent voltage regulation capability of the robust droop control strategy. This is true regardless of the virtual capacitance concept.

3.6 Summary

It has been shown that it is feasible to force the output impedance of an inverter to be capacitive over a wide range of both low and high frequencies although it normally has an inductor connected to the inverter bridge. Such inverters are called C-inverters. A simple but effective approach is to form an inductor current feedback through an integrator, of which the time constant is the desired output capacitance. This is a virtual capacitor so there is no limit on the current rating and can be applied to any power level. The capacitance can be selected to guarantee the stability of the current loop and an algorithm is proposed to optimise the value of the output capacitance so that the THD of the load voltage is minimised. Detailed guidelines have been provided to place the relevant frequencies properly so that the filter components can be determined. Extensive simulation and experimental results have shown that the voltage THD of an inverter can be reduced when it is designed to have capacitive output impedance, in comparison to an inverter having resistive or inductive output impedance. Moreover, no visible dc offsets are seen from the experimental results. One by-product of this study is that the filter inductor should be chosen small in order to reduce voltage harmonics and the criterion is reduced to meet the current ripples allowed on the inductor. A small inductor helps reduce the size, weight and volume of the passive components needed.

Chapter 4

Robust Droop Controller for C-inverters

In Chapter 3, the C-inverter has been proposed to achieve better voltage THD. In this chapter, the droop controller for parallel operation of C-inverters is studied. It aims to maintain the load voltage of parallel-connected C-inverters within a certain range, while sharing the loads proportionally according to their power ratings.

The droop control strategy is of different forms for inverters with different types of output impedance (Brabandere et al., 2007; Guerrero et al., 2008; 2005). The $Q \sim E$ and $P \sim \omega$ droops are used when the output impedance is inductive; the $Q \sim \omega$ and $P \sim E$ droops are used when the output impedance is resistive; for a complex impedance, a transformation involving the impedance phase angle needs to be introduced (Guerrero et al., 2006b; Yao et al., 2011). In this chapter, the droop for the C-inverter is studied, based on which a conventional droop controller for the C-inverter is proposed. However, inverters equipped with the conventional droop controller are required to have the same per-unit output resistance over a wide range of frequencies. To overcome this limitation, the structure of the robust droop controller (Zhong, 2013b) is adopted to achieve accurate sharing of the active power and the reactive power at the same time even when there are numerical errors, disturbances, component mismatches and parameter drifts.

The rest of the chapter is organised as follows. A conventional droop controller for the C-inverter is proposed in Section 4.1. Based on this, a robust droop controller for the C-inverter is developed in Section 4.2. Experimental results are presented in Section 4.4, followed by conclusions and discussions made in Section 4.5.

4.1 Conventional Droop Controller

An inverter can be modelled as a reference voltage source with an output impedance Z_o , as shown in Figure 2.5(b). According to (2.12) and (2.13), when the impedance is capacitive, then $\theta = -90^\circ$ and

$$P = -\frac{EV_o}{Z_o} \sin \delta \quad (4.1)$$

$$Q = -\frac{EV_o}{Z_o} \cos \delta + \frac{V_o^2}{Z_o}. \quad (4.2)$$

When δ is small,

$$P \approx -\frac{EV_o}{Z_o} \delta \quad (4.3)$$

$$Q \approx -\frac{E - V_o}{Z_o} V_o. \quad (4.4)$$

In this case, for a small δ , these are approximately

$$P \sim -\delta \quad (4.5)$$

$$Q \sim -E. \quad (4.6)$$

Hence, the conventional droop control strategy for inverters with capacitive output impedance should take the form

$$E = E^* + nQ \quad (4.7)$$

$$\omega = \omega^* + mP \quad (4.8)$$

which is sketched in Figure 4.1. Note that, in order to make sure that the $Q \sim -E$ loop and the $P \sim -\omega$ loop are of a negative feedback, respectively, so that the droop controller is able to regulate the frequency and the voltage, the signs before nQ and mP are all positive, which makes them boost terms.

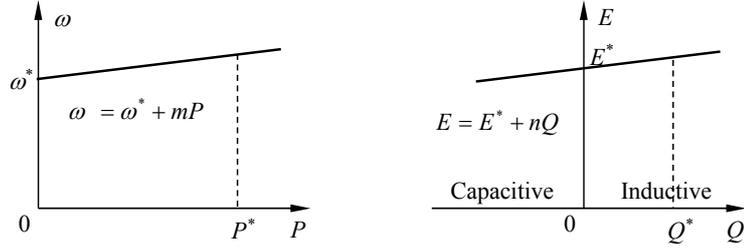


Figure 4.1: The droop controller for C-inverters.

The inverter voltage reference v_r is formed as a pure sinusoidal signal

$$v_r = \sqrt{2}E \sin(\omega t + \delta) \quad (4.9)$$

by taking E as the RMS voltage set-point and ω as its frequency. Figure 4.2 depicts the parallel operation of two inverters with capacitive output impedance. The power ratings of the inverters are $S_1^* = E^* I_1^*$ and $S_2^* = E^* I_2^*$ with the rated current I_1^* and I_2^* , respectively. They share the same load voltage v_o . Note that the load voltage drops when the load increases. This is called the load effect. In order for the inverters to share the load in proportion to their power ratings, the droop coefficients of the inverters should be in inverse proportion to their power ratings (Tuladhar et al., 1997; Guerrero et al., 2008), i.e., n and m should be chosen to satisfy

$$n_1 S_1^* = n_2 S_2^* \quad (4.10)$$

$$m_1 S_1^* = m_2 S_2^*. \quad (4.11)$$

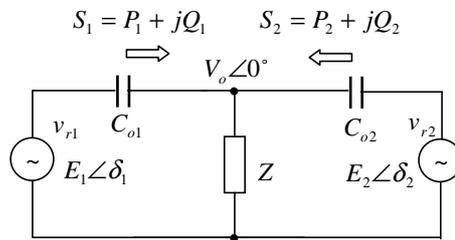


Figure 4.2: Two C-inverters operated in parallel.

4.2 Robust Droop Controller

As reported in (Zhong, 2013b), the conventional droop control strategy is not able to accurately share both real power and reactive power at the same time because there is no mechanism to make sure that the voltage set-points are the same when numerical errors, noises and disturbances exist. Also it is impossible to make sure that the per-unit output impedance are the same because of component mismatches and parameter shifts. Hence, the voltage regulator added to the conventional droop controllers for inverters with resistive (or inductive) impedance proposed in (Zhong, 2013b) should also be added to the droop controller for inverters with capacitive output impedance. This results in the robust droop controller, shown in Figure 4.3, and described with:

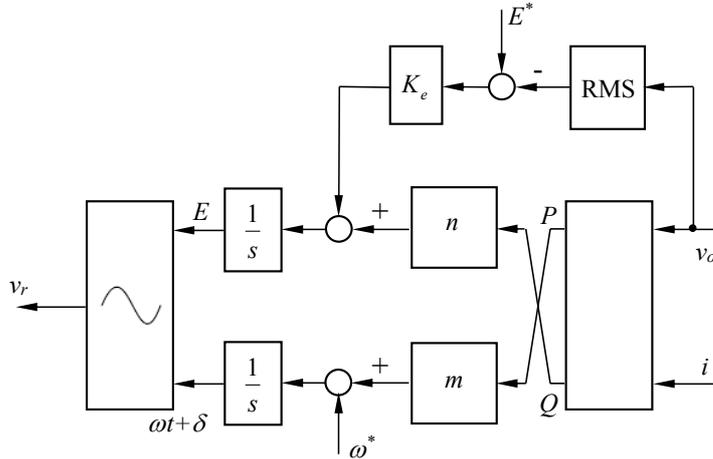


Figure 4.3: The robust droop controller for C-inverters (Zhong and Zeng, 2011).

$$\dot{E} = K_e(E^* - V_o) + nQ \quad (4.12)$$

$$\omega = \omega^* + mP. \quad (4.13)$$

It is able to share both real power and reactive power accurately even if the per-unit output impedance are not the same and/or there are numerical errors, disturbances and noises because, in a steady state, one has

$$nQ + K_e(E^* - V_o) = 0. \quad (4.14)$$

This means

$$nQ = \text{constant} \quad (4.15)$$

as long as K_e is the same for all inverters. This guarantees the accurate sharing of reactive power in proportion to their ratings. As long as the system is stable, which leads to the same frequency, the real power can be guaranteed as well (Zhong, 2013b).

According to (4.14), the load voltage is

$$V_o = E^* + \frac{n}{K_e}Q = E^* + \frac{nQ}{K_e E^*}E^* \quad (4.16)$$

which can be maintained within the desired range via choosing a big K_e . Hence, the control strategy has very good capability of voltage regulation as well, in addition to the accurate power sharing. This is the same as the inverters with resistive (and inductive) output impedance reported in (Zhong, 2013b). The droop coefficients n and m can be determined as usual by the desired voltage drop/boost ratio R_v and the frequency drop/boost ratio R_f , respectively, at the rated real power P^* and reactive power Q^* :

$$n = \frac{R_v K_e E^*}{Q^*} \quad (4.17)$$

$$m = \frac{R_f \omega^*}{P^*}. \quad (4.18)$$

4.3 Small-signal Stability

It is a great challenge to analyze the stability of inverters in parallel operation. Here, the small-signal stability of a C-inverter equipped with the robust droop controller (4.12-4.13) is analyzed. Consider small disturbances around the stable equilibrium operation point (δ_e, V_{oe}, E_e) , where E_e and V_{oe} are the magnitudes of the source voltage and the load voltage, respectively. δ_e is the phase angle difference between the source voltage and the load voltage. Linearising (2.12) and (2.13)

$$\Delta P(s) = \frac{V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)}{Z_o} \Delta E(s) + \frac{E_e V_{oe}(-\sin \delta_e \cos \theta + \cos \delta_e \sin \theta)}{Z_o} \Delta \delta(s) \quad (4.19)$$

$$\Delta Q(s) = \frac{V_{oe}(\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)}{Z_o} \Delta E(s) - \frac{E_e V_{oe}(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o} \Delta \delta(s). \quad (4.20)$$

The robust droop controller for C-inverter (4.12-4.13) can be linearized around the equilibrium as

$$s\Delta E(s) = n\Delta Q(s) \quad (4.21)$$

$$\Delta \omega(s) = m\Delta P(s). \quad (4.22)$$

Additionally, there is

$$\Delta \omega(s) = s\Delta \delta(s). \quad (4.23)$$

Note that the real power and the reactive power are normally measured using a low pass filter $\frac{\omega_f}{s+\omega_f}$. Combining (4.19-4.23), the small-signal model of the closed-loop system is

$$s\Delta E(s) = n \cdot \frac{\omega_f}{s+\omega_f} \cdot \left[\frac{V_{oe}(\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)}{Z_o} \Delta E(s) - \frac{E_e V_{oe}(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o} \Delta \delta(s) \right] \quad (4.24)$$

$$s\Delta \delta(s) = m \cdot \frac{\omega_f}{s+\omega_f} \cdot \left[\frac{V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)}{Z_o} \Delta E(s) + \frac{E_e V_{oe}(-\sin \delta_e \cos \theta + \cos \delta_e \sin \theta)}{Z_o} \Delta \delta(s) \right]. \quad (4.25)$$

From (4.24) and (4.25), there is

$$\Delta E(s) = \frac{-n\omega_f E_e V_{oe}(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o s^2 + Z_o \omega_f s - n\omega_f V_{oe}(\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)} \Delta \delta(s). \quad (4.26)$$

which leads to the following homogeneous equation

$$as^4 \Delta \delta(s) + bs^3 \Delta \delta(s) + cs^2 \Delta \delta(s) + ds \Delta \delta(s) + e \Delta \delta(s) = 0 \quad (4.27)$$

with

$$a = Z_o^2 \quad (4.28)$$

$$b = 2Z_o^2 \omega_f \quad (4.29)$$

$$c = Z_o \omega_f (-V_{oe}(\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)(n + mE_e) + Z_o \omega_f) \quad (4.30)$$

$$d = -Z_o \omega_f^2 V_{oe}((\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)(n + mE_e)) \quad (4.31)$$

$$e = mnE_e \omega_f^2 V_{oe}^2. \quad (4.32)$$

The system stability can be analyzed by investigating the characteristic equation

$$as^4 + bs^3 + cs^2 + ds + e = 0. \quad (4.33)$$

The rated system frequency is 50 Hz and the rated load voltage is 12 V. According to (4.16), V_{oe} remains as a constant at the equilibrium as long as the load is unchanged and n , K_e , E^* are fixed. Taking inverter 1 for example, according to the parameters in the experiment, and considering the nonlinear load case, there are

$$V_{oe} = 11.62V \quad (4.34)$$

$$E_e = 14.24V \quad (4.35)$$

$$\delta_e = -17.2^\circ \quad (4.36)$$

which result in

$$\lambda_1 = -6.5227 + 3.5092i \quad (4.37)$$

$$\lambda_2 = -6.5227 - 3.5092i \quad (4.38)$$

$$\lambda_3 = -3.4773 + 3.5092i \quad (4.39)$$

$$\lambda_4 = -3.4773 - 3.5092i. \quad (4.40)$$

As the real parts of the characteristic roots are all negative, the small signal stability around the equilibrium has been guaranteed.

4.4 Experimental Results

Experiments were carried out on the test rig consisting of three single-phase inverters, as shown in Figure B.1(a). More detailed information can be found in Appendix B. In this chapter, only two of the three inverters of the experimental setup are used. The capacity of Inverter 1 is 25 VA and the capacity of Inverter 2 is 50 VA, with the rated power factor of 0.9. It is expected that $P_2 = 2P_1$ and $Q_2 = 2Q_1$. The switching frequency is 7.5 kHz and the frequency of the system is 50 Hz. The dc voltage supply is 42 V, the rated voltage is 12 V and $K_e = 20$. The filter inductor is $L = 2.35$ mH with a parasitic resistance of 0.1Ω

and the filter capacitance C is $22\ \mu\text{F}$. The cut-off frequency of the power low pass filter is $10\ \text{rad/s}$.

The desired voltage drop ratio $\frac{n_i Q_i^*}{K_e E^*}$ is chosen to be 10% at the rated reactive power $Q_i^* = 0.436 S_i^*$, and the desired frequency boost ratio $\frac{m_i P_i^*}{\omega^*}$ is chosen to be 1% at the rated real power $P_i^* = 0.9 S_i^*$. As a result, $n_1 = 2.2$ and $n_2 = 1.1$; $m_1 = 0.14$ and $m_2 = 0.07$. The capacitor is chosen as $C_o = 479\ \mu\text{F}$ and the corresponding impedance at the fundamental frequency is $Z_o(j\omega^*) = -j6.65\ \Omega$, which is capacitive and is able to dominate the impedance between the voltage reference and the terminal. The performance of the parallel operation of C-inverters is compared with the performance of R-inverters with $Z_o = 4\ \Omega$, which are designed according to the current feedback controller proposed in (Zhong, 2013b). At $t = 0\ \text{s}$, Inverter 1 was started to feed the load. Then, at about $t = 3\ \text{s}$, Inverter 2 was connected in parallel with Inverter 1. After that, at about $t = 9\ \text{s}$, Inverter 2 was disconnected.

4.4.1 With a Linear Load

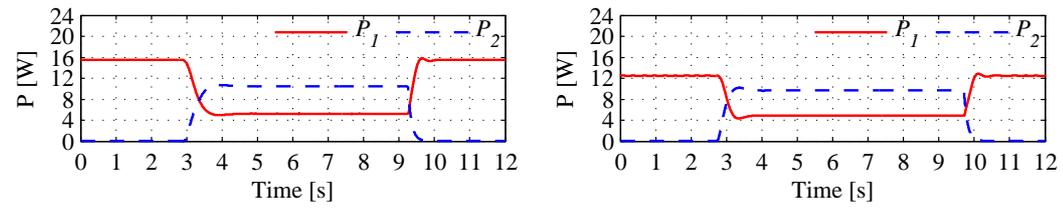
Experiments were carried out with a linear load $R_L = 9\ \Omega$. The results for the C-inverter and the R-inverter are shown in the left and right columns of Figure 4.4, respectively. The steady-state performance is shown in and Table 4.1. As can be seen, for both these two types of inverters, the power sharing was accurate, and the voltage magnitude and frequency were regulated very well:

- 1) the real power and the reactive power were well shared in the ratio 1:2;
- 2) the load voltage magnitude was close to $12\ \text{V}$;
- 3) the load voltage frequency deviation was maintained to be smaller than $0.5\ \text{Hz}$.

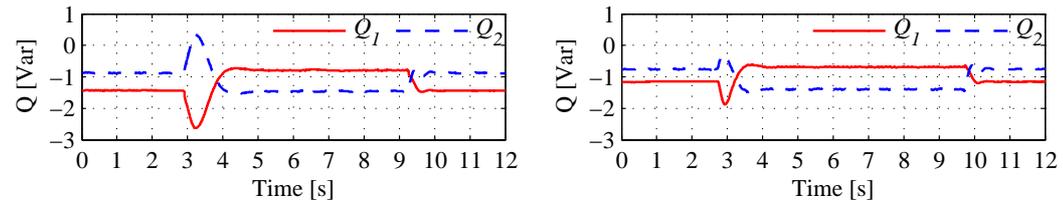
Note that for the C-inverter, the voltage magnitude dropped from its nominal value, while the frequency was boosted. For the R-inverter, both the voltage magnitude and the frequency dropped from their nominal values.

Table 4.1: Steady-state performance of two parallel operated inverters with a linear load

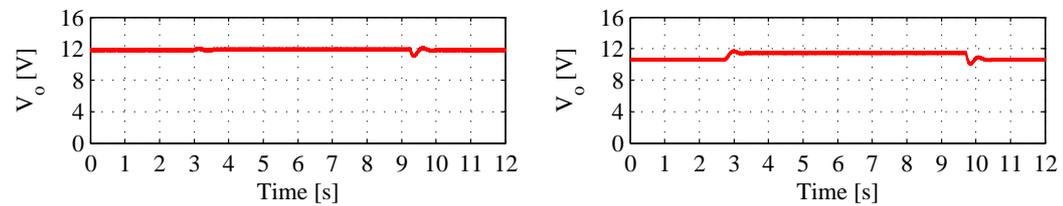
Variable	C-inverters	R-inverters
Apparent power 1 (VA)	5.3-0.75j	4.8-0.65j
Apparent power 2 (VA)	10.6-1.5j	9.6-1.3j
RMS load voltage (V)	11.9	11.5
Frequency f (Hz)	50.12	49.98



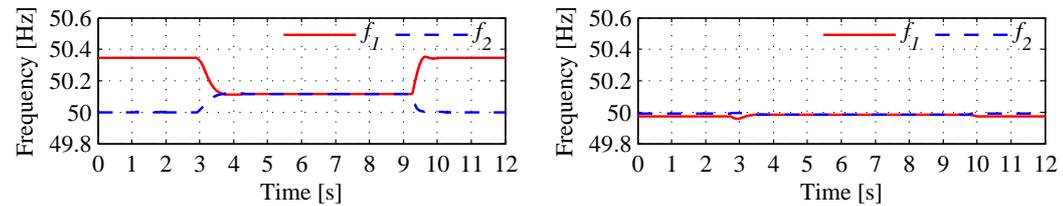
(a) Real power



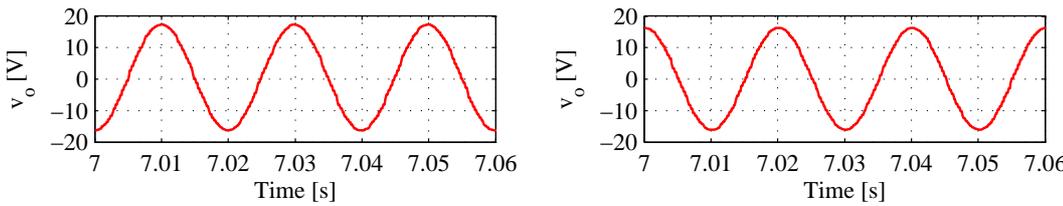
(b) Reactive power



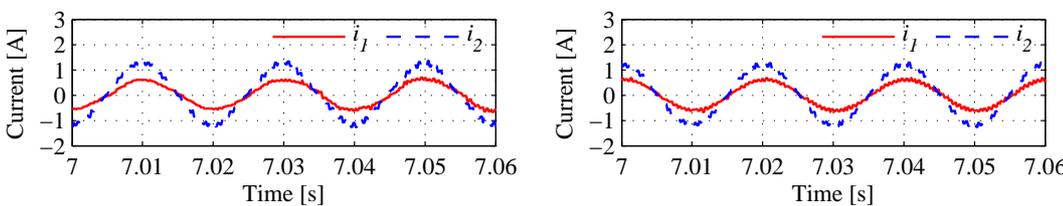
(c) RMS load voltage



(d) Frequency



(e) Load voltage at the steady state



(f) Current at the steady state

Figure 4.4: Experimental results of two parallel operated inverters with the linear load: using C-inverters (left column) and using R-inverters (right column).

In comparison to the R-inverter, the voltage regulation of the C-inverter was slightly better because the voltage magnitude was related to the reactive power, which was smaller than the real power, and the frequency variation of the C-inverter was slightly higher because the voltage magnitude was related to the real power. The load voltage THD for both these two types of inverters was kept to be approximately 2.2%, which is lower than 5%.

4.4.2 With a Nonlinear Load

Experiments were carried out for a full-bridge rectifier load with an LC filter $L = 2.2\text{mH}$, $C = 1000\mu\text{F}$ and $R_L = 9\Omega$, as shown in Figure A.2. The results are shown in Figure 4.5 and Table 4.2. Again, for both these two types of inverters, the power sharing was accurate, and the voltage magnitude and frequency were regulated very well. Compared with the cases with the linear load, the active power increased and the reactive power decreased, thus the voltage magnitude and frequency deviated further from the nominal values.

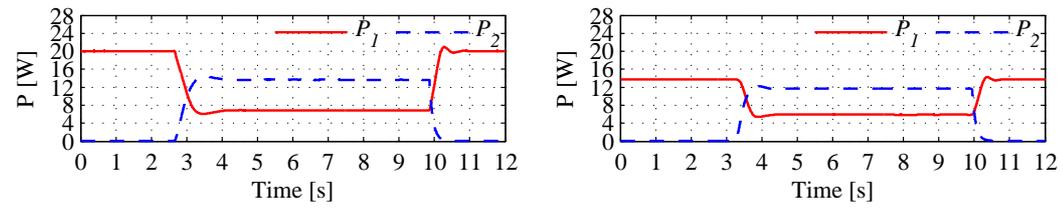
Table 4.2: Steady-state performance of two parallel operated inverters with a nonlinear load

Variable	C-inverters	R-inverters
Apparent power 1 (VA)	7-2.6j	12-1.8j
Apparent power 2 (VA)	14-5.2j	6-3.6j
RMS load voltage (V)	11.9	11.2
Frequency f (Hz)	50.16	49.96

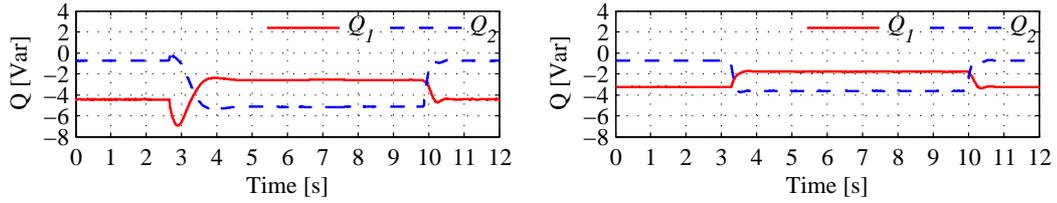
Besides, harmonic components exist in both the load voltage and the inductor current because of the nonlinear load. As shown in Table 4.3, the C-inverter achieved lower load voltage THD than the R-inverter. When Inverter 2 was disconnected with Inverter 1, the voltage THD of the C-inverter was approximately 18.3%, while the one of the R-inverter was approximately 20.8%. When Inverter 2 was connected in parallel with Inverter 1, the voltage THD of the C-inverter was approximately 10.2%, while the one of the R-inverter was approximately 14.3%. Obviously, compared with the case when these two inverters were disconnected, the THD of the load voltage dropped when these two inverters were operated in parallel, and it dropped more when with C-inverters than when with R-inverters.

Table 4.3: THD of v_o of parallel operated C-inverters or R-inverters (%)

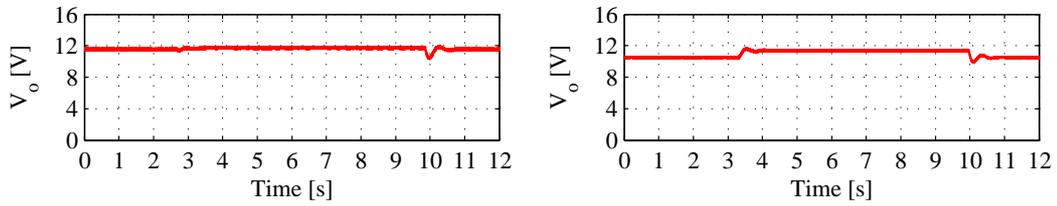
Type of inverter	C-	R-
THD of v_o when Inverter 2 was disconnected	18.3	20.8
THD of v_o when Inverter 2 was connected in parallel	10.2	14.3



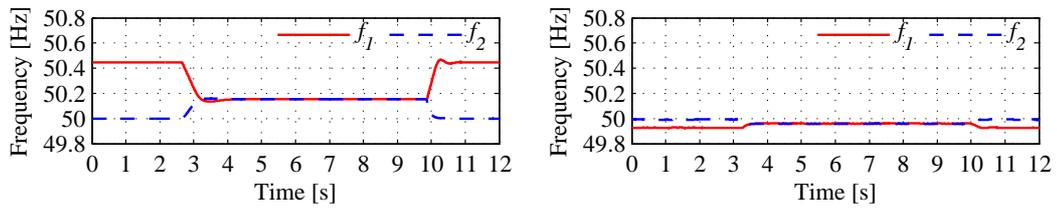
(a) Real power



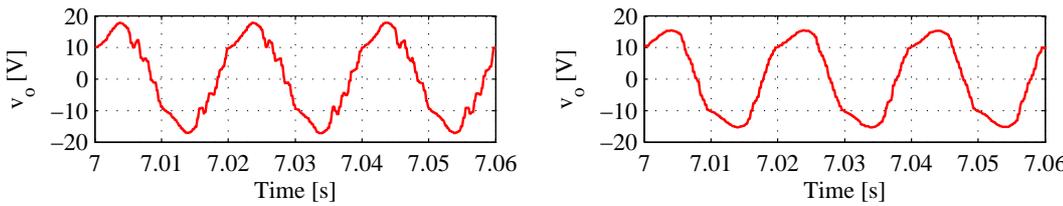
(b) Reactive power



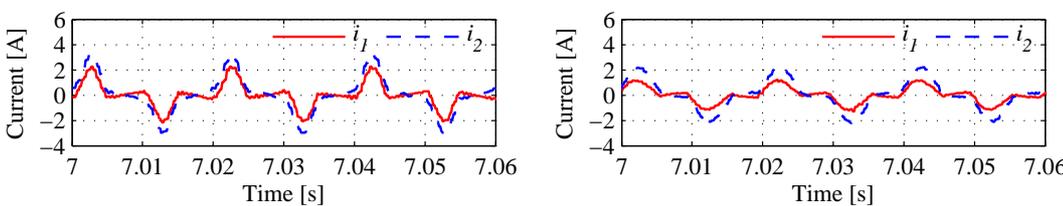
(c) RMS load voltage



(d) Frequency



(e) Load voltage at the steady state



(f) Current at the steady state

Figure 4.5: Experimental results of two parallel operated inverters with the nonlinear load: using C-inverters (left column) and using R-inverters (right column).

4.5 Summary

In order to enable parallel operation of C-inverters, the robust droop controller proposed in (Zhong, 2013b) is further developed and applied for accurate load sharing, as well as good voltage and frequency regulation. Experimental results have shown that C-inverters can be operated in parallel without any problem. Besides, with the developed robust droop controller, the parallel-connected C-inverter systems can achieve better power quality than parallel-connected R- inverter systems, while maintaining good voltage regulation and accurate load sharing.

Chapter 5

Improved C-inverters with Virtual Capacitive Resonant Impedance

In Chapter 3, it has been shown that the THD of an load voltage can be reduced when it is designed to have capacitive output impedance (Zhong and Hornik, 2013; Zhong and Zeng, 2011), in comparison to an inverter having resistive or inductive output impedance. In this chapter, the C-inverter is further developed. A control strategy is proposed to achieve the virtual resonant impedance to improve the quality of the load voltage. It is based on a resonant impedance topology consisting of inductors and capacitors, of which the magnitude approaches 0 at different frequencies. The proposed control strategy involves the feedback of the inductor current through a transfer function, which is actually the expression of the virtual resonant impedance. The coefficients of the transfer function or the virtual resonant impedance are selected and optimised to reduce load voltage harmonics of different orders at the same time, and thus the corresponding total harmonic distortion (THD) of the load voltage could be reduced.

The rest of the chapter is organised as follows. A controller is proposed in Section 5.1 to add the virtual resonant impedance. Control parameters is designed and optimised to reduce the voltage THD in Section 5.2. Three special cases are studied in Section 5.3. Experimental results are presented in Section 5.4, followed by conclusions and discussions made in Section 5.5.

5.1 Implementation of Virtual Resonant Impedance

The inverter can be modelled as shown in Figure 2.5(b) as the series connection of a voltage reference v_r and the output impedance Z_o . The following two equations hold for the closed-loop system consisting of Figure 2.5(b) and Figure 5.1 (a):

$$u = v_r - Z_v i, \quad \text{and} \quad u_f = (R + sL)i + v_o \quad (5.1)$$

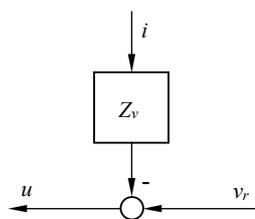
where R is the ESR of the inductor. It is normally small but not exactly 0. Since the average of u_f over a switching period is the same as u , there is (approximately)

$$v_o = v_r - Z_o(s) \cdot i \quad (5.2)$$

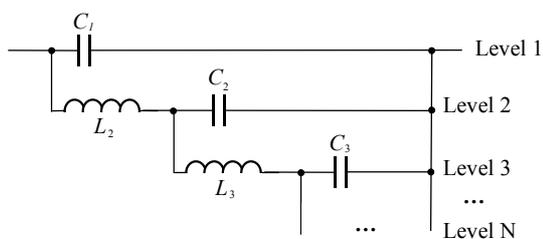
with the output impedance $Z_o(s)$ given by

$$Z_o(s) = R + sL + Z_v. \quad (5.3)$$

As a result, the integrator block Z_v is added virtually to the original output impedance of the inverter. This is equivalent to connecting the virtual resonant impedance shown in Figure 5.1(b) (inside the inverter) in series with the filter inductor L .



(a) The controller design



(b) The corresponding topology

Figure 5.1: The virtual resonant impedance.

When the virtual resonant impedance is not added, which means $Z_v = 0$, there is

$$Z_o(s) = R + sL. \quad (5.4)$$

When the level 1 of the virtual resonant impedance is added, the inverter is in fact a traditional C-inverter (Zhong and Zeng, 2011; 2014) with

$$Z_v = \frac{1}{sC_1} \quad (5.5)$$

where C_1 can be designed to reduce the voltage harmonic component at a certain order.

When the levels 1 and 2 of the virtual resonant impedance are added, the virtual impedance can be described by

$$Z_v = \frac{C_2L_2s^2 + 1}{s(C_1 + C_2 + C_1C_2L_2s^2)} \quad (5.6)$$

where C_1 , C_2 and L_2 can be designed to simultaneously reduce the voltage harmonic components at two different orders.

When the levels 1, 2 and 3 of the virtual resonant impedance are added, this means

$$Z_v = \frac{C_2L_2s^2 + C_3L_2s^2 + C_3L_3s^2 + C_2C_3L_2L_3s^4 + 1}{s(C_1 + C_2 + C_3 + C_1C_2L_2s^2 + C_1C_3L_2s^2 + C_1C_3L_3s^2 + C_2C_3L_3s^2 + C_1C_2C_3L_2L_3s^4)} \quad (5.7)$$

Here, C_1 , C_2 , C_3 , L_2 and L_3 can be designed to simultaneously reduce the voltage harmonic components at three different orders. Similarly, when level 1 to N of the virtual resonant impedance are added, parameters can be designed to simultaneously reduce the voltage harmonic components at N different orders.

5.2 Optimisation of Virtual Resonant Impedance

5.2.1 For 1 Level of Virtual Resonant Impedance

When the level 1 of the virtual resonant impedance is added, one specified order harmonic could be addressed. This is the same as C-inverter. If a single h_1 -th harmonic component

is concerned, according to (5.3) and (5.5), the optimal C_1 is

$$C_1 = \frac{1}{(h_1 \omega^*)^2 L}. \quad (5.8)$$

This forces the impedance at the h_1 -th harmonic frequency close to 0, hence no voltage at this frequency is caused, assuming $R = 0$.

5.2.2 For 2 Levels of Virtual Resonant Impedance

When the first two levels are added, two specified order harmonics could be addressed. If h_1 -th and h_2 -th harmonic components are concerned, according to (5.3) and (5.6), the nominator of the inverter output impedance should be 0:

$$C_1 C_2 L L_2 s^4 + C_1 L s^2 + C_2 L s^2 + C_2 L_2 s^2 + 1 = 0 \quad (5.9)$$

which forces the impedance at the h_1 -th and h_2 -th harmonic frequency close to 0, hence no voltage at these frequencies is caused, assuming $R = 0$. (5.9) should be equivalent to

$$(s^2 + h_1^2 \omega^{*2})(s^2 + h_2^2 \omega^{*2}) = 0. \quad (5.10)$$

Thus, there are

$$\begin{cases} C_1 C_2 L L_2 = \frac{1}{h_1^2 h_2^2 \omega^{*4}} \\ C_1 L + C_2 L + C_2 L_2 = \frac{h_1^2 + h_2^2}{h_1^2 h_2^2 \omega^{*2}} \end{cases} \quad (5.11)$$

and

$$\begin{cases} C_1 = \frac{h_1^2 + h_2^2 \pm \sqrt{\frac{L_2(h_1^4 + h_2^4) - 4Lh_1^2 h_2^2 - 2L_2 h_1^2 h_2^2}{L_2}}}{2L\omega^{*2} h_1^2 h_2^2} \\ C_2 = \frac{h_1^2 + h_2^2 \pm \sqrt{\frac{L_2(h_1^4 + h_2^4) - 4Lh_1^2 h_2^2 - 2L_2 h_1^2 h_2^2}{L_2}}}{2(L+L_2)\omega^{*2} h_1^2 h_2^2}. \end{cases} \quad (5.12)$$

As C_1 and C_2 have to be real values, there should be

$$L_2 \geq \frac{4h_1^2 h_2^2}{h_1^4 - 2h_1^2 h_2^2 + h_2^4} L. \quad (5.13)$$

In order to make the calculation simple, L_2 is chosen as

$$L_2 = \frac{4h_1^2 h_2^2}{h_1^4 + h_2^4 - 2h_1^2 h_2^2} L. \quad (5.14)$$

Then, there will be

$$\begin{cases} C_1 = \frac{h_1^2 + h_2^2}{2L\omega^{*2}h_1^2h_2^2} \\ C_2 = \frac{(\omega^{*2}h_1^2 + \omega^{*2}h_2^2)(h_1^4 + h_2^4 - 2h_1^2h_2^2)}{2L\omega^{*4}h_1^2h_2^2(h_1^4 + h_2^4 + 2h_1^2h_2^2)}. \end{cases} \quad (5.15)$$

Note that the following holds true:

$$C_1L = C_2(L + L_2) = \frac{h_1^2 + h_2^2}{2h_1^2h_2^2\omega^{*2}}. \quad (5.16)$$

5.2.3 For 3 Levels of Virtual Resonant Impedance

When the level 1, 2 and 3 of the virtual resonant impedance are added, three specified order harmonics could be addressed. If h_1 -th, h_2 -th and h_3 -th harmonic components are concerned, according to (5.3) and (5.7), the nominator of the inverter output impedance should be 0 assuming $R = 0$. It is equivalent to

$$(s^2 + h_1^2\omega^{*2})(s^2 + h_2^2\omega^{*2})(s^2 + h_3^2\omega^{*2}) = 0. \quad (5.17)$$

Thus, there are

$$\begin{cases} C_1C_2C_3LL_2L_3 = \frac{1}{\omega^{*6}h_1^2h_2^2h_3^2} \\ C_1C_2LL_2 + C_1C_3LL_2 + C_1C_3LL_3 + C_2C_3LL_3 + C_2C_3L_2L_3 = \frac{h_1^2 + h_2^2 + h_3^2}{\omega^{*4}h_1^2h_2^2h_3^2} \\ C_1L + C_2(L + L_2) + C_3(L + L_2 + L_3) = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{\omega^{*2}h_1^2h_2^2h_3^2}. \end{cases} \quad (5.18)$$

Similar to the case of level 2, set

$$C_1L = C_2(L + L_2) = C_3(L + L_2 + L_3) = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3\omega^{*2}h_1^2h_2^2h_3^2}. \quad (5.19)$$

It means that

$$\begin{cases} C_1 = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3L\omega^{*2}h_1^2h_2^2h_3^2} \\ C_2 = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3(L + L_2)\omega^{*2}h_1^2h_2^2h_3^2} \\ C_3 = \frac{h_1^2h_2^2 + h_1^2h_3^2 + h_2^2h_3^2}{3(L + L_2 + L_3)\omega^{*2}h_1^2h_2^2h_3^2}. \end{cases} \quad (5.20)$$

Then, there will be

$$\begin{cases} \frac{L_2 L_3}{(L+L_2)(L+L_2+L_3)} = \frac{27h_1^4 h_2^4 h_3^4}{(h_1^2 h_2^2 + h_1^2 h_3^2 + h_2^2 h_3^2)^3} \\ \frac{L_2}{L+L_2} + \frac{L_2+2L_3}{L+L_2+L_3} = \frac{9h_1^2 h_2^2 h_3^2 (h_1^2 + h_2^2 + h_3^2)}{(h_1^2 h_2^2 + h_1^2 h_3^2 + h_2^2 h_3^2)^2}. \end{cases} \quad (5.21)$$

Here, set

$$\begin{cases} K_1 = \frac{27h_1^4 h_2^4 h_3^4}{(h_1^2 h_2^2 + h_1^2 h_3^2 + h_2^2 h_3^2)^3} \\ K_2 = \frac{9h_1^2 h_2^2 h_3^2 (h_1^2 + h_2^2 + h_3^2)}{(h_1^2 h_2^2 + h_1^2 h_3^2 + h_2^2 h_3^2)^2}. \end{cases} \quad (5.22)$$

Then, there are

$$\begin{cases} L_2 = \frac{K_2 - 3K_1 \mp \sqrt{K_1^2 + K_2^2 + 2K_1 K_2 - 16K_1}}{2(K_1 - K_2 + 2)} L \\ L_3 = \frac{K_1 + K_2 \pm \sqrt{K_1^2 + K_2^2 + 2K_1 K_2 - 16K_1}}{2(K_1 - K_2 + 2)} L. \end{cases} \quad (5.23)$$

As L_2 and L_3 have to be real values, there should be

$$K_1^2 + K_2^2 + 2K_1 K_2 - 16K_1 \geq 0. \quad (5.24)$$

Similar to (5.16) and (5.19), this method could be extended to the case with N levels:

$$C_1 L = C_2 (L + L_2) = \cdots = C_N (L + \sum_{i=2}^N L_i). \quad (5.25)$$

According to (5.3), (5.6) and (5.7), it is obvious that the virtual resonant impedance has some magnitude peaks. In order to dampen these peaks, for N -level virtual resonant output impedance, a virtual R_c can be added in parallel with C_N . Besides, the overall output impedance $Z(s)$ after taking into account the filter capacitor C is

$$Z(s) = \frac{Z_o(s)}{sCZ_o(s) + 1} \quad (5.26)$$

of which the a typical Bode diagram is shown in Figure 5.2.

This figure is obtained with the parameters of the experiment given in Section 5.4. The dotted line is obtained with no virtual output impedance adopted (0 level), where the inverter is an L-inverter. The dash-dot line is for the case of the C-inverter, where 1 level of the VRI is adopted to reduce the 3rd order voltage harmonics. The dashed line is depicted with 2 levels of the VRI adopted, where both 3rd order and 5th order voltage harmonics are mitigated. The solid line is obtained when 3 levels of the VRI is adopted to handle the 3rd order, the 5th order, and the 7th order voltage harmonics simultaneously.

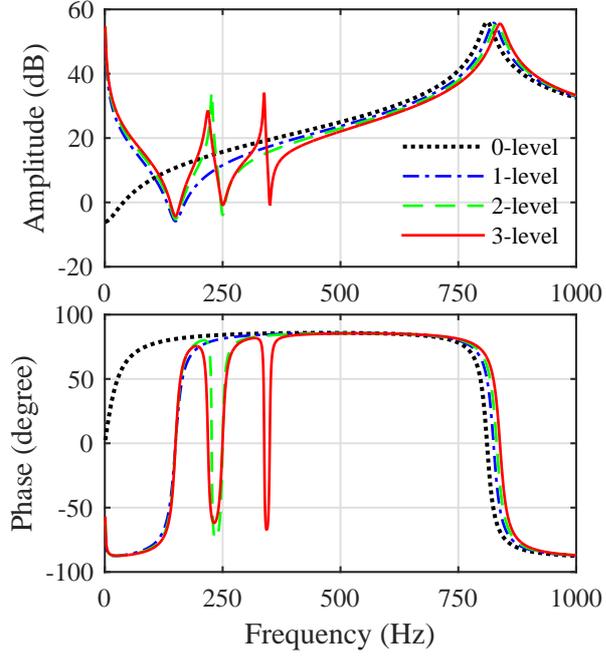


Figure 5.2: A typical Bode diagram for the overall inverter output impedance.

5.3 Special Cases Studied

5.3.1 Case I: To Minimise the 3rd Harmonic Component

This case is in fact the same as the Special Case II in Chapter 3, with C_1 :

$$C_1 = \frac{1}{(3\omega^*)^2 L} \quad (5.27)$$

and the corresponding impedance is

$$Z_o(j\omega) = R + j\omega^* L \left(\frac{\omega}{\omega^*} - \frac{9\omega^*}{\omega} \right). \quad (5.28)$$

At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j8\omega^* L \approx -j8\omega^* L. \quad (5.29)$$

It is nearly purely capacitive as expected because R is normally smaller than $8\omega^* L$.

5.3.2 Case II: To Minimise the 3rd and 5th Harmonic Components

In most cases, it is enough to consider the 3rd and 5th harmonics only. This gives the optimal capacitances

$$\begin{cases} C_1 = \frac{17}{225(\omega^*)^2 L} \\ C_2 = \frac{64}{3825(\omega^*)^2 L} \end{cases} \quad (5.30)$$

and

$$L_2 = \frac{225}{64} L. \quad (5.31)$$

As a result, the virtual impedance is

$$Z_v(j\omega) = (L_1 \omega^{*2} (\omega^2 - 17\omega^{*2}) (-225j)) / (\omega (17\omega^2 - 353\omega^{*2})). \quad (5.32)$$

The output impedance is

$$Z_o(j\omega) = R + j\omega 17L \frac{(\omega^4 + 225\omega^{*4} - 34\omega^2 \omega^{*2})}{\omega^2 (17\omega^2 - 353\omega^{*2})}. \quad (5.33)$$

At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j\frac{68}{7} \omega^* L \approx -j\frac{68}{7} \omega^* L \quad (5.34)$$

which is nearly purely capacitive.

5.3.3 Case III: To Minimise the 3rd, 5th and 7th Harmonic Components

Sometimes, 3rd, 5th and 7th harmonic components all need to be considered, which gives the optimal capacitances

$$\begin{cases} C_1 = \frac{1891}{33075(\omega^*)^2 L} \\ C_2 = \frac{3103726706488176928}{165531842759615479875(\omega^*)^2 L} \approx \frac{1}{54(\omega^*)^2 L} \\ C_3 = \frac{3103726706488176928}{595826230701116653875(\omega^*)^2 L} \approx \frac{1}{192(\omega^*)^2 L} \end{cases} \quad (5.35)$$

and

$$\begin{cases} L_2 = \frac{3363427011608657}{1641315021939808}L \approx 2L \\ L_3 = \frac{813103529745845}{102582188871238}L \approx 8L \end{cases} \quad (5.36)$$

with

$$\begin{cases} K_1 = 0.4853 \\ K_2 = 2.3031 \end{cases} \quad (5.37)$$

As a result, the output impedance is

$$Z_o(j\omega) = R - j\omega 17L \frac{\omega^{*2}(3.4e35\omega^4 + 2.2e38\omega^{*4} - 2.0e37\omega^2\omega^{*2})}{\omega^2(3.4e35\omega^4 + 3.1e38\omega^{*4} - 2.3e37\omega^2\omega^{*2})}. \quad (5.38)$$

At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j11\omega^*L \approx -j11\omega^*L \quad (5.39)$$

which is also nearly purely capacitive.

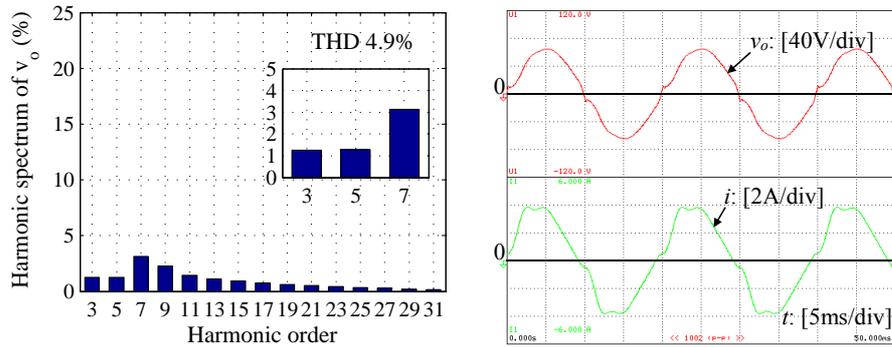
5.4 Experimental Results

In order to validate the proposed virtual resonant output impedance, experiments were performed with the test rig consisting of three single-phase inverters powered by three separate dc voltage supplies, as shown in Figure B.1(a). More detailed information can be found in Appendix B. In this chapter, only one of the three inverters of the experimental setup was used. The dc voltage supply is 80 V, and the a single-phase inverter is equipped with a robust droop controller proposed in Chapter 4. The filter inductor is $L = 3.5$ mH with a parasitic resistance of 0.5Ω and the filter capacitor C is $11\mu\text{F}$. The PWM switching frequency is 10 kHz, the line frequency of the system is 50 Hz. The rated load voltage of inverters is 48 V and $K_e = 20$. The desired voltage drop ratio $\frac{n_i S_i^*}{K_e E^*}$ is chosen to be 10% and the frequency boost ratio $\frac{m_i S_i^*}{\omega^*}$ to be 0.5%. The load is a full-bridge rectifier loaded with an inductor $L = 0.25$ mH and a resistor $R_L = 5\Omega$. The R-inverter is designed to has a 4Ω virtual resistance, and parameters of VRI are calculated according to the equations given in Section 5.2 with $R_c = 1000\Omega$. The experimental results when the inverter was designed to have different types of output impedance and with different levels of the virtual resonant impedance are shown in Figure 5.3 and Table 5.1.

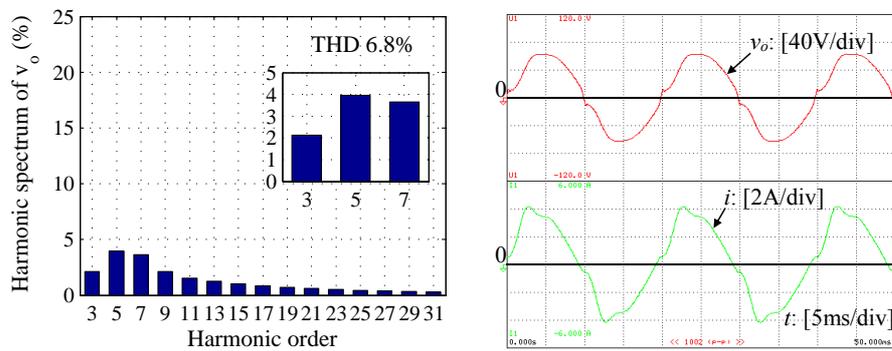
Table 5.1: Percentage harmonic values and THD of the v_o (%)

Harmonic Order	3rd and 5th	3rd	R-inverter	L-inverter
3	1.258	2.12	4.072	21.675
5	1.273	3.956	4.415	4.85
7	3.123	3.647	3.083	6.242
9	2.256	2.146	1.943	3.701
11	1.420	1.515	1.501	2.563
13	1.14	1.275	1.2	2.110
15	0.932	1.025	0.991	1.851
17	0.755	0.866	0.82	1.527
19	0.626	0.728	0.683	1.254
21	0.508	0.621	0.568	1.082
23	0.422	0.527	0.47	0.939
25	0.34	0.451	0.384	0.801
27	0.276	0.386	0.312	0.678
29	0.219	0.331	0.244	0.568
31	0.176	0.29	0.191	0.490
THD	4.9	6.8	7.5	23.9

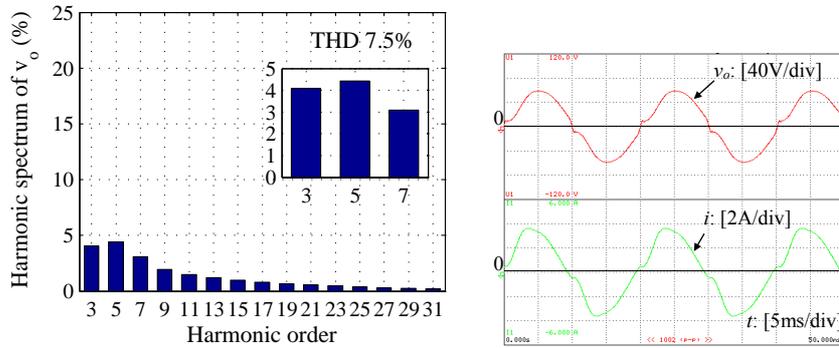
When the inverter was designed to have two levels of the virtual resonant impedance to reduce the effect of both 3rd and 5th harmonics, the THD was improved by 1.9% from the case with one level of the virtual resonant impedance to reduce 3rd harmonic, by nearly 2.6% from the case with a resistive output impedance (with $K_i = 4$), and by nearly 19% from the case with an inductive output impedance. Meanwhile, the 3rd harmonic distortion was improved by 0.86% from the case with one level of the virtual resonant impedance to reduce 3rd harmonic, by nearly 2.8% from the case with a resistive output impedance and by nearly 20.4% from the case with an inductive output impedance. The 5th harmonic distortion was improved by 2.7% from the case with one level of the virtual resonant impedance to reduce 3rd harmonic, by nearly 3.1% from the case with a resistive output impedance and by nearly 3.6% from the case with an inductive output impedance. Note that 2nd harmonic exists in the inductor current when the inverter has capacitive output impedance, which is caused by the nonlinear load. But the 2nd harmonic component of the load voltage is maintained very low, which is 0.045% in the case with one level of the virtual resonant impedance to reduce 3rd harmonic, and 0.032% the case with two levels of the virtual resonant impedance to reduce both 3rd and 5th harmonics.



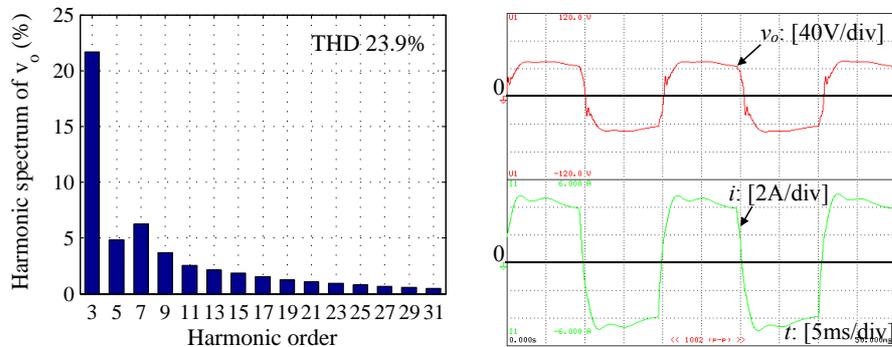
(a) Improved C-inverter (two levels with both 3rd and 5th harmonic components reduced)



(b) C-inverter (one level with 3rd harmonic component reduced)



(c) R-inverter



(d) L-inverter

Figure 5.3: Experimental results: harmonic distribution of the load voltage (left column), load voltage and inductor current (right column).

5.5 Summary

In this chapter, the virtual resonant impedance has been developed to improve the load voltage quality. It is achieved via a feedback of the inductor current through a transfer function, which is actually the expression of a resonant impedance topology consisting of inductors and capacitors. The parameters of the virtual resonant impedance have been optimised to reduce the magnitude at specified frequencies to reduce the load voltage harmonic. The feasibility and excellent performance of the virtual resonant impedance are demonstrated by the experimental results. It is shown that when the inverter is equipped with the virtual resonant impedance, the voltage harmonic is decreased further at the optimised orders and the voltage THD is also much improved compared with inverters with inductive, resistive or capacitive output impedance.

Chapter 6

Universal Droop Controller

As is well known, inverters could have different types of output impedance, which can be inductive, resistive, resistive-inductive (Guerrero et al., 2005; Zhong, 2013b), capacitive (Zhong and Zeng, 2011; 2014) or resistive-capacitive. Droop controllers have different forms for inverters with different types of output impedance (Zhong and Hornik, 2013). Because of this, it is impossible to operate inverters with different types of output impedance in parallel, which is inevitable for large-scale utilization of distributed generations and renewable energy sources.

After thoroughly considering this problem, a droop controller for C-, R- and R_C -inverters, called the R_C -controller, is proposed at first in this chapter. Then, the principles of the R_L -controller and the R_C -controller are further explored and clearly illustrated mathematically. Based on these principles, a universal transformation matrix T has been identified to develop a universal droop control principle that works for inverters with any types of output impedance having a phase angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad, for the first time, which covers any practical L-, R-, C-, R_L - and R_C -inverters. This universal droop control principle takes the form of the droop control principle for R-inverters and paves the way for designing universal droop controllers with different methods. In this chapter, the robust droop control mechanism proposed in (Zhong, 2013b) is added on to this droop control principle to provide one way to implement it, which turns out to be the same as the robust droop controller proposed in (Zhong, 2013b). The contribution of this chapter lies in revealing this universal droop control principle, mathematically proving it, implementing it and validating it with extensive experiments. Moreover, small-signal stability analysis is carried

out for inverters with different types of output impedance.

The rest of the chapter is organized as follows. In Section 6.1, the conventional droop controller is briefly reviewed with some new insights added. In Section 6.2, after reviewing the droop control strategy that is applicable to L-, R- and R_L -inverters, the droop control strategy that is applicable to C-, R- and R_C -inverters is proposed, together with some further developments for the two strategies (Zhong and Zeng, 2016). In Section 6.3, the universal droop control principle is developed and a universal droop controller to implement the principle is proposed, together with small-signal stability analysis. Extensive simulation and experimental results are provided in Section 6.5 and 6.6 for validation and conclusions are made in Section 6.7.

6.1 Droop Control for Inverters with the Same Type of Output Impedance

In this section, the widely-adopted droop control strategy is reviewed, with many new insights provided. An inverter can be modelled as a voltage source v_r in series with the output impedance $Z_o \angle \theta$, as shown in Figure 2.5(b). The real power and reactive power delivered from the voltage source v_r to the terminal v_o through the impedance $Z_o \angle \theta$ are described by (2.12) and (2.13). This characterizes a two-input-two-output control plant from the amplitude E and the phase δ of the source v_r to the real power P and the reactive power Q , as shown in the upper part of Figure 6.1.

The function of a droop control strategy is to generate appropriate amplitude E and phase δ for the inverter according to the measured P and Q , that is to close the loop, as shown in Figure 6.1. This sounds straightforward but, to the best knowledge of the author, this is the first time that the droop control of power inverters has been expressed in this way. This certainly helps understand the essence of droop control and motivates the design of other droop control strategies. Indeed, so far, the majority of the droop controllers are static rather than dynamic (Zhong and Boroyevich, 2013). Anyway, this is not the main concern of this chapter and will be further explored separately. In practice, it is often assumed that

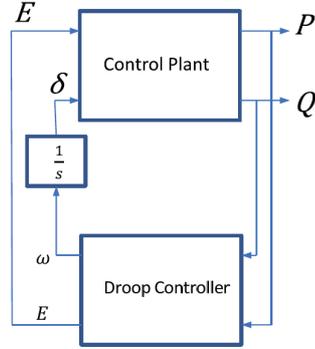


Figure 6.1: The closed-loop feedback system consisting of the power flow model of an inverter and the droop control strategy.

δ is small. In this case,

$$P \approx \left(\frac{EV_o}{Z_o} - \frac{V_o^2}{Z_o} \right) \cos \theta + \frac{EV_o}{Z_o} \delta \sin \theta \quad (6.1)$$

$$Q \approx \left(\frac{EV_o}{Z_o} - \frac{V_o^2}{Z_o} \right) \sin \theta - \frac{EV_o}{Z_o} \delta \cos \theta. \quad (6.2)$$

This leads to decoupled relationships between the inputs and the outputs, which change with the impedance angle θ . For example, when the output impedance is inductive ($\theta = \frac{\pi}{2}$ rad), P is roughly proportional to δ , noted as $P \sim \delta$, and Q is roughly proportional to E , noted as $Q \sim E$. According to this, the well-known droop control strategy, that is to droop the frequency when the real power increases and to droop the voltage when the reactive power increases, can be adopted. The cases when the inverter output impedance is resistive ($\theta = 0$ rad) and capacitive ($\theta = -\frac{\pi}{2}$ rad) can be analysed similarly, which results in different droop control strategies (Zhong and Hornik, 2013). The cases when the impedance is inductive (L-inverter), capacitive (C-inverter), resistive (R-inverter), resistive-capacitive (R_C-inverter) and resistive-inductive (R_L-inverter) are summarized in Table 6.1 for convenience. Apparently, the input-output relationships are different and so are the droop controllers. This holds true for the conventional droop controller as well as the robust droop controller (Zhong, 2013b), which is robust against the value variations of output impedance, component mismatches, parameter drifts, disturbances etc.

Table 6.1: Droop controllers for L-, R-, C-, R_L- and R_C-inverters

Inverter type	θ	Input-output/Droop relationship	Droop controller
L-	$\frac{\pi}{2}$	$P \sim \delta$	$E = E^* - nQ$
		$Q \sim E$	$\omega = \omega^* - mP$
R-	0°	$P \sim E$	$E = E^* - nP$
		$Q \sim -\delta$	$\omega = \omega^* + mQ$
C-	$-\frac{\pi}{2}$	$P \sim -\delta$	$E = E^* + nQ$
		$Q \sim -E$	$\omega = \omega^* + mP$
R _C -	$(-\frac{\pi}{2}, 0)$	Coupled	Depends on θ
R _L -	$(0, \frac{\pi}{2})$	Coupled	Depends on θ

As shown in Table 6.1, the droop control strategies change the form when the output impedance θ changes, thus it is difficult to operate inverters with different types of output impedance in parallel. In particular, the droop control strategies for L-inverters and C-inverters act in the opposite way and the parallel operation of a C-inverter with an L-inverter certainly does not work if these droop control strategies are employed.

6.2 Droop Control for Inverters with Different Types of Output Impedance

6.2.1 Parallel Operation of L-, R- and R_L-inverters

There have been some works (Brabandere et al., 2007; Yao et al., 2011; Bevrani and Shokoohi, 2013) reported in the literature to investigate the parallel operation of inverters with different types of output impedance, although they are limited to the parallel operation of L-, R- and R_L-inverters. This involves the introduction of the orthogonal transformation matrix

$$T_L = \begin{bmatrix} \sin \theta & -\cos \theta \\ \cos \theta & \sin \theta \end{bmatrix} \quad (6.3)$$

to convert the real power and the reactive power when $\theta \in (0, \frac{\pi}{2}]$ into

$$\begin{bmatrix} P_L \\ Q_L \end{bmatrix} = T_L \begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} \frac{EV_o}{Z_o} \sin \delta \\ \frac{EV_o}{Z_o} \cos \delta - \frac{V_o^2}{Z_o} \end{bmatrix}. \quad (6.4)$$

If δ is assumed small, roughly

$$P_L \sim \delta \quad \text{and} \quad Q_L \sim E \quad (6.5)$$

which results in the droop controller of the form

$$E = E^* - nQ_L \quad (6.6)$$

$$\omega = \omega^* - mP_L. \quad (6.7)$$

This is called the R_L -controller in order to facilitate the presentation in the sequel. Here, n and m are called droop coefficients. This controller has the same form as the droop controller for L-inverters but the impedance angle θ needs to be known in order to obtain the transformed power P_L and Q_L from (6.4); see (Brabandere et al., 2007; Yao et al., 2011; Bevrani and Shokoohi, 2013).

6.2.2 Parallel Operation of C-, R- and R_C -inverters

Following the same line of thinking as in the previous subsection, the transformation matrix

$$T_C = \begin{bmatrix} -\sin \theta & \cos \theta \\ -\cos \theta & -\sin \theta \end{bmatrix} \quad (6.8)$$

can be introduced for C-, R- or R_C -inverters with $\theta \in [-\frac{\pi}{2}, 0)$ to convert the real power and the reactive power into

$$\begin{bmatrix} P_C \\ Q_C \end{bmatrix} = T_C \begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} -\frac{EV_o}{Z_o} \sin \delta \\ -\frac{EV_o}{Z_o} \cos \delta + \frac{V_o^2}{Z_o} \end{bmatrix}. \quad (6.9)$$

In this case, for a small δ , roughly

$$P_C \sim -\delta \quad \text{and} \quad Q_C \sim -E \quad (6.10)$$

which results in the droop controller of the form

$$E = E^* + nQ_C \quad (6.11)$$

$$\omega = \omega^* + mP_C. \quad (6.12)$$

This is called the R_C -controller in order to facilitate the presentation in the sequel and it has the same form as the droop controller for C-inverters, which was proposed in (Zhong and Zeng, 2011; 2014). Again, the impedance angle θ needs to be known in order to obtain the transformed active power P_C and reactive power Q_C from (6.9). Apparently, this controller does not work for L- or R_L -inverters because of the negative signs in (6.6-6.7).

6.2.3 Further Development of the R_L -controller and the R_C -controller

The eigenvalues of T_L in (6.3) are $\sin \theta \pm j \cos \theta$, of which the real part $\sin \theta$ is positive for impedance with $\theta \in (0, \frac{\pi}{2}]$. According to the properties of the linear transformation (Poole, 2011) and the mapping described by (6.4), it can be seen that P and Q have positive correlations with P_L and Q_L , respectively. This can be described as

$$P \sim P_L \quad \text{and} \quad Q \sim Q_L. \quad (6.13)$$

So the relationship shown in (6.5) can be passed onto P and Q as

$$P \sim P_L \sim \delta \quad \text{and} \quad Q \sim Q_L \sim E. \quad (6.14)$$

In other words, for output impedance with $\theta \in (0, \frac{\pi}{2}]$, the real power P always has positive correlation with the power angle δ and the reactive power Q always has positive correlation with the voltage E . Hence, the R_L -controller can also be designed as

$$E = E^* - nQ \quad (6.15)$$

$$\omega = \omega^* - mP \quad (6.16)$$

which is directly related to the real power P and the reactive power Q , regardless of the impedance angle θ . In other words, the effect of the impedance angle θ has been removed as long as it satisfies $\theta \in (0, \frac{\pi}{2}]$.

In order to better understand the transformation matrix (6.3), the transformation (6.4) can actually be rewritten as

$$\begin{aligned} P_L + jQ_L &= P \sin \theta - Q \cos \theta + j(P \cos \theta + Q \sin \theta) \\ &= e^{j(\frac{\pi}{2}-\theta)}(P + jQ) \end{aligned}$$

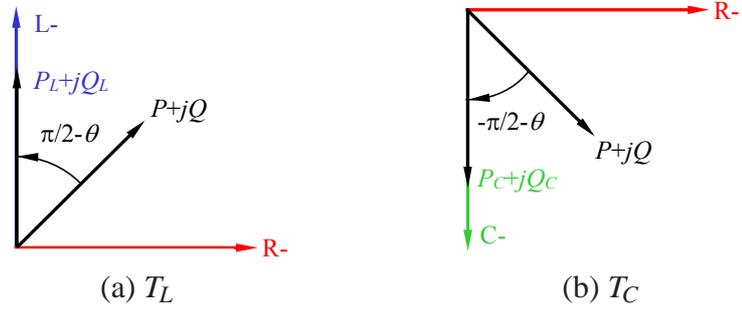


Figure 6.2: The interpretation of the transformation matrices T_L and T_C .

where $j = \sqrt{-1}$. In other words, the transformation (6.3) rotates the power vector $P + jQ$ by $\frac{\pi}{2} - \theta$ rad onto an axis aligned with the L -inverter, as shown in Figure 6.2(a), so that the droop controller (6.15-6.16) can be formed.

Similarly, for the R_C -controller, the eigenvalues of T_C in (6.8) are $-\sin \theta \pm j \cos \theta$, of which the real part $-\sin \theta$ is positive for any output impedance with $\theta \in [-\frac{\pi}{2}, 0)$. Hence, according to the mapping described by (6.9), P and Q have positive correlations with P_C and Q_C , respectively. This can be described as

$$P \sim P_C \quad \text{and} \quad Q \sim Q_C. \quad (6.17)$$

So the relationship shown in (6.10) can be passed onto P and Q as

$$P \sim P_C \sim -\delta \quad \text{and} \quad Q \sim Q_C \sim -E. \quad (6.18)$$

In other words, for impedance with $\theta \in [-\frac{\pi}{2}, 0)$, the real power P always has negative correlation with the power angle δ and the reactive power Q always has negative correlation with the voltage E . Then, the R_C -controller can also be designed as

$$E = E^* + nQ \quad (6.19)$$

$$\omega = \omega^* + mP \quad (6.20)$$

which is also directly related to the real power P and the reactive power Q . The effect of the impedance angle θ has been removed as long as it satisfies $\theta \in [-\frac{\pi}{2}, 0)$.

Also similarly, in order to better understand the transformation matrix (6.8), the trans-

formation (6.9) can be rewritten as

$$\begin{aligned} P_C + jQ_C &= -P \sin \theta + Q \cos \theta + j(-P \cos \theta - Q \sin \theta) \\ &= e^{j(-\frac{\pi}{2}-\theta)}(P + jQ). \end{aligned}$$

In other words, the transformation (6.8) actually rotates the power vector $P + jQ$ by $-\frac{\pi}{2} - \theta$ rad onto an axis aligned with the C -inverter, as shown in Figure 6.2(b), to form the droop controller (6.19-6.20).

Therefore, the R_L -controller (6.15-6.16) can be applied to inverters with the output impedance satisfying $\theta \in (0, \frac{\pi}{2}]$ and the R_C -controller can be applied to inverters with the output impedance satisfying $\theta \in [-\frac{\pi}{2}, 0)$. This widens the application range of the L-controller and the C-controller. However, the R_L -controller cannot be applied to C- or R_C -inverters and the R_C -controller cannot be applied to L- or R_L -inverters. There is still a need to develop a controller that is applicable to L-, R-, C-, R_L - and R_C -inverters.

6.3 Universal Droop Controller

6.3.1 Basic Principles

Following the above analysis, it would be great if a transformation matrix that is able to project the power vector onto the same axis for any impedance angle θ could be found. The transformation matrix

$$T = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \quad (6.21)$$

achieves this and it transforms the real power P and the reactive power Q to

$$\begin{bmatrix} P_R \\ Q_R \end{bmatrix} = T \begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} \frac{EV_o}{Z_o} \cos \delta - \frac{V_o^2}{Z_o} \\ -\frac{EV_o}{Z_o} \sin \delta \end{bmatrix}. \quad (6.22)$$

This transformation can be rewritten as

$$\begin{aligned} P_R + jQ_R &= P \cos \theta + Q \sin \theta + j(-P \sin \theta + Q \cos \theta) \\ &= e^{-j\theta}(P + jQ). \end{aligned}$$

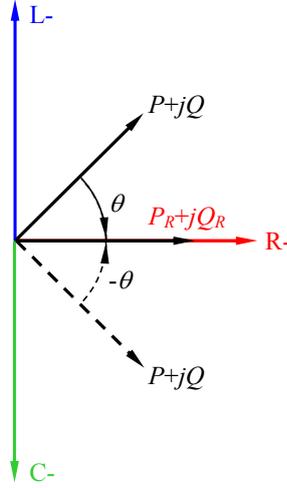


Figure 6.3: The interpretation of the transformation matrix T .

As shown in Figure 6.3, this transformation rotates the power vector $P + jQ$ by $-\theta$ onto an axis aligned with the R -inverter, clockwise when $\theta \in [0, \frac{\pi}{2})$ and counter-clockwise when $\theta \in (-\frac{\pi}{2}, 0]$. The eigenvalues of T in (6.21) are $\cos \theta \pm j \sin \theta$, of which the real part $\cos \theta$ is positive for any output impedance with $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$. According to the properties of the linear transformation (Poole, 2011) and the mapping described by (6.22), P and Q are proven to have positive correlations with P_R and Q_R , respectively. This can be described as

$$P \sim P_R \quad \text{and} \quad Q \sim Q_R. \quad (6.23)$$

According to (6.22), for a small δ , there are

$$P_R \sim E \quad \text{and} \quad Q_R \sim -\delta. \quad (6.24)$$

Combining these two, there is

$$P \sim P_R \sim E \quad \text{and} \quad Q \sim Q_R \sim -\delta \quad (6.25)$$

for any $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$. This basically indicates that the real power P always has positive correlation with the voltage E and the reactive power Q always has negative correlation with the power angle δ for any impedance angle $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$. This results in the following

conventional universal droop controller

$$E = E^* - nP \quad (6.26)$$

$$\omega = \omega^* + mQ \quad (6.27)$$

which is applicable to inverters with any type of output impedance satisfying $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$. Note that this droop controller (6.26-6.27) takes the form of the droop controller for R-inverters. The main contribution of this chapter is actually to have revealed this fact and formally proven it. Theoretically, when the impedance is purely inductive ($\theta = \frac{\pi}{2}$ rad) or capacitive ($\theta = -\frac{\pi}{2}$ rad), this relationship does not hold but, in practice, there is always an equivalent series resistance (ESR) in series with the filter inductor so the controller (6.26-6.27) is actually applicable to all practical L-, R-, C-, R_L - and R_C -inverters.

6.3.2 Implementation

There are many ways to implement the universal droop control principle revealed in the previous subsection. In this chapter, the thinking along the line of the robust droop control proposed in (Zhong, 2013b; Zhong and Hornik, 2013) is followed.

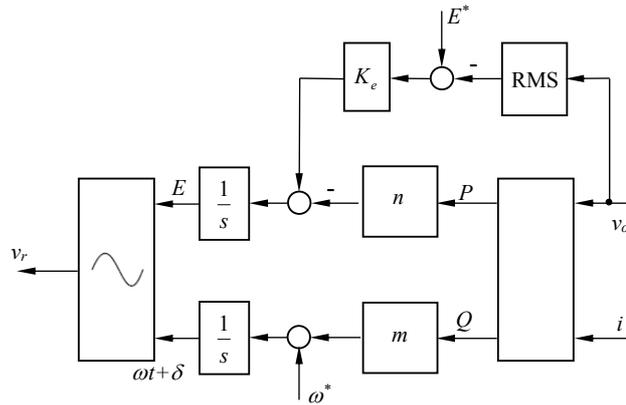


Figure 6.4: The proposed universal droop controller, which takes the form of the robust droop controller for R-inverters reported in (Zhong, 2013b).

As reported in (Zhong, 2013b), the conventional droop control is not able to achieve tight voltage regulation and accurate power sharing in the presence of numerical errors, noises, disturbances, component mismatches and parameter shifts etc. This is the same for

the droop control principle derived in the previous subsection. In order to address these issues, the robust droop control strategy proposed in (Zhong, 2013b) can be adopted to form the universal droop controller, as shown in Figure 6.4. Actually, it takes the same form as the robust droop controller for R-inverters reported in (Zhong, 2013b) with

$$\dot{E} = K_e(E^* - V_o) - nP \quad (6.28)$$

$$\omega = \omega^* + mQ. \quad (6.29)$$

In the steady state, there is

$$nP = K_e(E^* - V_o) \quad (6.30)$$

which means

$$nP = \text{constant} \quad (6.31)$$

as long as K_e is the same for all inverters. This guarantees the accurate sharing of real power in proportion to their rating. As long as the system is stable, which leads to the same frequency, the accurate sharing of reactive power is guaranteed as well (Zhong, 2013b).

According to (6.30), the load voltage is

$$V_o = E^* - \frac{nP}{K_e E^*} E^* \quad (6.32)$$

which can be maintained within the desired range via choosing a large K_e . Hence, the universal droop controller has very good capability of voltage regulation and accurate power sharing. This is the same for the inverters with resistive (and inductive) output impedance reported in (Zhong, 2013b). The droop coefficients n and m , as well as K_e , can be determined by the desired voltage drop ratio $\frac{nP^*}{K_e E^*}$ and the frequency boost ratio $\frac{mQ^*}{\omega^*}$, respectively, where P^* and Q^* are the rated real power and reactive power of the inverter.

Although this controller is not new and its excellent performance is known, what is important is that it has now been proven that this controller is applicable to all practical L-, R-, C-, R_L - and R_C -inverters to address the challenging problem of operating inverters with different types of output impedance in parallel.

6.4 Small-signal Stability

6.4.1 With the Conventional Form

Here, the small-signal stability of one inverter equipped with the conventional universal droop controller (6.26-6.27) is analysed. Considering small disturbances around the stable equilibrium operation point (δ_e, V_{oe}, E_e) , where E_e is the magnitude of the inverter source voltage, V_{oe} is the magnitude of the load voltage and δ_e is the phase angle difference between the inverter source voltage and the load voltage. Linearising (2.12) and (2.13) around the equilibrium:

$$\begin{aligned} \Delta P(s) = & \frac{V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)}{Z_o} \Delta E(s) \\ & + \frac{E_e V_{oe}(-\sin \delta_e \cos \theta + \cos \delta_e \sin \theta)}{Z_o} \Delta \delta(s) \end{aligned} \quad (6.33)$$

$$\begin{aligned} \Delta Q(s) = & \frac{V_{oe}(\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)}{Z_o} \Delta E(s) \\ & - \frac{E_e V_{oe}(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o} \Delta \delta(s). \end{aligned} \quad (6.34)$$

Similarly, the conventional universal controller (6.26-6.27) can be linearised around the equilibrium as

$$\begin{aligned} \Delta E(s) &= -n \Delta P(s) \\ \Delta \omega &= m \Delta Q(s). \end{aligned}$$

Additionally, there is

$$\Delta \omega(s) = s \Delta \delta(s). \quad (6.35)$$

Taking into account the fact that it is a normal practice to filter the active power and the reactive power with a low pass filter $\frac{\omega_f}{s + \omega_f}$, the small-signal model of the closed-loop system

described above, as depicted in Figure 6.1, satisfies

$$\Delta E(s) = \frac{-n\omega_f}{s + \omega_f} \left[\frac{V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)}{Z_o} \Delta E(s) + \frac{E_e V_{oe}(-\sin \delta_e \cos \theta + \cos \delta_e \sin \theta)}{Z_o} \Delta \delta(s) \right] \quad (6.36)$$

$$\Delta \omega(s) = \frac{m\omega_f}{s + \omega_f} \left[\frac{V_{oe}(\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)}{Z_o} \Delta E(s) - \frac{E_e V_{oe}(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o} \Delta \delta(s) \right]. \quad (6.37)$$

Combining (6.35), (6.36) and (6.37) results in the following homogeneous equation

$$as^3 \Delta \delta(s) + bs^2 \Delta \delta(s) + cs \Delta \delta(s) + d \Delta \delta(s) = 0 \quad (6.38)$$

with

$$\begin{aligned} a &= Z_o^2 \\ b &= Z_o \omega_f (2Z_o + nV_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)) \\ c &= Z_o \omega_f (Z_o \omega_f + (mE_e + n\omega_f)V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)) \\ d &= m\omega_f^2 E_e V_{oe} [nV_{oe} + Z_o(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)]. \end{aligned} \quad (6.39)$$

The system stability can be analysed by investigating the characteristic equation

$$as^3 + bs^2 + cs + d = 0. \quad (6.40)$$

The root-locus plot of this characteristic equation when the impedance angle θ changes from $-\frac{\pi}{2}$ to $\frac{\pi}{2}$ is shown in Figure 6.5 using the parameters from the experimental system to be described later in Section 6.6. The rated system frequency is 50 Hz and the rated load voltage is 12 V. The load is a 3.8Ω resistor in series with two 2.2 mH inductors. The droop coefficients are $n = 0.02$ and $m = 0.01$. It is assumed that V_{oe} remains constant with $V_{oe} = 11$ V at the equilibrium independently when the inverter output impedance angle θ changes. According to (6.26), there is $E_e = 11.43$ V. Under this assumption, the δ_e changes with θ , as shown in Figure 6.6. As can be seen from Figure 6.5, the roots are always located in the left half of the s -plane, which indicates that the stability is always guaranteed

when the inverter is equipped with the conventional droop controller, independently from the type of the output impedance, as long as the phase angle satisfies $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$.

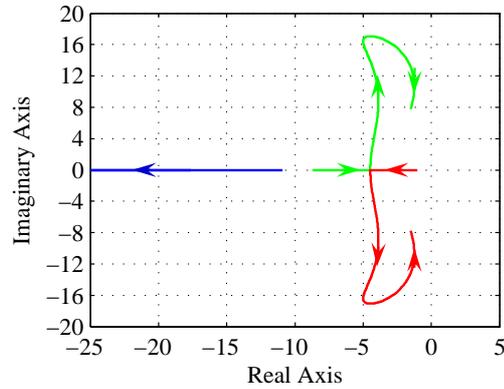


Figure 6.5: The root loci of the small-signal model of the closed-loop system (6.40) when θ changes from $-\frac{\pi}{2}$ to $\frac{\pi}{2}$.

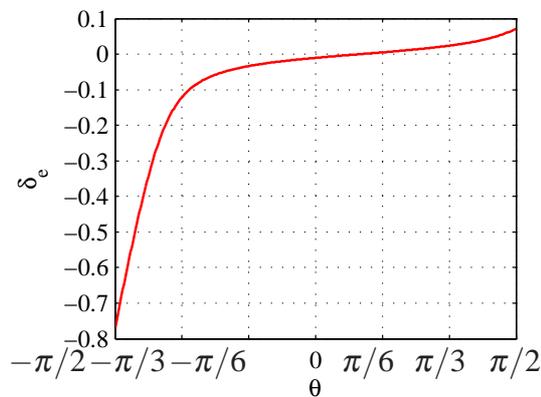


Figure 6.6: The value of δ_e when θ changes from $-\frac{\pi}{2}$ to $\frac{\pi}{2}$.

6.4.2 With the Robust Form

Similarly, the controller (6.28-6.29) can be linearised around the equilibrium as

$$s\Delta E(s) = -n\Delta P(s)$$

$$\Delta\omega(s) = m\Delta Q(s).$$

Additionally, there is

$$\Delta\omega(s) = s\Delta\delta(s). \quad (6.41)$$

Considering the low pass filter $\frac{\omega_f}{s+\omega_f}$ used in the real power and the reactive power measurement, the small-signal model of the closed-loop system is

$$\begin{aligned} s\Delta E(s) &= -n \cdot \frac{\omega_f}{s+\omega_f} \cdot \left[\frac{V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)}{Z_o} \Delta E(s) \right. \\ &\quad \left. + \frac{E_e V_{oe}(-\sin \delta_e \cos \theta + \cos \delta_e \sin \theta)}{Z_o} \Delta \delta(s) \right] \end{aligned} \quad (6.42)$$

$$\begin{aligned} s\Delta \delta(s) &= m \cdot \frac{\omega_f}{s+\omega_f} \cdot \left[\frac{V_{oe}(\cos \delta_e \sin \theta - \sin \delta_e \cos \theta)}{Z_o} \Delta E(s) \right. \\ &\quad \left. - \frac{E_e V_{oe}(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o} \Delta \delta(s) \right] \end{aligned} \quad (6.43)$$

which leads to the following fourth-order homogeneous equation

$$as^4\Delta\delta(s) + bs^3\Delta\delta(s) + cs^2\Delta\delta(s) + ds\Delta\delta(s) + e\Delta\delta(s) = 0 \quad (6.44)$$

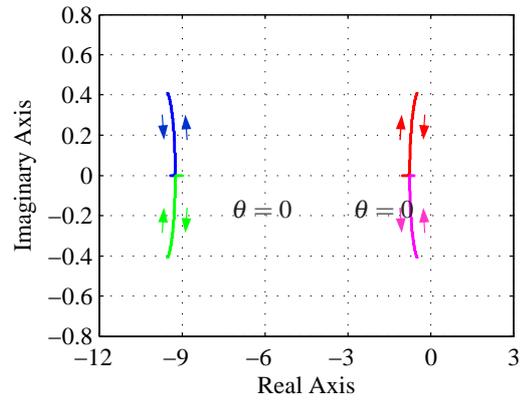
with

$$\begin{aligned} a &= Z_o^2 \\ b &= 2Z_o^2\omega_f \\ c &= Z_o\omega_f(V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)(n + mE_e) + Z_o\omega_f) \\ d &= Z_o\omega_f^2V_{oe}(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)(n + mE_e) \\ e &= mE_en\omega_f^2V_{oe}^2. \end{aligned} \quad (6.45)$$

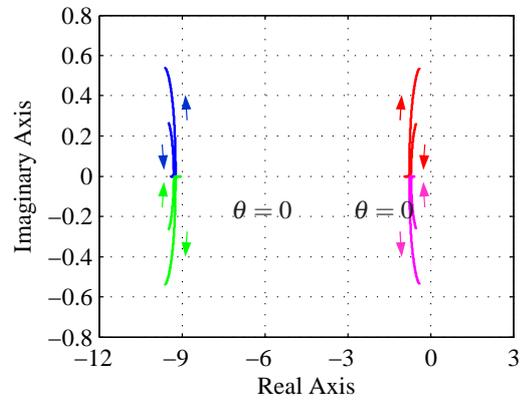
The system stability can be analysed by investigating the characteristic equation

$$as^4 + bs^3 + cs^2 + ds + e = 0. \quad (6.46)$$

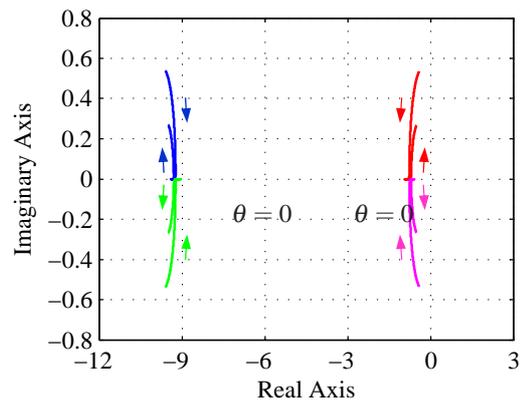
The root-locus plots of this characteristic equation when θ changes from $-\frac{\pi}{2}$ rad to $\frac{\pi}{2}$ rad are shown in Figure 6.7 for three cases of different loads, using the parameters from the experimental system to be described later in Section 6.6.



(a) with a resistive load $R = 8\Omega$



(b) with a resistive-inductive load $7.6 + 2.76j$



(c) with a resistive-capacitive load $7.6 - 2.76j$

Figure 6.7: The root loci of the small-signal model of the closed-loop system (6.46) when θ changes from $-\frac{\pi}{2}$ to $\frac{\pi}{2}$.

The rated system frequency is 50 Hz and the rated load voltage is 12 V, with $n = 0.48$ and $m = 0.03$. According to (6.32), V_{oe} is independent from the output impedance angle

θ . Thus, as long as the load is unchanged and n , K_e , E^* are fixed, it remains as a constant at the equilibrium when the inverter output impedance angle θ changes. E_e changes with impedance angle θ but can be calculated according to V_{oe} and a given load. For all these cases, the roots are always located in the left half of the s -plane, which indicates that the stability is guaranteed when the inverter is equipped with the universal droop controller, independently from the type of the output impedance, as long as the phase angle satisfies $\theta \in (-\frac{\pi}{2}, \frac{\pi}{2})$. When the load is purely resistive, the roots when θ changes from $-\frac{\pi}{2}$ rad to 0 overlap with the roots when θ changes from 0 to $\frac{\pi}{2}$ rad, as shown in Figure 6.7(a). When the load is resistive-inductive the roots move in the opposite direction of those when the load is resistive-capacitive, as shown in Figures 6.7(b) and 6.7(c).

6.5 Simulation Results

To demonstrate the feasibility of the universal droop controller, simulations were carried out with MATLAB 2013a, toolboxes such as Simulink and Simscape were extensively used. The solver used in the simulations was Tustin with a relative tolerance of 10^{-3} and the sampling time is $1 \mu\text{F}$. More detailed information can be found in Appendix A. The inverter system consisted of two single-phase inverters powered by two separate 400 V dc voltage supplies and with a linear load $R = 57 \Omega$.

6.5.1 Case I: Parallel Operation of Two Inverters

The ratings of Inverter 1 and 2 were 0.5 kVA and 1 kVA, respectively. It is expected that $P_2 = 2P_1$ and $Q_2 = 2Q_1$. The PWM switching frequency was 15 kHz and the line frequency of the system was 50 Hz. The rated load voltage of inverters was 230 V and $K_e = 10$. The filter inductor was $L = 0.55 \text{ mH}$ with a parasitic resistance of 0.3Ω and the filter capacitor C was $20 \mu\text{F}$. The desired voltage drop ratio $\frac{n_i S_i^*}{K_e E^*}$ is chosen to be 0.25% and frequency boost ratio $\frac{m_i S_i^*}{\omega^*}$ to be 0.1%. As a result, for the universal droop controller, L-controller and C-controller, there are $n_1 = 0.0115$ and $n_2 = 0.0057$; $m_1 = 6.2832e^{-4}$ and $m_2 = 3.1416e^{-4}$.

To verify the design, the proposed universal droop controller is applied to parallel-operated inverters with different types of output impedance, which include parallel-connected L-inverters (L&L), R-inverters (R&R), C-inverters (C&C), R_C -inverters (R_C & R_C), L-inverter

and R-inverter (L&R), L-inverter and C-inverter (L&C), L-inverter and R_C -inverter (L& R_C), R-inverter and C-inverter (R&C), R-inverter and R_C -inverter (R& R_C), as well as C-inverter and R_C -inverter (C& R_C). Because of the filter inductor, the output impedance of the inverter would be inductive (the L-inverter) if no current loop is added to change its type. The R-inverter is designed with a virtual resistor $R = 1\ \Omega$ via a current loop proposed in (Zhong, 2013b; Guerrero et al., 2005); the C-inverter is designed with a virtual capacitor $C_o = \frac{1}{(3\omega^*)^2 L} = 2046.9\ \mu\text{F}$ via a current loop proposed in (Zhong and Zeng, 2011). As shown in Figure 6.8, the R_C -inverter is designed with a virtual resistor $R = 1\ \Omega$ and a virtual capacitor $C_o = \frac{1}{(3\omega^*)^2 L} = 2046.9\ \mu\text{F}$ via a current loop shown in Figure 6.8.

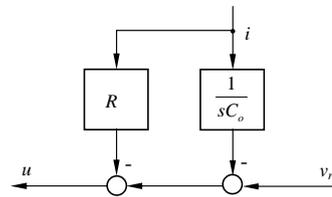


Figure 6.8: A controller to achieve the R_C -inverter.

As shown in Table 6.2 and Figure 6.9-6.18, the universal droop controller worked very well for all cases of two parallel operated inverters without causing instability:

- 1) the real power and reactive power were accurately shared in the ratio of 2:1;
- 2) the load voltage was maintained close to the rated voltage and the frequency close to the rated frequency even when the inverters in parallel were with different types of output impedance;
- 3) the dynamic performance was excellent - it was fast and with very small overshoot.

Table 6.2: Steady-state performance of two parallel operated inverters with UDC

Variable	L-&L-	R-&R-	C-&C-	R_C -& R_C -	L-&R-
Apparent power 1 (VA)	306.87-242.71j	306.44-242.79j	307.48-242.59j	306.73-242.87j	307.06-242.97j
Apparent power 2 (VA)	618.05-485.69j	618.67-485.77j	617.44-485.81j	618.38-485.68j	618.04-485.56j
RMS load voltage (V)	229.64	229.65	229.65	229.65	229.65
Frequency f (Hz)	49.98	49.98	49.98	49.98	49.98
Variable	L-&C-	L-& R_C	C-&R-	C-& R_C -	R_C -&R-
Apparent power 1 (VA)	307.08-242.97j	307.49-242.728j	307.94-242.93j	307.02-242.83j	307.10-243.00j
Apparent power 2 (VA)	617.84-485.43j	617.60-485.80j	617.15-485.60j	618.07-485.71j	617.99-485.54j
RMS load voltage (V)	229.65	229.64	229.65	229.65	229.64
Frequency f (Hz)	49.98	49.98	49.98	49.98	49.98

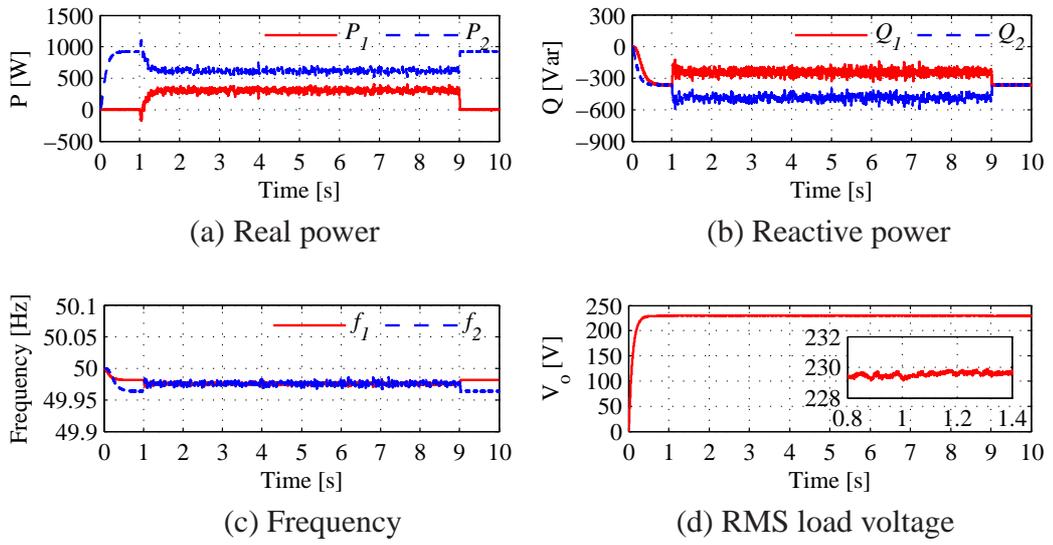


Figure 6.9: Simulation results for the parallel operation of two L-inverters

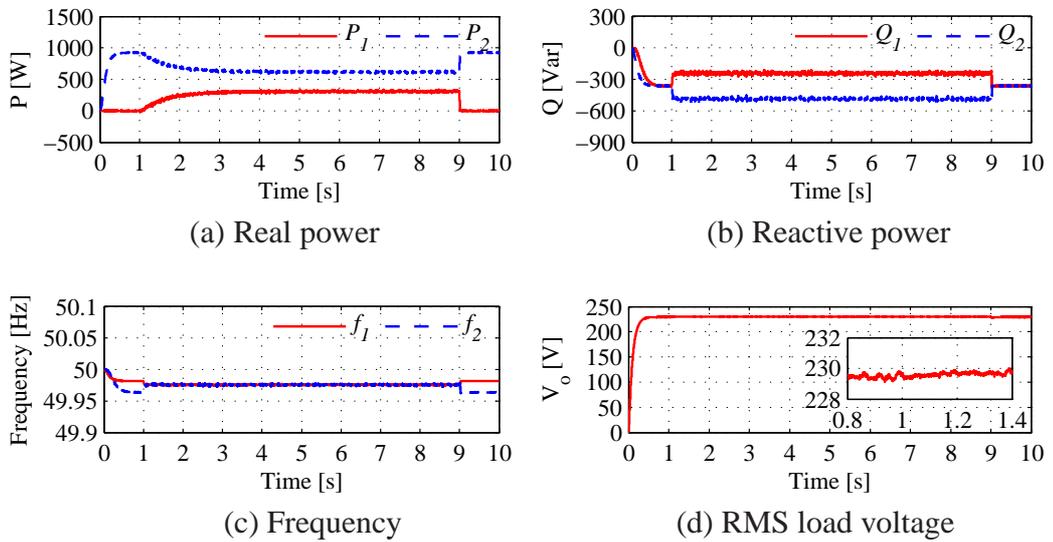


Figure 6.10: Simulation results for the parallel operation of two R-inverters

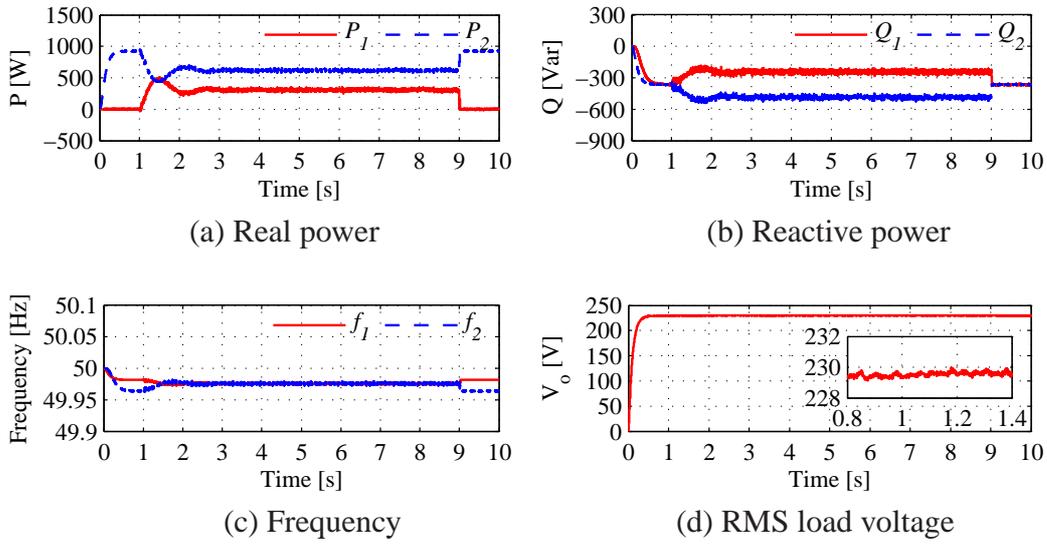


Figure 6.11: Simulation results for the parallel operation of two C-inverters

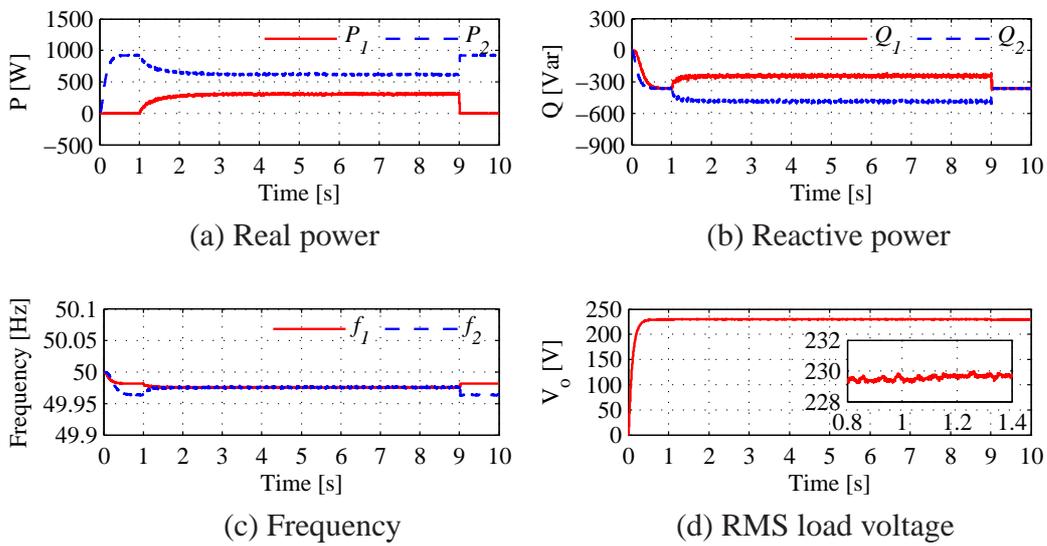


Figure 6.12: Simulation results for the parallel operation of two R_C -inverters

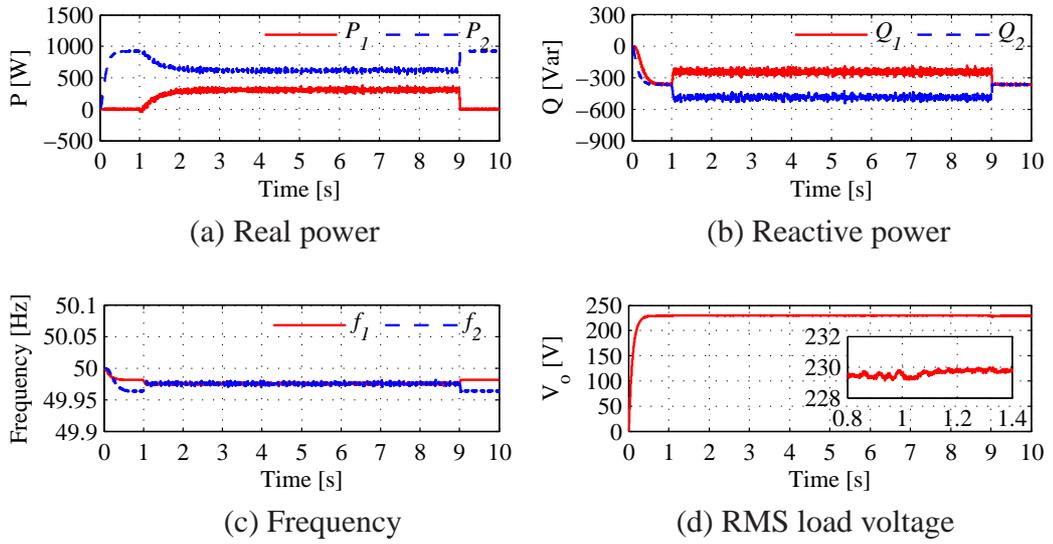


Figure 6.13: Simulation results for the parallel operation of an L-inverter & an R-inverter.

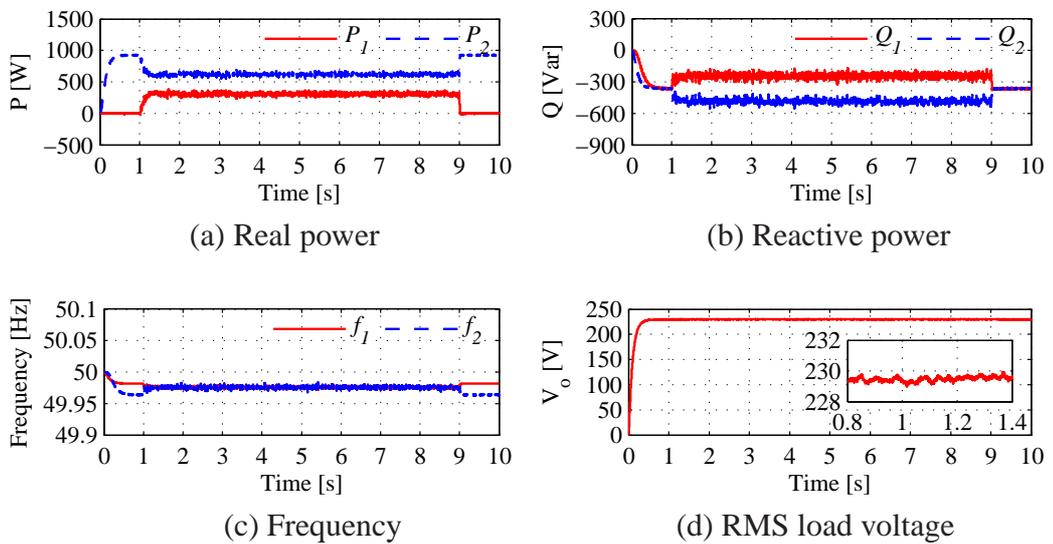


Figure 6.14: Simulation results for the parallel operation of an L-inverter & a C-inverter.

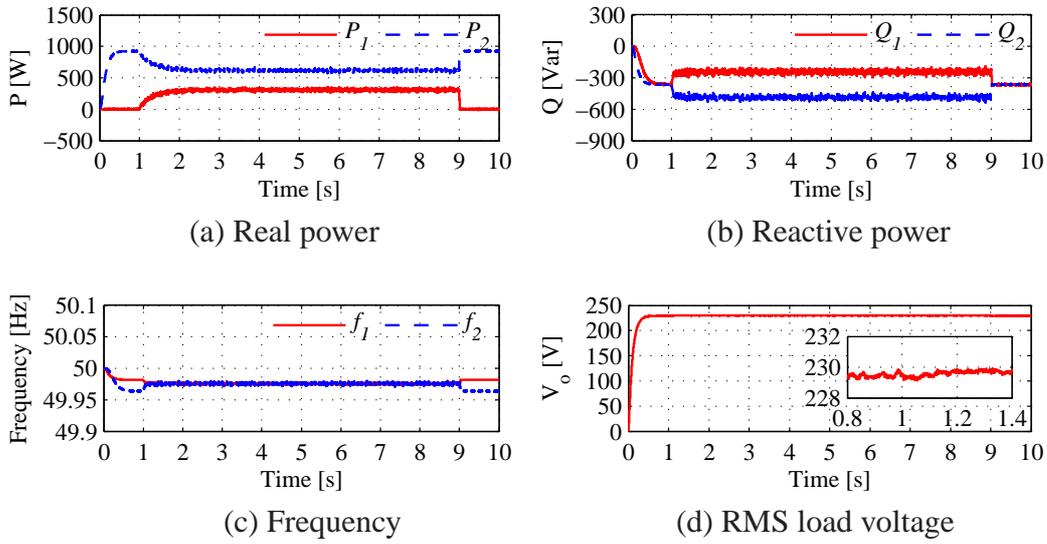


Figure 6.15: Simulation results for the parallel operation of an L-inverter & an RC-inverter.

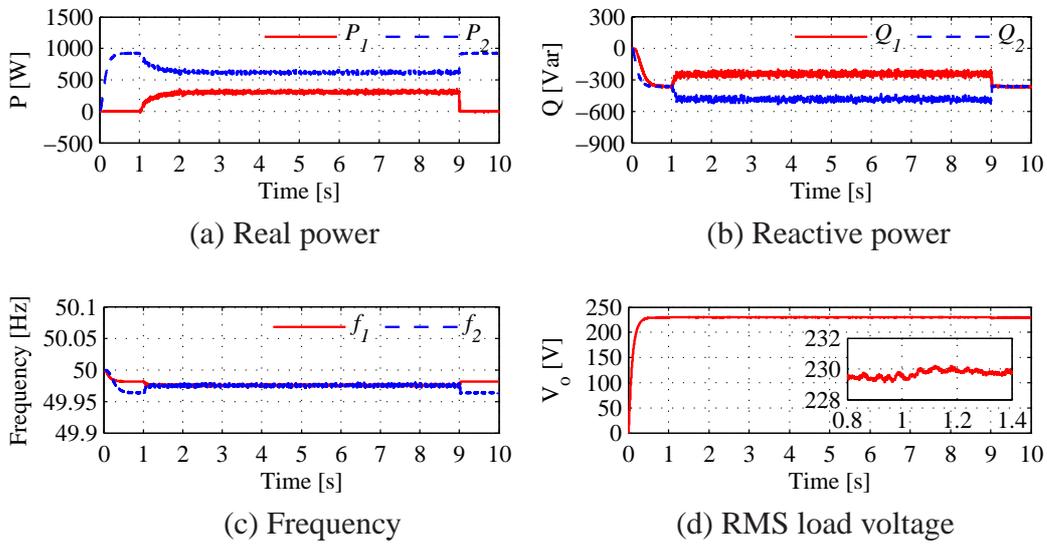


Figure 6.16: Simulation results for the parallel operation of a C-inverter & an R-inverter.

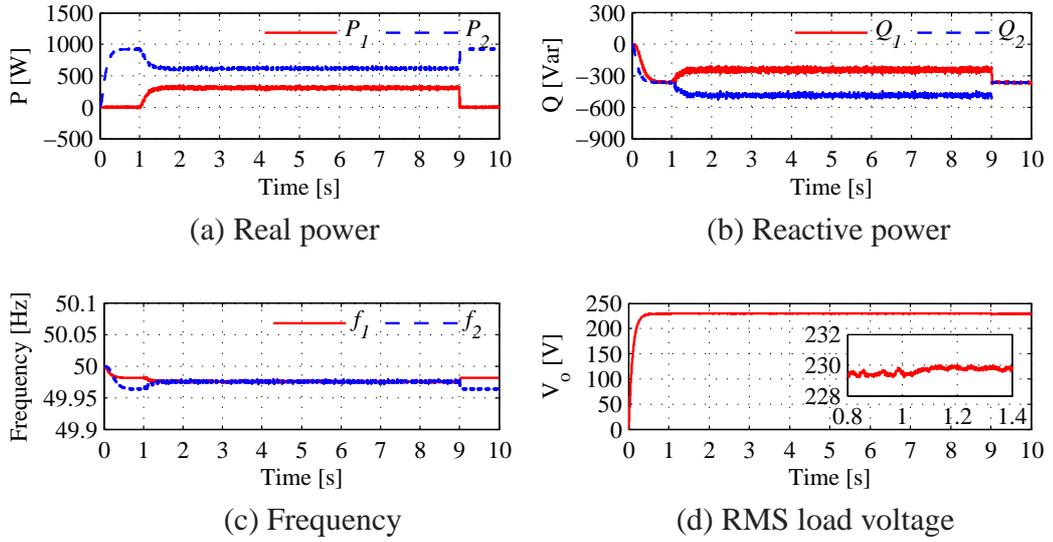


Figure 6.17: Simulation results for the parallel operation of a C-inverter & an R_C -inverter.

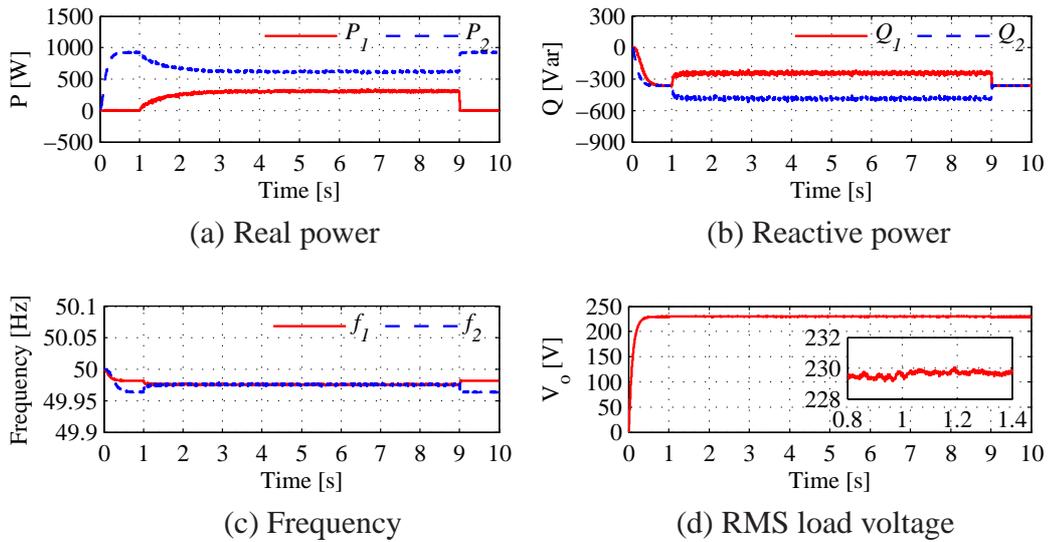
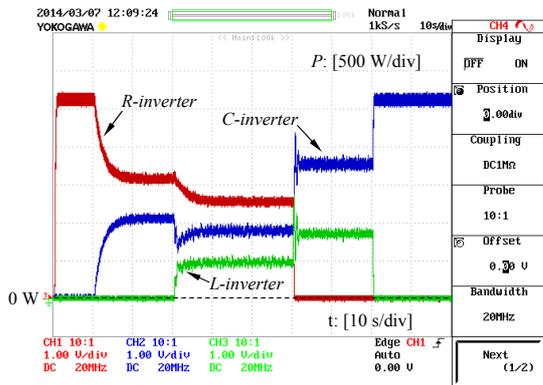


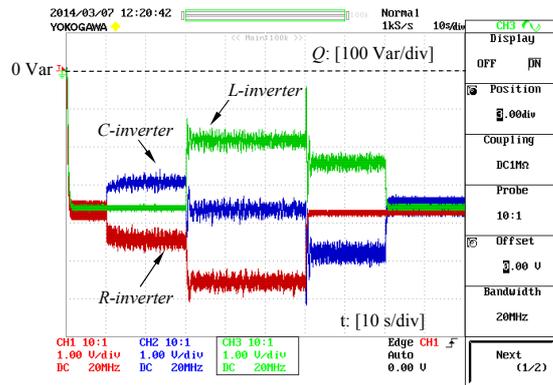
Figure 6.18: Simulation results for the parallel operation of an R_C -inverter & an R-inverter.

6.5.2 Case II: Parallel Operation of Three Inverters

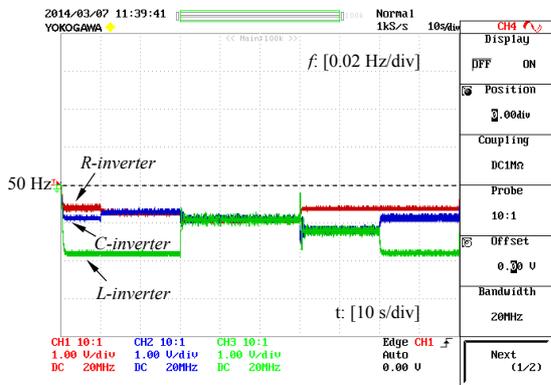
In order to further validate the proposed robust universal droop controller, real-time simulations were carried out on an OPAL RT real-time digital simulator. Three single-phase inverters powered by three separate 400 V dc voltage supplies were operated together to power a 20Ω linear load. The capacities of Inverters 1 (L-inverter), 2 (C-inverter) and 3 (R-inverter with a virtual 4Ω resistor) were 1 kVA, 2 kVA and 3kVA, respectively.



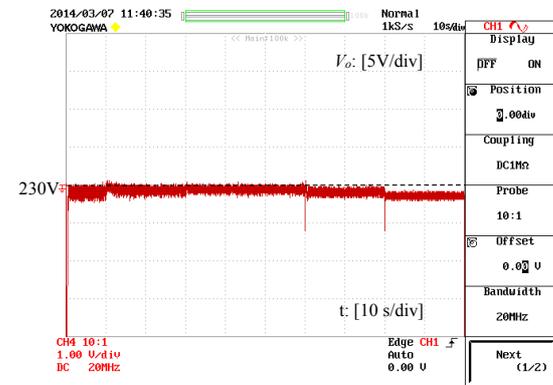
(a) Real power



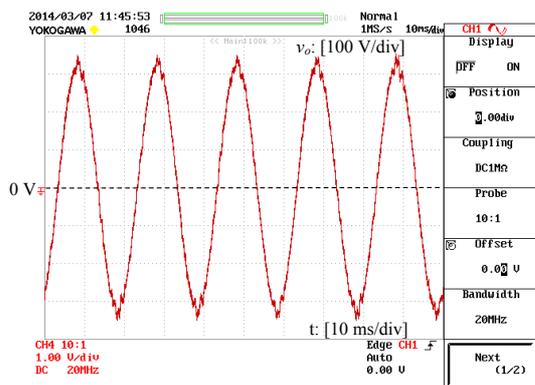
(b) Reactive power



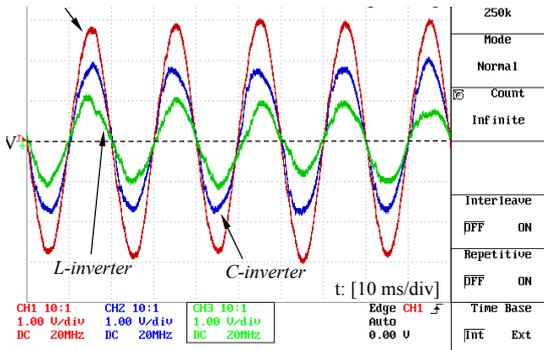
(c) Frequency



(d) RMS load voltage



(e) Load voltage



(f) Inductor current

Figure 6.19: Real-time simulation results of the parallel operation of an L-inverter, a C-inverter and an R-inverter.

It is expected that $P_2 = 2P_1$, $Q_2 = 2Q_1$, $P_3 = 3P_1$ and $Q_3 = 3Q_1$. The PWM switching frequency was 10 kHz and the line frequency of the system was 50 Hz. The rated load voltage was 230 V and $K_e = 10$. The filter inductor was $L = 0.55$ mH with a parasitic

resistance of $0.3\ \Omega$ and the filter capacitor C was $20\ \mu\text{F}$. The desired voltage drop ratio $\frac{n_i S_i^*}{K_e E^*}$ was chosen as 0.25% and the frequency boost ratio $\frac{m_i S_i^*}{\omega^*}$ was 0.1% so the droop coefficients are $n_1 = 0.0057$, $n_2 = 0.0029$, $n_3 = 0.0019$, $m_1 = 3.1416 \times 10^{-4}$, $m_2 = 1.5708 \times 10^{-4}$ and $m_3 = 1.0472 \times 10^{-4}$.

The real-time simulation results are shown in Figure 6.19. At $t = 0$ s, the three inverters were operated separately with the load connected to the R-inverter only. Then, at $t = 10$ s, the C-inverter was connected in parallel with the R-inverter and the two inverters shared the real power and reactive power accurately in the ratio of 2:3.

At $t = 30$ s, the L-inverter was put into parallel operation. The three inverters shared the real power and reactive power accurately in the ratio of 1:2:3. Then the R-inverter was disconnected at $t = 60$ s and the C-inverter and the L-inverter shared the power accurately in the ratio of 2:1. Finally, the L-inverter was disconnected at $t=80$ s and the load was powered by the C-inverter only. The frequency and the voltage were regulated to be very close to the rated values, respectively, as can be seen from Figure 6.19(c) and (d).

The waveforms of the load voltage and the inductor currents of the three inverters after taking away the switching ripples with a hold filter when the three inverters were in parallel operation are shown in Figure 6.19(e) and (f). It can be seen that indeed the three inverters shared the load accurately in the ratio of 1:2:3.

6.6 Experimental Validation

In order to validate the proposed universal droop controller, the experiment was carried out with a system consisting of three inverters operated in parallel, as shown in Figure B.1(a). More detailed information can be found in Appendix B. These three single-phase inverters are powered by three separate 30 V dc voltage supplies and loaded with a $3.8\ \Omega$ resistor in series with two 2.2 mH inductors. Since the aim of this chapter is to address the parallel operation of inverters with different types of output impedance, the case with a nonlinear load is not considered. The original inverters include a filter inductor $L = 7$ mH with a parasitic resistance of $1\ \Omega$ and a filter capacitor $C = 1\ \mu\text{F}$. The PWM switching frequency is 10 kHz; the line frequency of the system is 50 Hz and the cut-off frequency ω_f of the measuring filter is 10 rad/s. The rated load voltage of the inverters is 12 V and $K_e = 20$.

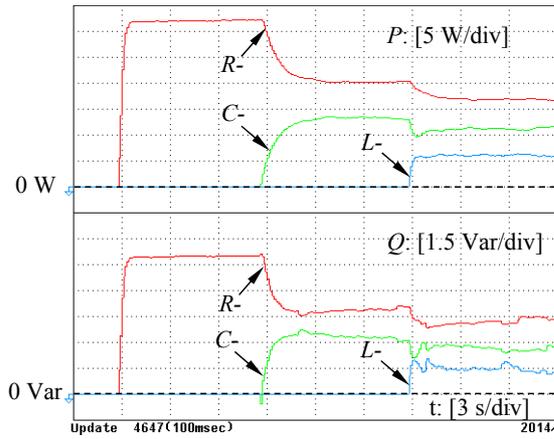
Table 6.3: Steady-state performance of three parallel operated inverters with UDC

Variable	R-&L-&C-inverters
Apparent power 1 (VA)	6.07+1.54j
Apparent power 2 (VA)	11.62+2.83j
Apparent power 3 (VA)	16.60+3.97j
RMS load voltage (V)	11.55
RMS inductor current 1 (A)	0.54
RMS inductor current 2 (A)	1.03
Inductor current 3 (A)	1.48
Frequency f (Hz)	50.016
Current sharing error $\frac{I_3-3I_1}{4I_3} \times 100\%$	-2.4%
Voltage drop $\frac{E^*-V_o}{E^*} \times 100\%$	3.8%
Frequency error $\frac{f^*-f}{f^*} \times 100\%$	0.03%

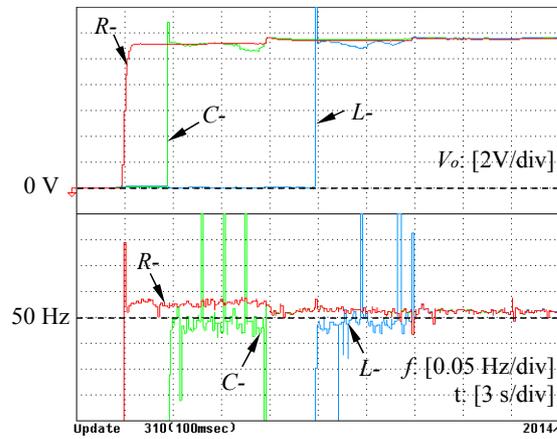
The desired voltage drop ratio $\frac{n_i S_i^*}{K_e E^*}$ is chosen as 10% and the frequency boost ratio $\frac{m_i S_i^*}{\omega^*}$ is chosen as 0.5%. Here the subscript i is the inverter index.

These three inverters are operated as an R-inverter with a virtual 8Ω resistor (Guerrero et al., 2005; Zhong, 2013b), a C-inverter with a virtual $161 \mu\text{F}$ capacitor in series with a virtual 2.5Ω resistor (Zhong and Zeng, 2011; 2014), and an original L-inverter, respectively. The parallel operation of the three inverters is tested, and the L-inverter, the C-inverter and the R-inverter were designed to have a power capacity ratio of 1:2:3, with $P_3 = 1.5P_2 = 3P_1$ and $Q_3 = 1.5Q_2 = 3Q_1$. The corresponding droop coefficients are $n_1 = 1.44$, $n_2 = 0.72$, $n_3 = 0.48$, $m_1 = 0.09$, $m_2 = 0.045$ and $m_3 = 0.03$. The experimental results are shown in Figure 6.20 with the measured steady-state performance shown in Table 6.3.

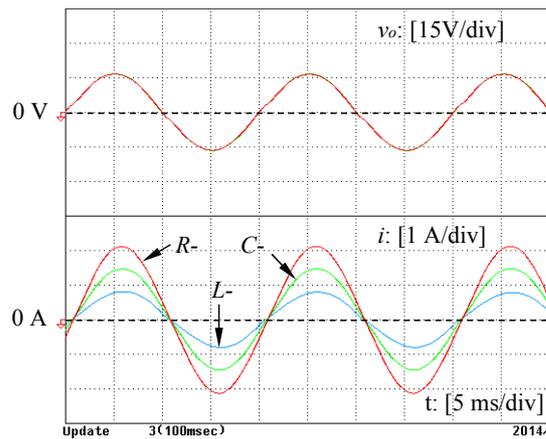
At $t = 3$ s, the R-inverter was started to supply the load. Then, at about $t = 6$ s, the C-inverter was started and began to synchronize with the R-inverter. As shown in Figure 6.20 (b), the RMS load voltage of the C-inverter stepped up to be almost the same as that of the R-inverter and the frequency of the C-inverter stepped up to be approximately 50Hz. At about $t = 12$ s, the C-inverter was connected to the load and thus in parallel with the R-inverter. As shown in Figure 6.20 (a), after a short transient, the R-inverter and the C-inverter shared the real power and the reactive power with a ratio of 3:2, as designed. As shown in Figure 6.20 (b), the RMS value of the load voltage and the frequency of both inverters became the same. The inverter load voltage RMS value slightly increased and the R-inverter frequency decreased a little bit.



(a) Real power and reactive power



(b) Frequency and RMS load voltage



(c) Loadt voltage and inductor current

Figure 6.20: Experimental results for parallel operation of an L-inverter, a C-inverter and an R-inverter.

At $t = 15$ s, the L-inverter was started to synchronize with the terminal voltage estab-

lished by the R-inverter and the C-inverter. As shown in Figure 6.20 (b), the RMS load voltage of the L-inverter stepped up to be almost the same as that of the load and the frequency of the L-inverter stepped up to be approximately 50 Hz. After that, at about $t = 21$ s, the L-inverter was connected to the load and thus in parallel with the R-inverter and the C-inverter. As shown in Figure 6.20 (a), the L-inverter, the C-inverter and the R-inverter shared the real power and the reactive power with a ratio of 1:2:3, as designed. As shown in Figure 6.20 (b), the RMS value of the load voltage and the frequency of these three inverters became the same. The RMS voltage of the load slightly increased and the frequency decreased a little bit. The load voltage was regulated well and the inverter currents were shared accurately with a ratio of 1:2:3 in the steady state, as shown in Figure 6.20 (c). Note that because of this phase resetting, the frequency of the inverters measured by the WT500 power analyser had some spikes but this does not matter.

6.7 Summary

In this chapter, a universal droop control principle has been proposed for inverters with any type of output impedance having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad to achieve parallel operation. Moreover, it has been shown that the robust droop controller recently proposed in the literature for R-inverters actually offers one way to implement this principle. In other words, it is actually a universal droop controller that can be applied to any practical inverters having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad. Small-signal stability analysis has been carried out for an inverter equipped with the universal droop controller when the impedance angle changes from $-\frac{\pi}{2}$ rad to $\frac{\pi}{2}$ rad for different loads. The universal droop controller works well for the parallel operation of inverters with different types of output impedance. It is also able to achieve system stability, accurate proportional power sharing, tight voltage regulation and very tight frequency regulation.

Chapter 7

Droop Controller without Voltage and Frequency Deviations

Although a universal droop controller has been proposed in Chapter 6, which enables the parallel operation of inverters with different types of output impedance, droop controllers still have a trade-off between the power sharing and the regulation of the load voltage and frequency. Then, a question arises: Is it possible to have accurate power sharing without any load voltage or frequency deviation?

To solve this problem, a new droop controller adopting the structure of the robust droop controller (Zhong, 2013b) and utilizing the transient droop characteristics (Guerrero et al., 2005) is proposed. This controller can achieve proportional power sharing while maintaining the load voltage and frequency at the nominal values. This means that the voltage drop caused by the inverter output impedance will be automatically compensated. Besides, this controller needs no communication between parallel connected inverters.

7.1 The Trade-off of the Droop Controller

Inverters can have different types of output impedance, corresponding to which the droop controller has different forms (Brabandere et al., 2007; Yao et al., 2011; Guerrero et al., 2005; 2007). To simplify the analysis, the R-inverter is taken as an example. The proposed droop controller can be easily extended to the case of the L-inverter and the C-inverter.

7.1.1 The Trade-off of the Conventional Droop Controller

The conventional droop controller of the R-inverter is

$$E = E^* - nP \quad (7.1)$$

$$\omega = \omega^* + mQ. \quad (7.2)$$

According to (7.1) and (7.2), the load voltage amplitude and frequency deviations caused by the droop controller are $-nP$ and mQ , respectively. Obviously, the deviations exist as long as the power is not zero. Besides, the voltage drop on the inverter output impedance will make the load voltage amplitude deviate further.

7.1.2 The Trade-off of the Robust Droop Controller

As shown in Figure 2.9, the robust droop controller of the R-inverter is

$$\dot{E} = K_e(E^* - V_o) - nP \quad (7.3)$$

$$\omega = \omega^* + mQ. \quad (7.4)$$

At the steady state, (7.3) becomes

$$nP = K_e(E^* - V_o). \quad (7.5)$$

According to (7.4) and (7.5), the deviations caused by the droop controller are $\frac{-nP}{K_e}$ and mQ , respectively. Although by adjusting K_e , n and m , the deviations can be controlled to be small, they exist as long as the power is not zero.

7.1.3 Limitations of Droop Controllers Reported in Literature

This trade-off can be partly removed with the method proposed in (Guerrero et al., 2005).

As shown in Figure 7.1, there are

$$E = E^* \quad (7.6)$$

$$\omega - \omega^* = m\tilde{Q} \quad (7.7)$$

with

$$\tilde{Q} = H(s)Q = \frac{\tau s}{\tau s + 1}Q \quad (7.8)$$

where τ is the time constant of the transient droop action. Then, according to Figure 2.5(a) and Figure 7.1,

$$v_o = v_r - Z_o(s) \cdot i \quad (7.9)$$

with

$$Z_o(s) = Z_{vir}(s) + sL = R + K_L P + sL \quad (7.10)$$

where $Z_{vir}(s)$ is the adaptive virtual impedance. Note that the output impedance in (Guerero et al., 2005) is defined at the terminal with the load voltage and the load current, while the one in this chapter is defined with the load voltage and the filter inductor current. These two are almost the same at low frequencies (Zhong and Zeng, 2014). According to (7.7), the steady-state frequency deviation would be 0, and the reactive power Q can be shared proportionally.

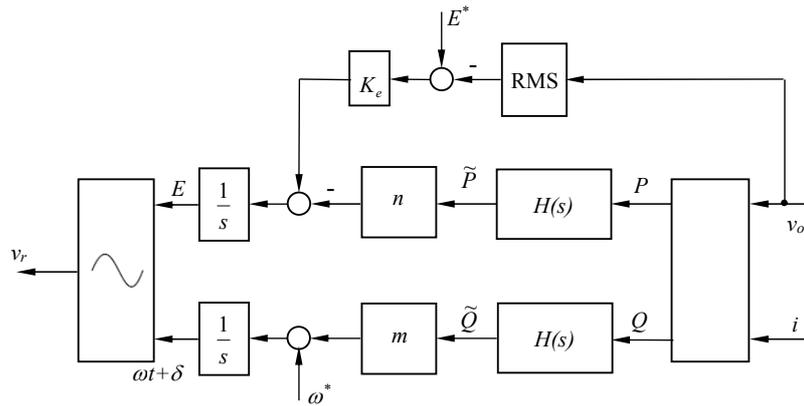
However, the magnitude deviation of the load voltage v_o can not be avoided. According to (7.6), the amplitude of the inverter reference voltage v_r is set to be the nominal value. Then, according to (7.9), the amplitude of the load voltage v_o will deviate from the nominal value because of the voltage drop on the inverter output impedance. Another issue is the active power sharing. For the R-inverter, $R \gg sL$, and roughly

$$P = \frac{E - V_o}{Z_o} V_o \approx \frac{E^* - V_o}{R + K_L P} V_o \quad (7.11)$$

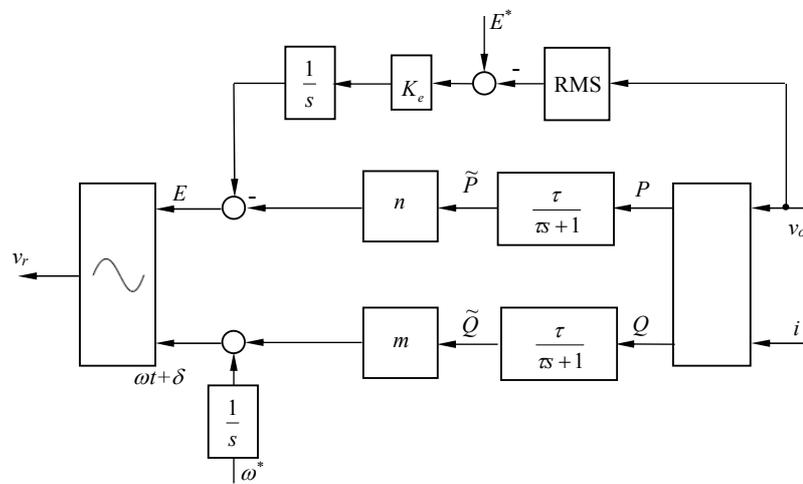
which is equal to

$$K_L P^2 + RP + V_o(V_o - E^*) = 0 \quad (7.12)$$

where $V_o(V_o - E^*)$ would be constant at the steady state. For equal active power sharing, all inverters should have the same K_L and R , which can be easily set by the controller. However, for proportional active power sharing, K_L and R need to be calculated according to the value of $V_o(V_o - E^*)$, which is difficult to be obtained in advance.



(a) The principle of the proposed robust droop controller



(b) The proposed droop controller without zero-pole cancellation

Figure 7.2: The proposed droop controller.

of (7.14) and (7.15) will also be 0. Hence, this yields

$$V_o = E^* \quad (7.18)$$

$$\omega = \omega^* \quad (7.19)$$

which guarantee the steady-state deviations of both the load voltage magnitude and frequency to be 0. It indicates that the voltage drop on the inverter output impedance has been automatically compensated. For the active and the reactive power sharing, there are

$$P = \left(\frac{1}{\tau_s} + 1\right)\tilde{P} \quad (7.20)$$

$$Q = \left(\frac{1}{\tau_s} + 1\right)\tilde{Q}. \quad (7.21)$$

When the initial conditions of both integral of \tilde{P} and \tilde{Q} are the same, it holds that

$$P = \frac{1}{\tau} \int_0^\infty \tilde{P} dt + \tilde{P} \quad (7.22)$$

$$Q = \frac{1}{\tau} \int_0^\infty \tilde{Q} dt + \tilde{Q}. \quad (7.23)$$

According to (7.22) and (7.23), the active power P and reactive power Q will be accurately proportionally shared, as long as the transient active power \tilde{P} and the transient reactive power \tilde{Q} are proportionally shared, which can be achieved by choosing proper n and m . However, the zero-pole cancellation caused by the integrators and $H(s)$ exists, which makes the system internally unstable. As shown in Figure 7.2(b), to avoid the zero-pole cancellation, the integrator positions are changed.

7.3 Simulation Results

To verify the proposed droop controller, simulations were carried out with MATLAB 2013a, toolboxes such as Simulink and Simscape were extensively used. The solver used in the simulations was ode23 with a relative tolerance of 10^{-3} and the sampling time is $1 \mu\text{F}$. More detailed information can be found in Appendix A. The inverter system consisted of two single-phase inverters powered by two separate 400 V dc voltage supplies. The load is a 50Ω resistor. The PWM switching frequency is 15 kHz, the filter inductor is $L = 0.55$

mH with a parasitic resistance of $0.3\ \Omega$, and the filter capacitor C is $20\ \mu\text{F}$. The rated RMS value of the load voltage is $230\ \text{V}$, and the rated system line frequency is $50\ \text{Hz}$. K_e is chosen to be 10 , and τ is chosen to be 1 . The rated capacity of inverter 1 and inverter 2 are $0.5\ \text{kVA}$ and $1\ \text{kVA}$, respectively. It is expected that $P_2 = 2P_1$ and $Q_2 = 2Q_1$. With the proposed controller, the load voltage magnitude and frequency deviations at the steady state will be maintained at 0 . Thus, the desired voltage drop ratio $\frac{nS^*}{K_e E^*}$ and the frequency boost ratio $\frac{mS^*}{\omega^*}$ do not influence the corresponding steady-state deviations any more, but influence the speeds of the corresponding transient responses. The frequency boost ratio is set to be 0.1% , and the desired voltage drop ratio is chosen to be 10% to guarantee the response speed. As a result, $n_1 = 0.46$ and $n_2 = 0.23$; $m_1 = 6.2832 \times 10^{-4}$ and $m_2 = 3.1416 \times 10^{-4}$.

Simulation 1 was carried out with the droop controller proposed in this chapter, while simulation 2 is with the robust droop controller (Zhong, 2013b), which can be easily implemented by setting $H(s) = 1$. Simulation 3 was carried out with the droop controller proposed in (Guerrero et al., 2005). For Simulation 1 and 2, the virtual resistive output impedance is designed via a current loop $u = v_r - Ri$ (Guerrero et al., 2005). For all the simulations, the virtual resistance for inverter 1 and 2 is set to be $R_1 = 12\ \Omega$ and $R_2 = 6\ \Omega$, respectively. For simulation 3, K_L is set to be 0.01 .

As can be seen from Figure 7.3 and Table 7.1, the robust droop controller was able to accurately proportionally share both the active power and the reactive power. However, there existed load voltage amplitude and frequency deviations and were $-14\ \text{V}$ and $-0.02\ \text{Hz}$, respectively. Thus, the voltage drop is approximately 6.1% of the rated voltage and the frequency error is approximately 0.04% of the rated frequency. The droop controller proposed in (Guerrero et al., 2005) was able to maintain the frequency at the nominal value. However, the power sharing, and particularly the active power sharing, was not good. Besides, the load voltage amplitude deviation was approximately $-27\ \text{V}$. Thus, the voltage drop is approximately 11.7% of the rated voltage, which is larger than the desired voltage drop. These simulation results agreed with the analysis in Section 7.1 and Section 7.2. The droop controller proposed in this chapter was able to achieve proportional sharing for both the active and the reactive powers. Meanwhile, it was able to keep both the load voltage amplitude and the frequency at the exact nominal values.

Table 7.1: Steady-state performance of two parallel operated inverters.

Variable	simulation 1	simulation 2	simulation 3
Apparent power 1 (VA)	340-220j	300-200j	340-200j
Apparent power 2 (VA)	680-440j	600-400j	500-340j
RMS load voltage (V)	230	216	203
Frequency f (Hz)	50	49.98	50
Voltage drop $\frac{E^* - V_2}{E^*} \times 100\%$	0	6.1%	11.7%
Frequency error $\frac{f^* - f}{f^*} \times 100\%$	0	0.04%	0

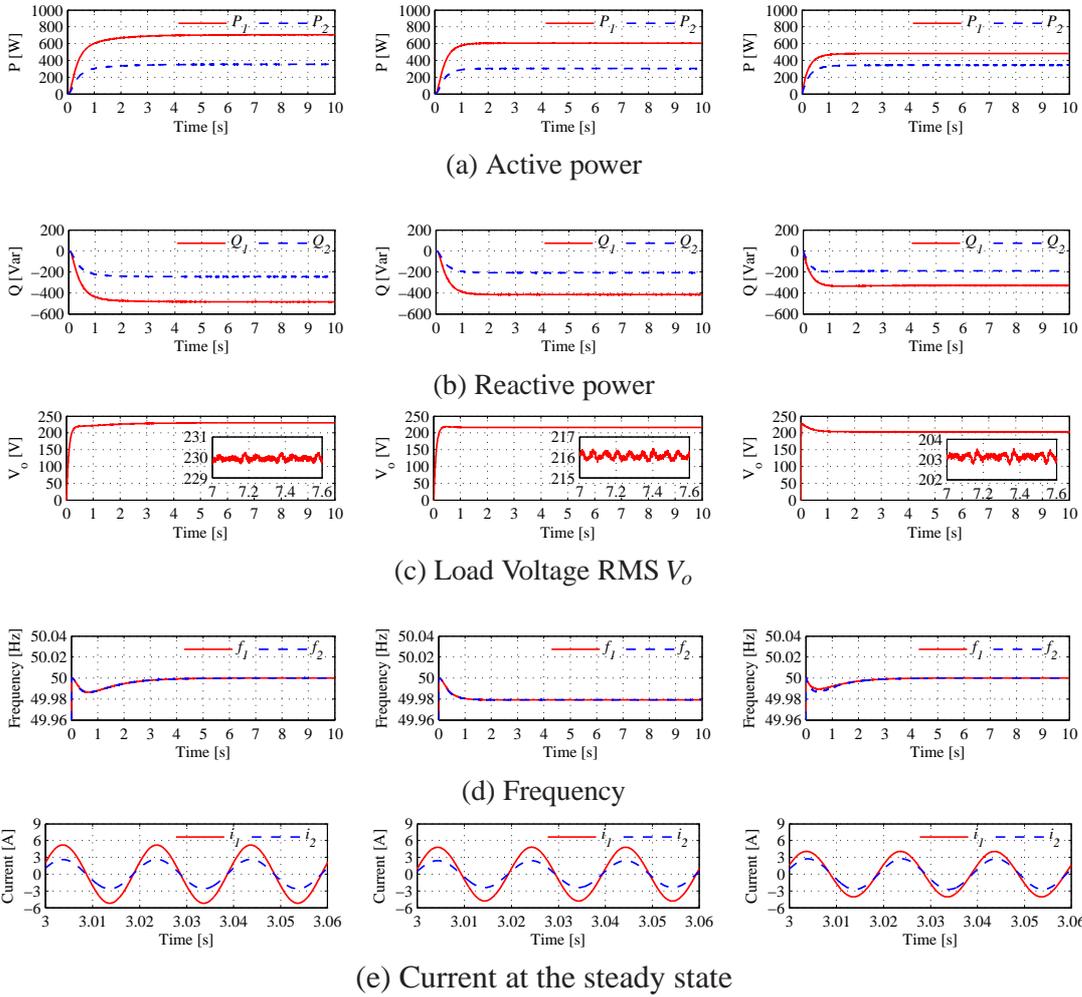


Figure 7.3: Simulation results with the linear load $R = 50\Omega$: simulation 1 with the proposed droop controller (left column), simulation 2 with the robust droop controller (middle column), and simulation 3 with the droop controller proposed in (Guerrero et al., 2005) (right column).

As the magnitude of the load voltage in simulation 1 was maintained at the nominal

value, while both the load voltage magnitude of simulation 2 and 3 dropped, the power generated in simulation 1 was the largest. Meanwhile, the voltage drop in simulation 3 caused by the virtual impedance $R + K_L P + sL$ was larger than the one of simulation 2 caused by the robust droop controller ($\frac{K_e E^* P}{10S}$) and the output impedance $R + sL$. The active power and the reactive power of simulation 3 were smaller than the one of simulation 2.

7.4 Summary

In this chapter, the trade-off of the conventional droop control scheme has been pointed out. Conventional droop controllers have voltage and frequency deviations when the load power is not zero. A droop control method has been proposed in (Guerrero et al., 2005) to address this problem. However, as this method can not compensate the voltage drop caused by the inverter output impedance, it can not avoid the voltage amplitude deviation. Besides, it does not work well when the active power sharing ratio is not 1:1. To solve these problems, a new droop control strategy is proposed in this chapter. It adopts the structure of the robust droop controller and utilizes the transient droop characteristics. It is able to achieve proportional power sharing while maintaining the inverter output amplitude and frequency at the nominal values. However, limitations on the initial conditions of the integrators and the per-unit output impedance are very strict and need to be further studied.

Chapter 8

Current Droop Controller

Droop controllers studied in the previous chapters are all about the control of the power. However, even if the power is controlled, currents are still not limited when a sudden load change or short-circuit occurs. A possible solution is directly controlling the active and the reactive currents (Brabandere et al., 2007; Liu et al., 2012; Khodadoost Arani et al., 2013). In this chapter, a current droop controller is proposed. It first develops a new current calculation unit to obtain the active and the reactive currents only according to the angle of the load voltage. This unit is simpler than the ones reported and does not need any information of the inverter output impedance. Then, these currents take the places of the power as the control variable to limit the current RMS value at the steady state. Next, the structure of the robust droop controller is adopted to guarantee the robustness, based on which the CDC is developed. With an adaptive coefficient added to the voltage magnitude loop, this controller is able to better limit the current than the proposed ones. After that, the small signal stability is analysed. Finally, experimental results are provided to verify the feasibility of the proposed current droop controller.

8.1 Limitations of Droop Controllers Reported in Literature

The droop controller has different forms for inverters with different types of output impedance. In this chapter, the inverter with resistive output impedance is taken as an example. The conventional droop controller (2.16)-(2.17) (Diaz et al., 2010) and robust droop con-

troller (2.18)-(2.19) (Zhong, 2013b) are not able to limit the currents well when the load voltage v_o deviates far away from its nominal value. The conventional current droop controller takes the form

$$E = E^* - nI_p \quad (8.1)$$

$$\omega = \omega^* + mI_q \quad (8.2)$$

where I_p and I_q are the RMS values of the active and the reactive currents, respectively. It has better performance but the response speed has not been improved enough (Brabandere et al., 2007; Liu et al., 2012; Khodadoost Arani et al., 2013).

In both (Brabandere et al., 2007) and (Liu et al., 2012), active and reactive currents are calculated with

$$\begin{bmatrix} I_p \\ I_q \end{bmatrix} = \frac{1}{V_o} \begin{bmatrix} \frac{X}{Z} & -\frac{R}{Z} \\ \frac{R}{Z} & \frac{X}{Z} \end{bmatrix} \begin{bmatrix} P \\ Q \end{bmatrix} \quad (8.3)$$

where R is the resistance of the inverter output impedance and X is the reactance of the inverter output impedance. Thus, the power, the magnitude of the load voltage, and the ratios $\frac{X}{Z}$ and $\frac{R}{Z}$ are needed.

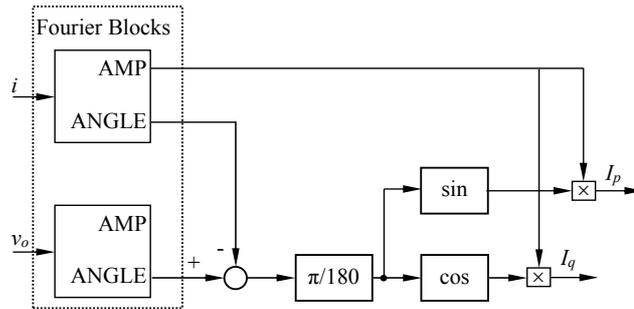


Figure 8.1: The current calculation unit reported in (Khodadoost Arani et al., 2013).

As shown in Figure 8.1, for the current calculation unit proposed in (Khodadoost Arani et al., 2013), two Fourier blocks are firstly adopted to obtain the angle of the inverter load voltage v_o , the angle and amplitude of the current i . Then, the current amplitude and the

angle difference are used in the calculation of the active and the reactive currents:

$$I_p = I \cos(\theta_v - \theta_i) \quad (8.4)$$

$$I_q = I \sin(\theta_v - \theta_i) \quad (8.5)$$

where I is the RMS value of the current i . As the controller proposed in (Khodadoost Arani et al., 2013) adopts the control structure of the conventional droop controller, it has some strict limitations, such as the same per-unit output impedance for all the parallel operated inverters.

8.2 The Proposed Current Droop Controller

In this chapter, a new droop control method named current droop controller is proposed. It is based on a new current calculation unit and adopts the structure of the robust droop controller, which makes it robust to numerical errors, disturbances, component mismatches and parameter drifts. Besides, it adds an adaptive coefficient to voltage magnitude and frequency loops, so that the short-circuit current could be limited.

8.2.1 The Current Calculation Unit

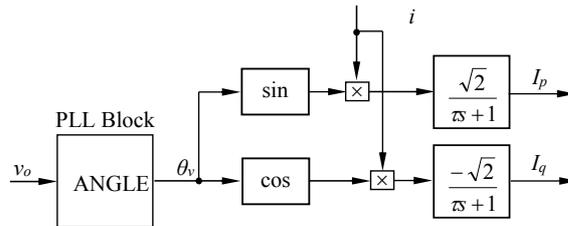


Figure 8.2: The proposed current calculation unit.

As shown in Figure 8.2, following applies

$$I_p = \frac{\sqrt{2}}{\tau s + 1} i \sin \theta_v \approx I \cos(\theta_v - \theta_i) \quad (8.6)$$

$$I_q = \frac{-\sqrt{2}}{\tau s + 1} i \cos \theta_v \approx I \sin(\theta_v - \theta_i). \quad (8.7)$$

where i is the inductor current, θ_i is the angle of the inductor current, and θ_v is the angle of

the inverter load voltage. Note that this unit only adopts one Fourier block and only needs the angle of the inverter load voltage v_o .

8.2.2 The Current Droop Controller

Based on this current calculation unit, a current droop controller with robust form is proposed, which adopts the structure of the robust droop controller:

$$\dot{E} = K_e(E^* - V_o) - nI_p \quad (8.8)$$

$$\omega = \omega^* + mI_q \quad (8.9)$$

However, its current limiting ability is very weak. As shown in Figure 8.3, an adaptive coefficient is added to the voltage magnitude loop:

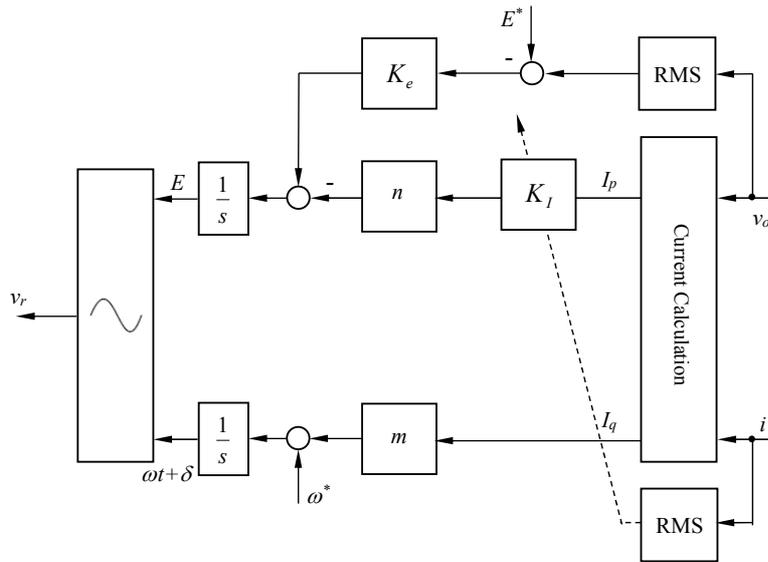


Figure 8.3: The proposed current droop controller.

$$\dot{E} = K_e(E^* - V_o) - nK_I I_p \quad (8.10)$$

$$\omega = \omega^* + mI_q \quad (8.11)$$

where

$$K_I = \left(\frac{I}{I_r}\right)^h \quad (8.12)$$

and

$$h = 1, 2, 3, \dots$$

Here, n and m are set according to the voltage drop ratio R_v and frequency boost ratio R_f , with current $I = I_{max}$:

$$n = \frac{K_e E^* R_v}{I_{max}} \quad (8.13)$$

$$m = \frac{\omega^* R_f}{I_{max}}. \quad (8.14)$$

8.2.3 Current Limiting

For conventional current droop controller, one has

$$n = \frac{E^* R_v}{I_{max}} \quad (8.15)$$

$$m = \frac{\omega^* R_f}{I_{max}}. \quad (8.16)$$

According to (8.1), (8.2), (8.15) and (8.16), at the steady state, there should be

$$I_p = \frac{E^* - E}{n} = \frac{E^* - E}{R_v E^*} I_{max} \quad (8.17)$$

$$I_q = \frac{\omega - \omega^*}{m} = \frac{\omega - \omega^*}{\omega^* R_f} I_{max}. \quad (8.18)$$

Assuming that $S^* = I_{max} E^*$, for robust droop controller, there are

$$n = \frac{K_e R_v}{I_{max}} \quad (8.19)$$

$$m = \frac{\omega^* R_f}{I_{max} E^*} \quad (8.20)$$

According to (8.8), (8.9), (8.19) and (8.20), at the steady state, there should be

$$I_p = \frac{K_e (E^* - V_o)}{n V_o} = \frac{E^* - V_o}{R_v V_o} I_{max} \quad (8.21)$$

$$I_q = \frac{\omega - \omega^*}{m V_o} = \frac{(\omega - \omega^*) E^*}{\omega^* R_f V_o} I_{max}. \quad (8.22)$$

For the CDC proposed in this chapter, according to (8.10), (8.11), (8.13) and (8.14), at the steady state, there should be

$$I_p = \frac{K_e(E^* - V_o)}{nK_I} = \frac{K_e I_{max}(E^* - V_o)}{K_e R_v E^* K_I} = \frac{E^* - V_o}{R_v E^* K_I} I_{max} \quad (8.23)$$

$$I_q = \frac{\omega - \omega^*}{m} = \frac{\omega - \omega^*}{\omega^* R_f} I_{max}. \quad (8.24)$$

Ignoring the voltage drop on the inverter output impedance, then $V_o \approx E$. When the inverter is working at the rated current $I = I_r$, there will be $K_I = 1$ and $V_o \approx E^*$. Then

$$I_p = \frac{E^* - V_o}{R_v E^*} I_{max} \approx \frac{E^* - E}{R_v E^*} I_{max} \approx \frac{E^* - V_o}{R_v V_o} I_{max}. \quad (8.25)$$

This indicates that when the inverter is working at the rated current, the active current of the proposed CDC is almost the same with the ones of the conventional current droop controller and the robust droop controller. When the inverter is working above the rated current $I > I_r$, there will be $K_I > 1$ and $V_o < E^*$. Then

$$I_p < \frac{E^* - V_o}{R_v E^*} I_{max} \approx \frac{E^* - E}{R_v E^*} I_{max} < \frac{E^* - V_o}{R_v V_o} I_{max}. \quad (8.26)$$

Thus, I_p with the proposed CDC is better limited than the ones with the conventional current droop controller and the robust droop controller. The bigger the current I , the stronger the limitation on I_p . Similarly, K_I can be used in the I_q droop to limit the reactive current.

8.2.4 Power Sharing

In this chapter, h is chosen to be 2 as an example:

$$h = 2. \quad (8.27)$$

According to (8.6) and (8.7), there is

$$I^2 = I_p^2 + I_q^2. \quad (8.28)$$

According to (8.10), there is

$$K_e(E^* - V_o) = n\left(\frac{I}{I_r}\right)^2 I_p. \quad (8.29)$$

By solving (8.11), (8.28) and (8.29), one gets

$$I_q = \frac{\omega - \omega^*}{m} \quad (8.30)$$

$$I_p = \frac{3\left(\sqrt{\frac{I_r^4 K_e^2 (E^* - V_o)^2}{4n^2} + \frac{(\omega - \omega^*)^6}{27m^6} + \frac{I_r^2 K_e (E^* - V_o)}{2n}}\right)^{2/3} - \left(\frac{\omega - \omega^*}{m}\right)^2}{3\left(\sqrt{\frac{I_r^4 K_e^2 (E^* - V_o)^2}{4n^2} + \frac{(\omega - \omega^*)^6}{27m^6} + \frac{I_r^2 K_e (E^* - V_o)}{2n}}\right)^{1/3}}. \quad (8.31)$$

When two inverters are operated in parallel,

$$\frac{m_1}{m_2} = \frac{n_1}{n_2} = \frac{I_2^*}{I_1^*} = N. \quad (8.32)$$

According to (8.30) and (8.31), there will be

$$\frac{I_{p1}}{I_{p2}} = \frac{I_{q1}}{I_{q2}} = \frac{1}{N} \quad (8.33)$$

which guarantees the current sharing of the parallel operated inverters. Especially, when the short-circuit happens, there will be $V_o = 0$ and

$$I_p = \frac{3\left(\sqrt{\frac{I_r^4 K_e^2 E^{*2}}{4n^2} + \frac{(\omega - \omega^*)^6}{27m^6} + \frac{I_r^2 K_e E^*}{2n}}\right)^{2/3} - \left(\frac{\omega - \omega^*}{m}\right)^2}{3\left(\sqrt{\frac{I_r^4 K_e^2 E^{*2}}{4n^2} + \frac{(\omega - \omega^*)^6}{27m^6} + \frac{I_r^2 K_e E^*}{2n}}\right)^{1/3}} \quad (8.34)$$

$$I_q = \frac{\omega - \omega^*}{m}. \quad (8.35)$$

Obviously, the current sharing is also guaranteed when the short-circuit happens.

8.3 Stability for the Current Droop Controller

It is very complicated to analyse the system stability with the current droop controller with the adaptive coefficient (8.10-8.11). Thus the case with current droop controller without the adaptive coefficient (8.8-8.9) is analysed here.

8.3.1 Small-Signal Stability

Consider small disturbances Δ around the stable equilibrium operation point (δ_e, E_e) , where δ_e, E_e represent the phase angle difference between the inverter source voltage and load voltage, and the magnitude of the inverter source voltage, respectively. Consider the low pass filter, the linearised forms of (8.8-8.9) for a small disturbance around the stable equilibrium point become

$$\Delta E(s)s = \frac{-n\omega_f}{s + \omega_f} \Delta I_{Pi}(s) \quad (8.36)$$

$$\Delta \omega(s) = \frac{m\omega_f}{s + \omega_f} \Delta I_{Qi}(s). \quad (8.37)$$

Then

$$I_p = \left(\frac{E}{Z_o} \cos \delta - \frac{V_o}{Z_o} \right) \cos \theta + \frac{E}{Z_o} \sin \delta \sin \theta \quad (8.38)$$

$$I_q = \left(\frac{E}{Z_o} \cos \delta - \frac{V_o}{Z_o} \right) \sin \theta - \frac{E}{Z_o} \sin \delta \cos \theta. \quad (8.39)$$

It is assumed that V_o is constant, thus this term could be ignored

$$I_p = \frac{E(\cos \delta \cos \theta + \sin \delta \sin \theta)}{Z_o} \quad (8.40)$$

$$I_q = \frac{E(\cos \delta \sin \theta - \sin \delta \cos \theta)}{Z_o} \quad (8.41)$$

and hence

$$\begin{aligned} \Delta I_p(s) = & \frac{\cos \delta_e \cos \theta + \sin \delta_e \sin \theta}{Z_o} \Delta E(s) \\ & + \frac{E_e(-\sin \delta_e \cos \theta + \cos \delta_e \sin \theta)}{Z_o} \Delta \delta(s) \end{aligned} \quad (8.42)$$

$$\begin{aligned} \Delta I_q(s) = & \frac{\cos \delta_e \sin \theta - \sin \delta_e \cos \theta}{Z_o} \Delta E(s) \\ & - \frac{E_e(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o} \Delta \delta(s). \end{aligned} \quad (8.43)$$

Thus

$$\Delta E(s)s = \frac{-n\omega_f}{s + \omega_f} \left[\frac{\cos \delta_e \cos \theta + \sin \delta_e \sin \theta}{Z_o} \Delta E(s) + \frac{E_e(-\sin \delta_e \cos \theta + \cos \delta_e \sin \theta)}{Z_o} \Delta \delta(s) \right] \quad (8.44)$$

$$\Delta \omega(s) = \frac{m\omega_f}{s + \omega_f} \left[\frac{\cos \delta_e \sin \theta - \sin \delta_e \cos \theta}{Z_o} \Delta E(s) - \frac{E_e(\sin \delta_e \sin \theta + \cos \delta_e \cos \theta)}{Z_o} \Delta \delta(s) \right]. \quad (8.45)$$

Additionally, it holds true that

$$\Delta \omega(s) = s\Delta \delta(s). \quad (8.46)$$

According to (8.44), (8.45) and (8.46), the homogeneous equation will be

$$as^4\Delta \delta(s) + bs^3\Delta \delta(s) + cs^2\Delta \delta(s) + ds\Delta \delta(s) + e\Delta \delta(s) = 0 \quad (8.47)$$

where

$$a = Z_o^2 \quad (8.48)$$

$$b = 2Z_o^2\omega_f \quad (8.49)$$

$$c = Z_o\omega_f((\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)(n + mE_e) + Z_o\omega_f) \quad (8.50)$$

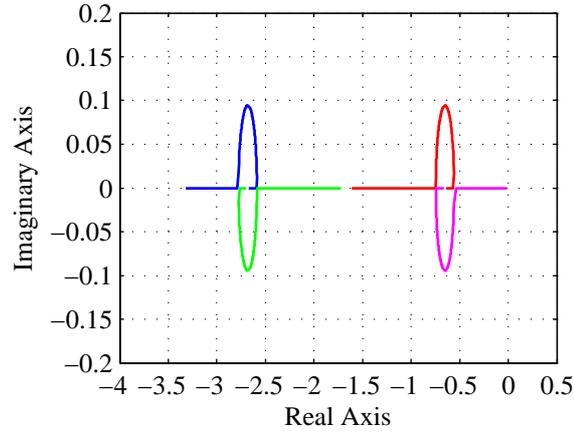
$$d = Z_o\omega_f^2(\cos \delta_e \cos \theta + \sin \delta_e \sin \theta)(n + mE_e) \quad (8.51)$$

$$e = mE_en\omega_f^2. \quad (8.52)$$

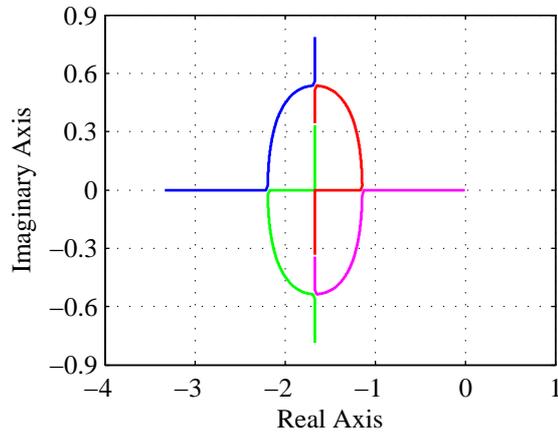
The system response can be analysed by the characteristic equation

$$as^4 + bs^3 + cs^2 + ds + e = 0. \quad (8.53)$$

To make the analysis simpler, the load is assumed to be purely resistive, which indicates that the reactive power would be 0 and the frequency would be maintained at ω^* . As can be seen from Figure 8.4, for one inverter equipped with current droop controller (8.8-8.9), the system is always stable when K_e and n are positive.



(a) K_e increases from 0.01 to 30



(b) n increases from 0.01 to 10

Figure 8.4: The root-locus for the current droop control scheme.

8.3.2 The Stability of the Load Voltage Dynamics

When the load is complex $R + jX$, where the output impedance is $R_o + jX_o$, there are

$$\vec{E} = V_o + \frac{(R_o + jX_o)V_o}{R + jX} = \frac{R + jX + R_o + jX_o}{R + jX} V_o. \quad (8.54)$$

Thus

$$E = \frac{\sqrt{(R^2 + RR_o + X^2 + XX_o)^2 + (RX_o - XR_o)^2}}{R^2 + X^2} V_o \quad (8.55)$$

thereby

$$V_o = \frac{R^2 + X^2}{\sqrt{(R^2 + RR_o + X^2 + XX_o)^2 + (RX_o - XR_o)^2}} E \quad (8.56)$$

and

$$I = \frac{V_o}{R + jX} = \frac{R - jX}{R^2 + X^2} V_o \quad (8.57)$$

$$I_p = \frac{R}{R^2 + X^2} V_o. \quad (8.58)$$

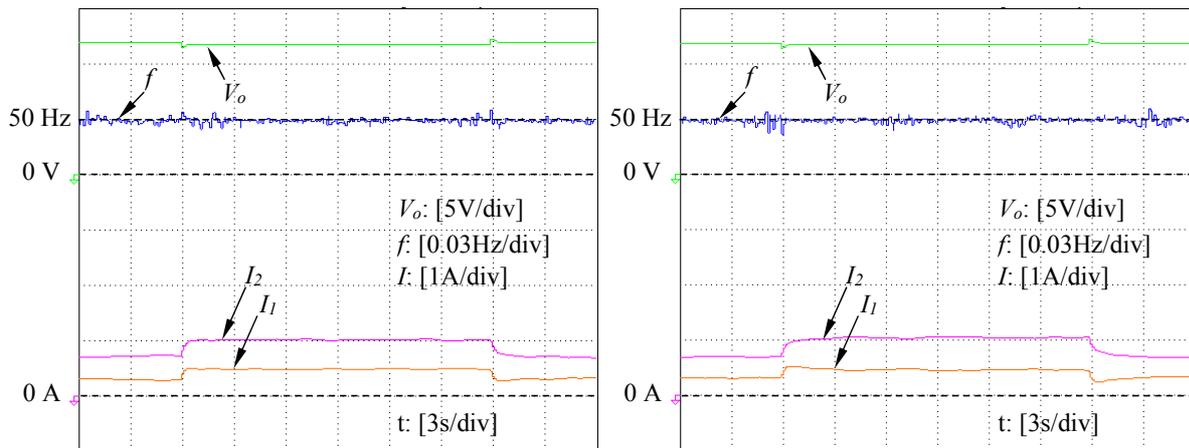
Thus

$$\dot{E} = K_e E^* - \frac{(K_e + \frac{nR}{R^2 + X^2})(R^2 + X^2)}{\sqrt{(R^2 + RR_o + X^2 + XX_o)^2 + (RX_o - XR_o)^2}} E. \quad (8.59)$$

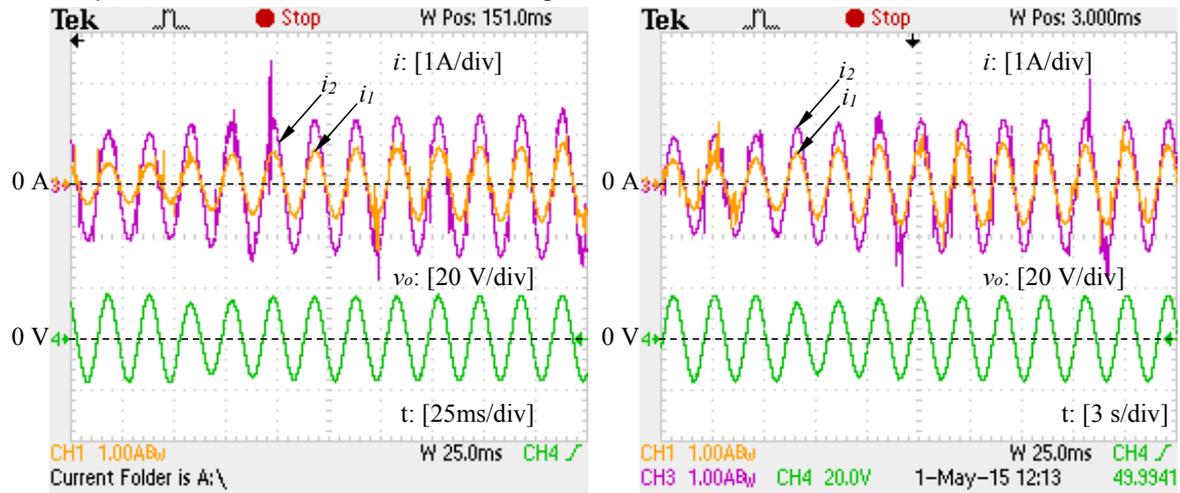
Thereby, when K_e is positive bounded and n is positive, the system would be stable. Besides, when K_e is fixed and n is increased, the system would be more stable.

8.4 Experimental Results

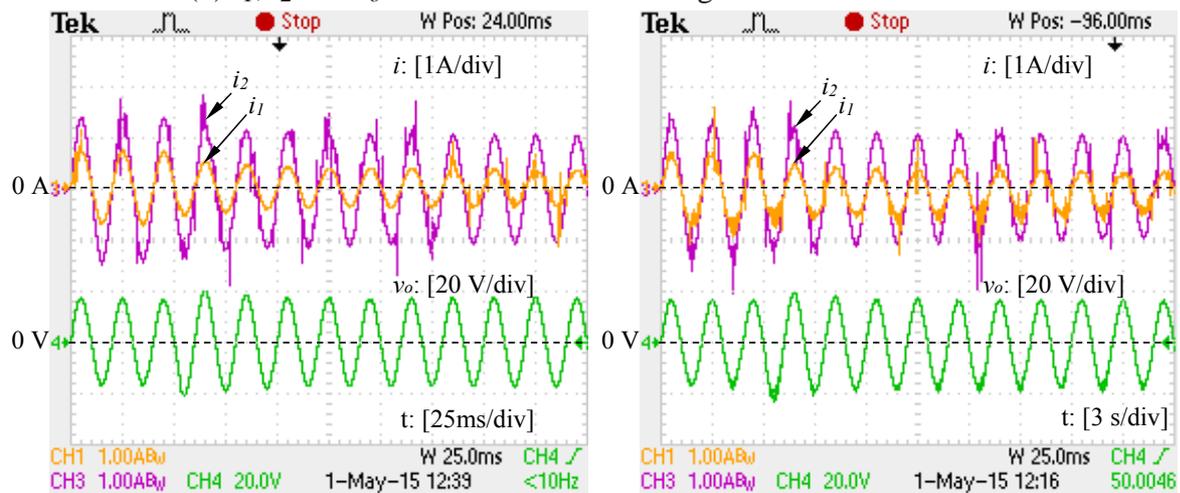
To validate the proposed current droop controller, experiments were carried out on the test rig consisting of three single-phase inverters, as shown in Figure B.1(a). More detailed information can be found in Appendix B. In this chapter, only two of the three inverters of the experimental setup were used. The dc voltage supplies are 30 V. The filter inductor is $L = 7$ mH with a parasitic resistance of 1Ω and the filter capacitor C is $1 \mu\text{F}$. The PWM switching frequency is 10 kHz, the line frequency of the system is 50 Hz. The rated load voltage of inverters is 12 V and $K_e = 20$. The desired voltage drop ratio R_v is chosen to be 10% and the frequency boost ratio R_f to be 0.5%. Since the aim of this chapter is to address current droop controller for the parallel operation of inverters, the case with a nonlinear load is not considered. Besides, these two inverters are operated as an R-inverter with a virtual 4Ω resistor. For the proposed current droop controller, the two inverters were designed to have $I_{max1} = 2.5$ A, and $I_{max2} = 5$ A, with the droop coefficients of $n_1 = 0.62$, $n_2 = 9.6$, $m_1 = 0.31$ and $m_2 = 4.8$. Besides, the rated currents are set as $I_{r1} = 0.5$ A, and $I_{r2} = 1$ A. It was expected that $I_2 = 2I_1$ in parallel operation, and that i_2 is in phase with i_1 . For the robust droop controller, the corresponding power capacities were $S_1 = 30$ VA, and $S_2 = 60$ VA, with $n_1 = 0.052$, $n_2 = 0.8$, $m_1 = 0.026$ and $m_2 = 0.4$.



(a) f , V_o , I_1 and I_2 when the load changed from $12\ \Omega$ to $8\ \Omega$ and then back to $12\ \Omega$



(b) i_1 , i_2 and v_o when the load was changed from $12\ \Omega$ to $8\ \Omega$



(c) i_1 , i_2 and v_o when the load was changed from $8\ \Omega$ to $12\ \Omega$

Figure 8.5: Experimental results with the load changed from $12\ \Omega$ to $8\ \Omega$ and then back to $12\ \Omega$: with the current droop controller (left column), and with the robust droop controller (right column).

8.4.1 Case I: Load Changed from 12 Ω to 8 Ω and Then Back to 12 Ω

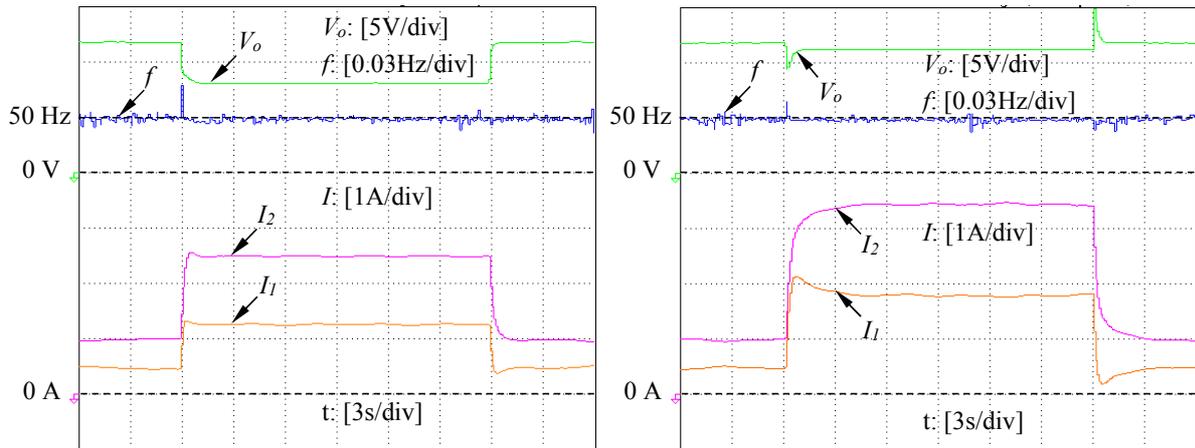
As shown in Figure 8.5 and Table 8.1, the load was changed from 12 Ω to 8 Ω at time $t = 6$ s and then back to 12 Ω at time $t = 24$ s. As shown in Figure 8.5(a), for both current droop controller and robust droop controller, current I_1 was changed from 0.33 A to 0.5 A and I_2 was changed from 0.67 A to 1 A at time $t = 6$ s. Then, current I_2 was changed back to 0.33 A and I_2 to 0.67 A at time $t = 24$ s. The voltage magnitude had a small drop at time $t = 6$ s and a small jump at time $t = 24$ s. While the voltage magnitude with the 8 Ω load is slightly lower than the one with 12 Ω load that is approximately 12 V, the frequency remains almost the same at approximately 50 Hz before and after the load change. The instantaneous currents and voltage were shown in 8.5(b) and (c). The current dynamic response of current droop controller (approximately 0.6 s) was faster than the one of the robust droop controller (approximately 3 s). For both controllers, i_2 is in phase with i_1 at the steady state.

8.4.2 Case II: Load Changed from 8 Ω to 2 Ω and Then Back to 8 Ω

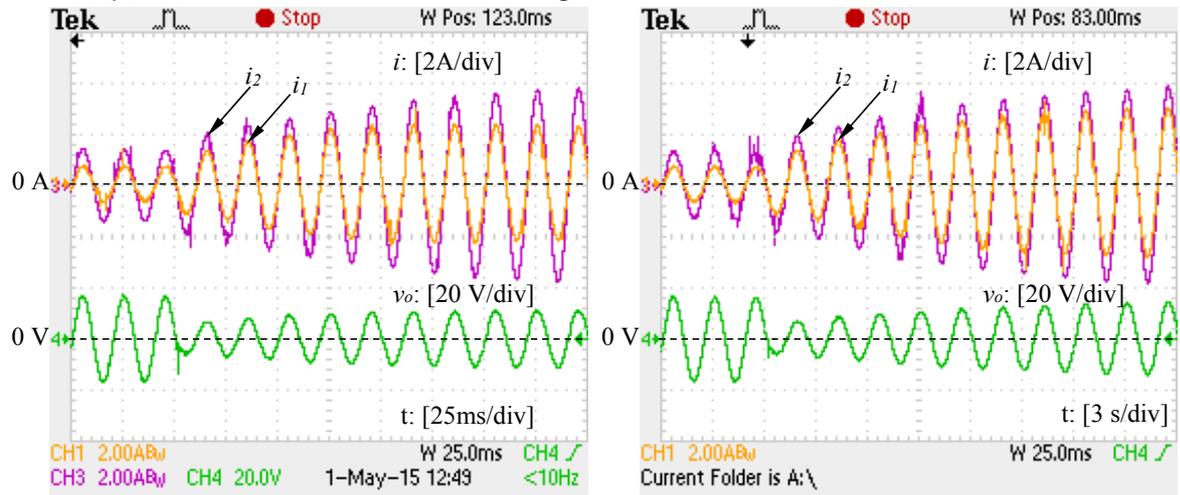
As shown in Figure 8.6 and Table 8.1, the load was changed from 8 Ω to 2 Ω at time $t = 6$ s and then back to 8 Ω at time $t = 24$ s. As shown in Figure 8.6(a), for current droop controller, current I_1 was changed from 0.5 A to 1.3 A and I_2 was changed from 1 A to 2.6 A at time $t = 6$ s. Then, I_1 returned to be 0.5 A and I_2 returned to be 1 A at time $t = 24$ s. For robust droop controller, current I_1 was changed from 0.5 A to 1.8 A and I_2 was changed from 1 A to 3.6 A at time $t = 6$ s. Then, I_1 returned to be 0.5 A and I_2 returned to be 1 A at time $t = 24$ s. Thus, in the case with 2 Ω load, in which case the inductor current is larger than the rated current, the current droop controller is able to limit the current approximately 28% lower than the robust droop controller.

Table 8.1: Steady-state performance of two parallel operated inverters with CDC.

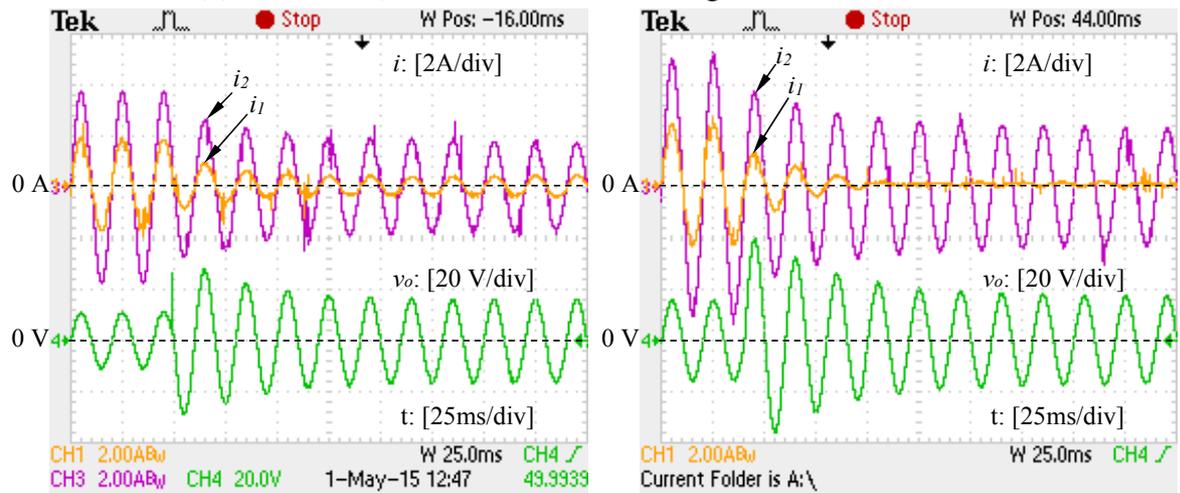
Variable	With CDC			With UDC		
	12 Ω	8 Ω	2 Ω	12 Ω	8 Ω	2 Ω
RMS load voltage (V)	11.9	11.6	8	11.8	11.6	11
RMS inductor current 1 (A)	0.33	0.5	1.3	0.33	0.5	1.8
RMS inductor current 2 (A)	0.67	1	2.6	0.67	1	3.6
Response time for load change (s)	-	0.6	1	-	3	6



(a) f , V_o , I_1 and I_2 when the load changed from 8Ω to 2Ω and then back to 8Ω



(b) i_1 , i_2 and v_o when the load was changed from 8Ω to 2Ω



(c) i_1 , i_2 and v_o when the load was changed from 2Ω to 8Ω

Figure 8.6: Experimental results with the load changed from 8Ω to 2Ω and then back to 8Ω : with the current droop controller (left column), and with the robust droop controller (right column).

When the load was 2Ω , the load voltage magnitude when equipped with the current droop controller was approximately 8 V, while the one when equipped with the robust droop controller was approximately 11 V. In this case, the current droop controller is able to reduce the load voltage magnitude by approximately 27% from the one when equipped with the robust droop controller. Besides, the load voltage magnitude when equipped with the robust droop controller had a deep drop (approximately 2.5 V) at time $t = 6$ s and a big jump (approximately 4V) at time $t = 24$ s, while the voltage magnitude when equipped with the current droop controller changed very smoothly. The frequency remained almost the same at approximately 50 Hz before and after the load change.

The instantaneous currents and voltage are shown in 8.6(b) and (c). As can be seen, the current dynamic response when equipped with the current droop controller (approximately 1 s) was much faster than the one when equipped with the robust droop controller (approximately 6 s). Besides, for both the two controllers, i_2 was in phase with i_1 at the steady state.

8.5 Summary

For the parallel operation of inverters, a new droop control method named current droop controller is proposed in this chapter. A new current calculation unit is first proposed to obtain the active and the reactive currents. It only needs the angle of the load voltage, which is obtained by a PLL block. These currents are then used as the control variables of the droop controller to limit the current RMS value at the steady state. To make the controller robust to numerical errors, disturbances, component mismatches and parameter drifts, the structure of the robust droop controller is adopted. To better limit the currents, an adaptive coefficient is added to the voltage magnitude loop. Experimental results in different cases have demonstrated the effectiveness of the proposed current droop controller. It is able to achieve faster response during the the load change and is able to better limit the current RMS value at the steady state. Meanwhile, accurate load sharing, good voltage and frequency regulation are maintained.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

In this thesis, the inverter output impedance has been designed to improve the power quality and the droop controller for the parallel operation of inverters has been investigated. Small signal analysis has been adopted to analyse the stability of the inverter system equipped with the proposed controllers.

9.1.1 Design of the Inverter Output Impedance

Mainstream inverters have inductive output impedance (L-inverter) because of the filter inductor and could also have resistive output impedance (R-inverter) in some low-voltage applications. In order to improve the load voltage THD, the C-inverter has been proposed. Its output impedance is capacitive over a wide range of both low and high frequencies although it still has the inductor connected to the inverter bridge. The C-inverter is achieved via an inductor current feedback through an integrator, of which the time constant is the desired output capacitance. As the capacitor is a virtual one, there is no limit on the current rating and can be applied to any power level. The capacitance can be selected to guarantee the stability of the current loop. Besides, the value of the output capacitance can be optimised so that the THD of the load voltage is minimised. When compared to an inverter having resistive or inductive output impedance, the C-inverter is able to achieve lower voltage THD. Moreover, some guidelines are developed to facilitate the selection of the filter components for C-inverters.

After that, the output impedance of the C-inverter has been further developed to be a virtual resonant impedance. Its principle generates from a resonant impedance topology consisting of inductors and capacitors, of which the magnitude approaches 0 at different frequencies. The improved C-inverter is achieved via a feedback of the inductor current through an transfer function, which is the expression of a resonant impedance topology consisting of inductors and capacitors. The virtual resonant impedance could be designed to have different levels. It is exactly the same with a virtual capacitor when it only has one level. When it is designed to have N levels, where N is larger than one, the coefficients of the transfer function or the virtual resonant impedance are selected and optimised to minimise the load voltage harmonics at N different orders, and thus the corresponding total harmonic distortion (THD) of the load voltage could be minimised. Simulation and experimental results are provided to demonstrate the feasibility and excellent performance of C-inverters and Improved C-inverters. The filter parameters of the test rig are selected according to the guidelines developed. It is shown that, with the same hardware, C-inverters are able to achieve lower voltage THD than L-inverters and R-inverters, and Improved C-inverters are able to achieve even lower voltage THD than C-inverters.

9.1.2 The Development of the Droop Controller

After the C-inverter is proposed, in order to facilitate the parallel operation of C-inverters, the robust droop controller has been further developed. Usually, the $Q \sim E$ and $P \sim \omega$ droops are used when the output impedance is inductive; the $Q \sim \omega$ and $P \sim E$ droops are used when the output impedance is resistive; for a complex impedance, a transformation involving the impedance phase angle needs to be introduced (Guerrero et al., 2006b; Yao et al., 2011). For the C-inverter, the $Q \sim -E$ and $P \sim -\omega$ droops are adopted. For the improved C-inverter, as the virtual resonant impedance is also capacitive at the fundamental frequency, the $Q \sim -E$ and $P \sim -\omega$ droops could also be used.

In order to enable the parallel operation of inverters with different types of output impedance, a universal transformation matrix T has been identified to transform the actual active power and reactive power into the virtual ones. With the matrix T , a universal droop control principle that works for inverters with any type of output impedance having a phase angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad is developed. Coincidentally and interestingly, this prin-

principle takes the form of the droop control principle for R-inverters and paves the way for designing universal droop controllers with different methods. In this project, the robust droop control mechanism proposed in (Zhong, 2013b) is added to this droop control principle to provide one way to implement it, which turns out to be the same as the robust droop controller proposed in (Zhong, 2013b). Note that the proposed universal droop controller enables the parallel operation of inverters with any type of output impedance having a phase angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad, for the first time, which covers any practical L-, R-, C-, R_L - and R_C -inverters. This finding is mathematically proven and validated experimentally with a test rig consisting of three inverters operated in parallel.

Then, in order to achieve accurate power sharing without any load voltage amplitude or frequency deviation, a droop controller that adopts the structure of the robust droop controller and utilizes the transient droop characteristics has been presented. It is able to achieve proportional power sharing while maintaining the inverter output amplitude and frequency at the nominal values. Besides, in order to limit the current RMS value at the steady state when a sudden load change or short-circuit occurs, a current droop controller (CDC) is proposed. It is based on a current calculation unit, which has been proposed to obtain the active and the reactive currents only according to the angle of the load voltage. These currents are used in place of the power as the control variables. It also adopts the structure of the robust droop controller to guarantee the robustness. An adaptive coefficient is added to voltage magnitude loop to better limit the inverter currents. This controller is able to better limit the current and response faster than the robust droop controller, and the conventional current droop controller.

9.2 Future Work

Based on the study carried out in this thesis, much more work could be done in the future. The inverter output impedance can be further developed to improve the power quality, the limitations of proposed droop controllers should be addressed, and the application of the controllers can be extended to three-phase inverters and grid-connected inverters.

9.2.1 Further Development of the Inverter Output Impedance

As has been mentioned in Chapter 3, the output impedance of an inverter can be defined at different terminals that have different pairs of voltage and current and hence can be different. According to (3.49), the overall output impedance is more or less the same as the output impedance without considering the filter capacitor at low frequencies, where the major voltage harmonics are concerned. Thus, the filter capacitor has little influence on the optimal virtual capacitor C_o . However, the influence of the filter capacitor on the whole inverter system should be further investigated. Take C-inverter for example, according to Figure 2.5(a) and Figure 3.1, there are

$$u = v_r - \frac{1}{sC_o}(i_o + i_c) \quad (9.1)$$

and

$$u_f = (R + sL)(i_o + i_c) + v_o. \quad (9.2)$$

Since the average of u_f over a switching period is the same as u , there is (approximately)

$$v_r - \frac{1}{sC_o}\left(i_o + \frac{v_o}{R_o + \frac{1}{sC}}\right) = (R + sL)\left(i_o + \frac{v_o}{R_o + \frac{1}{sC}}\right) + v_o \quad (9.3)$$

which gives

$$v_o = K_{vr}v_r - Z(s)i_o \quad (9.4)$$

where $Z(s)$ is the overall output impedance described by (3.51), and

$$K_{vr} = \frac{R_o + \frac{1}{sC}}{R + sL + \frac{1}{sC_o} + R_o + \frac{1}{sC}}. \quad (9.5)$$

At low frequencies, K_r could be simplified to

$$K_{vr} \approx \frac{1}{\frac{C}{C_o} + 1}. \quad (9.6)$$

At the fundamental frequencies, according to (3.55), there is

$$C \ll C_o, \quad (9.7)$$

so

$$K_{vr} \approx 1. \quad (9.8)$$

This fact indicates that C and R_o have little impact on the output voltage at the fundamental frequency. For frequencies higher than the fundamental frequency, take the 3rd harmonic for example, Figure 9.1 shows the Bode plots of K_{vr} .

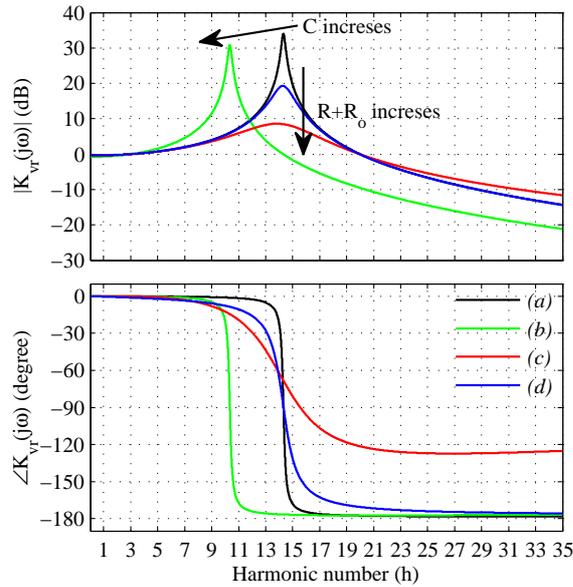


Figure 9.1: The Bode plot of K_{vr} with $L = 2.35$ mH and $C_o = 479$ μ F, under four different conditions: (a) $C = 22$ μ F, $R = 0.1$ Ω and $R_o = 0.1$ Ω ; (b) $C = 44$ μ F, $R = 0.1$ Ω and $R_o = 0.1$ Ω ; (c) $C = 22$ μ F, $R = 4$ Ω and $R_o = 0.1$ Ω ; (d) $C = 22$ μ F, $R = 0.1$ Ω and $R_o = 1$ Ω .

As can be seen, when C increases, the peak of the magnitude curve shifts left-bottom, and the phase curve shifts left. It indicates that the filter capacitor has an effect on voltage harmonics if the reference voltage v_r contains some harmonic components. When R and R_o increases, the peak of the magnitude curve falls a lot and its phase curve becomes smoother. To avoid energy loss caused by the real resistor, the virtual resistor can be introduced to the virtual resonant impedance. On the one hand, the virtual resistor would raise the magnitude of the voltage harmonic components at a wide range of frequencies. On the other hand, it could decrease the magnitude of the voltage harmonic components at the resonant frequencies of the virtual resonant impedance. Besides, the virtual resistor offers the system stronger damping and stability. Then, how to wisely design the parameters to achieve

lower voltage THD while maintaining good damping needs to be studied.

Furthermore, the concept of the smart impedance can be introduced. In fact, the resonant impedance has been widely investigated (Mallett, 1924; Iinuma, 1931; Moheimani and Behrens, 2004), and its principle has been introduced together with the proportional-resonant controller (Herman et al., 2014) to achieve active impedance (Da Silva et al., 2009), hybrid active impedance (Gonzatti et al., 2013) and smart impedance (Gonzatti et al., 2015). The smart impedance can be regarded as a new way to look at hybrid active power filters (Gonzatti et al., 2015), where the proportional-resonant controller is often used to generate resonant peaks to extracting the selected harmonics for generating harmonic command reference (Teodorescu et al., 2006). To handle the harmonic problems with smart impedance, an extra active converter, a coupling transformer, a capacitive unit and corresponding controllers are needed.

9.2.2 Improvement of Proposed Droop Controllers

For the droop controller proposed in Chapter 7, the limitations on the initial conditions of the integrators and the per-unit output impedance are very strict. How to remove this limitation is a critical problem. For the current droop controller proposed in Chapter 8, at least one period delay exists in the transient response because of the current RMS block. This delay could cause the system failure in some extreme cases, and needs to be addressed. Moreover, proposed droop controllers all focus on the control of single-phase voltage-controlled VSI with local load. The application of the controllers can be extended to the case of three-phase inverters and grid-connected inverters.

For three-phase inverters, the voltages and currents can be described in different reference frames, including the natural (abc) frame, the stationary reference ($\alpha\beta$) frame, and the synchronously rotating reference (dq) frame. Thus, the controller should be designed in different coordinates. For the droop controller, the synchronously rotating reference (dq) frame is often adopted, as the voltages and currents under this frame are no longer dependent on time, and the real and reactive power components of the voltage and the current can be obtained, respectively. This facilitates the droop controller design and analysis. For the grid-connected inverters, the droop controller has different forms with the the droop controller for stand-alone inverters. Take the L-inverter for example, the conventional droop

controller for the L-inverter in grid-connected mode is

$$E = E^* + n(Q_{set} - Q) \quad (9.9)$$

$$\omega = \omega^* + m(P_{set} - P). \quad (9.10)$$

Besides, the filter for the grid-connected connected inverters are often LCL filters, as shown in Figure 2.4(b), which needs to be carefully designed.

9.2.3 Small Signal Stability

The small signal stability analysis in this thesis focuses on one inverter equipped with the proposed droop controller. However, the parallel operated inverter system equipped with the droop controller is much more complicated, and need to be further studied. The method presented in (Coelho et al., 2002) could be adopted. The key principle is to consider a common $d - q$ reference frame for all inverters, and represent the vector \vec{E} as

$$\vec{E} = e_d + je_q \quad (9.11)$$

where

$$e_d = E \cos(\delta) \quad (9.12)$$

$$e_q = E \sin(\delta) \quad (9.13)$$

$$\delta = \arctan\left(\frac{e_q}{e_d}\right). \quad (9.14)$$

Linearising the equation for δ , which is the angular position of the vector \vec{E} ,

$$\Delta\delta = m_d \Delta e_d + m_q \Delta e_q \quad (9.15)$$

where

$$m_d = -\frac{e_q}{e_d^2 + e_q^2} \quad (9.16)$$

$$m_q = \frac{e_d}{e_d^2 + e_q^2}. \quad (9.17)$$

According to (4.23) and (9.15), one has

$$\Delta\omega = m_d\Delta\dot{e}_d + m_q\Delta\dot{e}_q. \quad (9.18)$$

Then, considering that

$$E = |\vec{E}| = \sqrt{e_d^2 + e_q^2} \quad (9.19)$$

after linearisation, there is

$$\Delta E = n_d\Delta e_d + n_q\Delta e_q \quad (9.20)$$

where

$$n_d = \frac{e_d}{\sqrt{e_d^2 + e_q^2}} \quad (9.21)$$

$$n_q = \frac{e_q}{\sqrt{e_d^2 + e_q^2}}. \quad (9.22)$$

It follows that

$$\Delta\dot{E} = n_d\Delta\dot{e}_d + n_q\Delta\dot{e}_q. \quad (9.23)$$

Take two parallel operated L-inverters for example, considering (2.25), (2.26), (9.18), (9.20) and (9.23), we can obtain the following state equation, which describes each inverter

$$\begin{bmatrix} \Delta\dot{\omega}_i \\ \Delta\dot{e}_{di} \\ \Delta\dot{e}_{qi} \end{bmatrix} = [M_i] \begin{bmatrix} \Delta\omega_i \\ \Delta e_{di} \\ \Delta e_{qi} \end{bmatrix} + [C_i] \begin{bmatrix} \Delta P_i \\ \Delta Q_i \end{bmatrix} \quad (9.24)$$

where

$$[M_i] = \begin{bmatrix} -\omega_f & 0 & 0 \\ \frac{n_{qi}}{m_{di}n_{qi} - m_{qi}n_{di}} & \frac{m_{qi}n_{di}\omega_f}{m_{di}n_{qi} - m_{qi}n_{di}} & \frac{m_{qi}n_{qi}\omega_f}{m_{di}n_{qi} - m_{qi}n_{di}} \\ \frac{n_{di}}{m_{qi}n_{di} - m_{di}n_{qi}} & \frac{m_{di}n_{di}\omega_f}{m_{qi}n_{di} - m_{di}n_{qi}} & \frac{m_{di}n_{qi}\omega_f}{m_{qi}n_{di} - m_{di}n_{qi}} \end{bmatrix} \quad (9.25)$$

$$[C_i] = \begin{bmatrix} 0 & m_i\omega_f \\ \frac{n_i m_q \omega_f}{m_{di}n_{qi} - m_{qi}n_{di}} & 0 \\ \frac{n_i m_d \omega_f}{m_{qi}n_{di} - m_{di}n_{qi}} & 0 \end{bmatrix}. \quad (9.26)$$

Considering the relationship between the current and the voltage

$$[\Delta i] = [Y_s][\Delta e]. \quad (9.27)$$

and the active power and the reactive power supplied by each inverter

$$P_i = e_{di}i_{di} + e_{qi}i_{qi} \quad (9.28)$$

$$Q_i = e_{di}i_{qi} - e_{qi}i_{di}. \quad (9.29)$$

There are

$$[\Delta \dot{X}] = [A][\Delta X] \quad (9.30)$$

where

$$[A] = [M_s] + [C_s]([I_s] + [E_s][Y_s])[K_s] \quad (9.31)$$

$$[M_s] = \begin{bmatrix} M_1 & \\ & M_2 \end{bmatrix} \quad (9.32)$$

$$[C_s] = \begin{bmatrix} C_1 & \\ & C_2 \end{bmatrix} \quad (9.33)$$

$$[I_s] = \begin{bmatrix} i_{d1} & i_{q1} & 0 & 0 \\ i_{q1} & -i_{d1} & 0 & 0 \\ 0 & 0 & i_{d2} & i_{q2} \\ 0 & 0 & i_{q2} & -i_{d2} \end{bmatrix} \quad (9.34)$$

$$[E_s] = \begin{bmatrix} e_{d1} & e_{q1} & 0 & 0 \\ -e_{q1} & e_{d1} & 0 & 0 \\ 0 & 0 & e_{d2} & e_{q2} \\ 0 & 0 & -e_{q2} & e_{d2} \end{bmatrix} \quad (9.35)$$

$$[Y_s] = \begin{bmatrix} G_{11} & -B_{11} & G_{12} & -B_{12} \\ B_{11} & G_{11} & B_{12} & G_{12} \\ G_{21} & -B_{21} & G_{22} & -B_{22} \\ B_{21} & G_{21} & B_{22} & G_{22} \end{bmatrix} \quad (9.36)$$

$$[K_s] = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}. \quad (9.37)$$

This equation describes the behaviour of $\Delta\omega_1$, Δe_{d1} , Δe_{q1} , $\Delta\omega_2$, Δe_{d2} and Δe_{q2} around an operating point defined by ω_1 , e_{d1} , e_{q1} , ω_2 , e_{d2} and e_{q2} from a given small initial condition. However, the small signal stability analysis only works well for linearised case. As the parallel operated inverter system with the droop controller is strongly nonlinear, some nonlinear stability analysis methods need to be studied and applied.

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Appendix A

Simulation and Experimental Software

Simulations were carried out with MATLAB 2013a, toolboxes such as Simulink and Simscape were extensively used. The solver used in the simulations was ode23/Tustin with a relative tolerance of 10^{-3} and the sampling time is $1\mu\text{F}$. The control algorithms for the experiments were programmed and downloaded from MATLAB to the microcontroller TMS320F28335 of Texas Instruments (TI) with Code Composer Studio (CCS) and Blackhawk USB2000.

A.1 Electric Circuit Representation

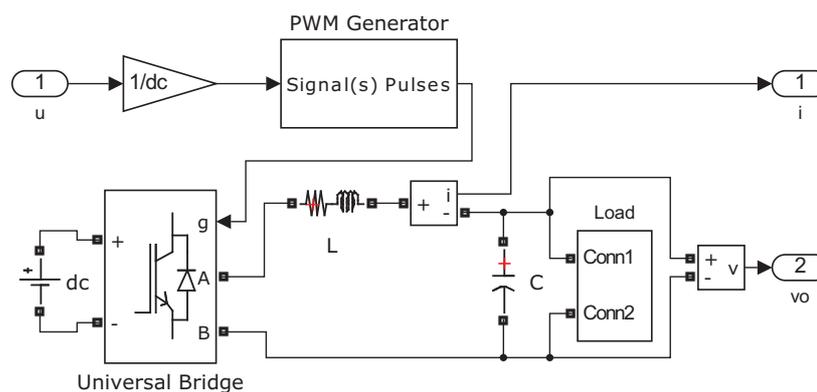


Figure A.1: The circuit of the inverter for the simulation.

As shown in Figure A.1, the inverter can be modelled by the Simscape/SimPowerSystems/Power Electronics/Universal Bridge block. As the inverter is single phase, the number of

bridge arms is chosen to be 2. As IGBT are used in the experiment, the power electronic device of the bridge in the simulation is chosen to be IGBT/Diodes. Other parameters such as the snubber resistance and capacitance, as well as forward voltages are kept as the default values. It is controlled by the signal generated from the Simscape/SimPowerSystems/Control and Measurements Library/Pulse & Signal Generators/PWM Generator block according to the control signal u . The inverter is powered by a dc voltage source and the output voltage is sent to the load through an LC filter. The dc voltage source can be found in the path Simscape/Foundation Library/Electrical/Electrical Sources. The filter inductor and capacitor can be found in the path Simscape/SimPowerSystems/Elements. The inductor current i and load voltage v_o are measured by the current and voltage measurement block, respectively. These blocks can be found in the path Simscape/SimPowerSystems/Measurements.

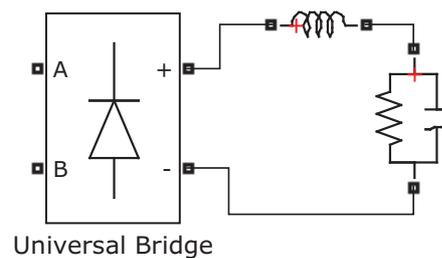


Figure A.2: The nonlinear load for the simulation.

As shown in Figure A.2, the nonlinear load for the simulation is a full-bridge rectifier loaded with an LC filter and a resistor. The full-bridge rectifier can be modelled by the Simscape/SimPowerSystems/Power Electronics/Universal Bridge block, and the number of bridge arms is chosen to be 2. As diodes are used in the experiment, the power electronic device of the bridge in the simulation is chosen to be Diodes. The inductor, capacitor and resistor can be found in the path Simscape/SimPowerSystems/Elements.

A.2 Control Block Diagrams

The controllers proposed in this paper can be achieved in MATLAB with the following control block diagrams, where $K_v = \sqrt{2}$, E_0 and W_0 denote the rated voltage RMS value and system frequency.

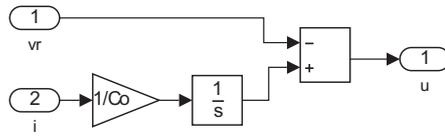


Figure A.3: The virtual capacitor proposed in Chapter 3

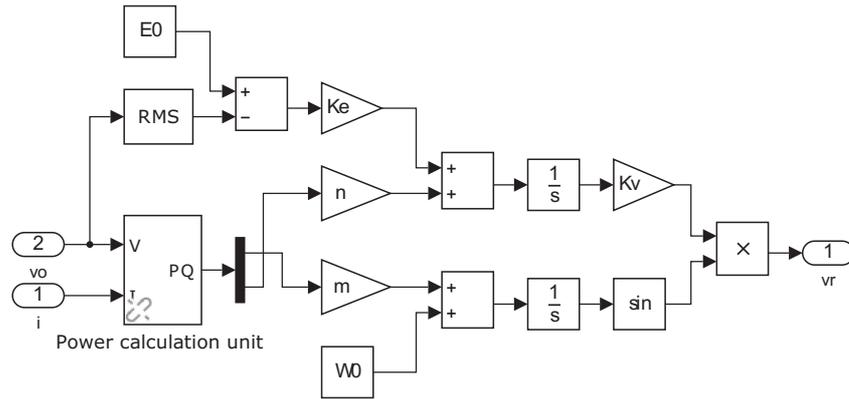


Figure A.4: The robust droop controller for the C-inverter proposed in Chapter 4.

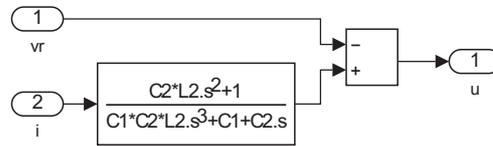


Figure A.5: The virtual resonant impedance proposed in Chapter 5

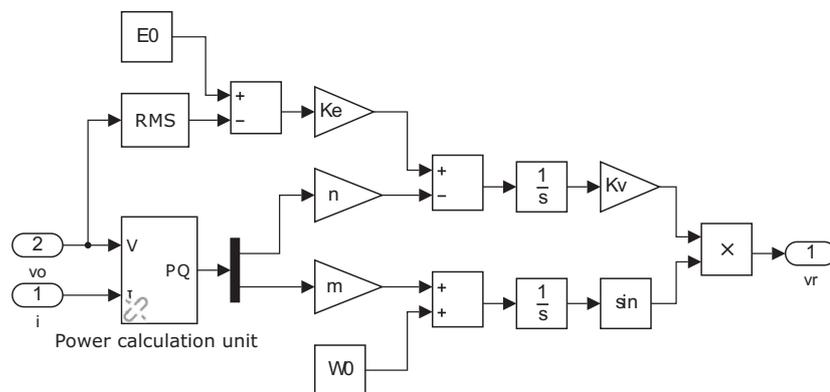


Figure A.6: The universal droop controller proposed in Chapter 6.

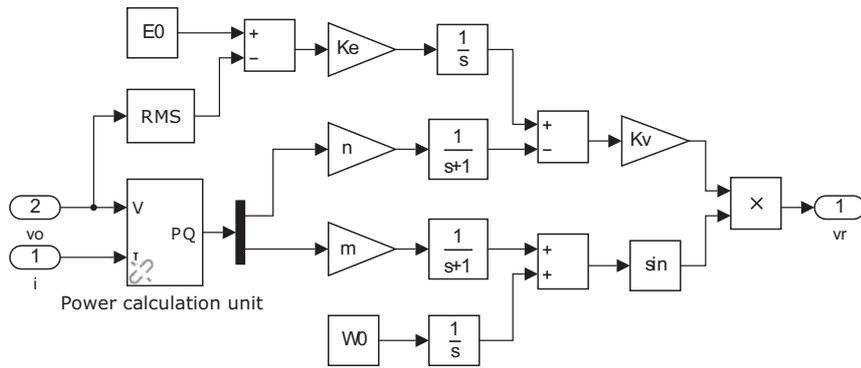


Figure A.7: The droop controller proposed in Chapter 7.

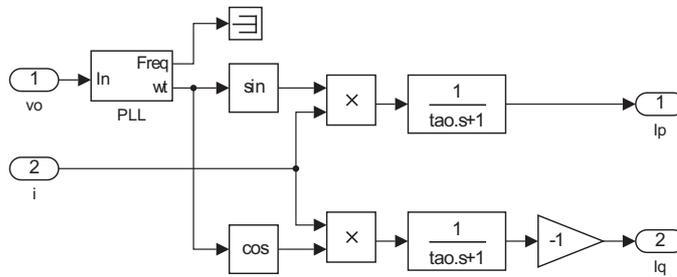


Figure A.8: The current calculation unit proposed in Chapter 8.

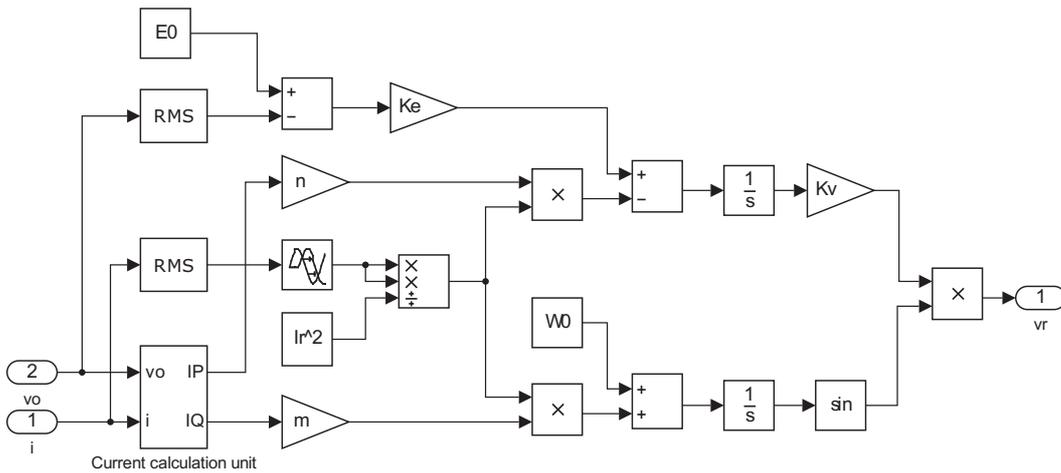


Figure A.9: The current droop controller proposed in Chapter 8.

A.3 CCS Configuration

As shown in Figure A.10, CCS should be configured as follows:

- 1) Under the Family drop down menu, select C28xx.
- 2) Under the Platform drop down menu, select Blackhawk USB2000 controller.
- 3) Select Blackhawk USB2000-F28335 controller.
- 4) Click Add, click Save & Quit and then click Yes to launch CCS on exit.

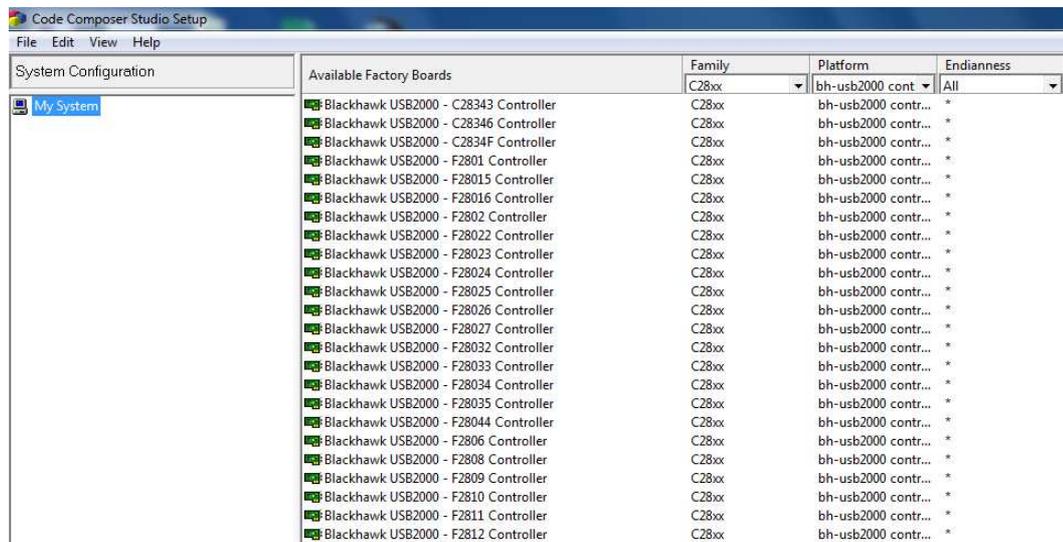
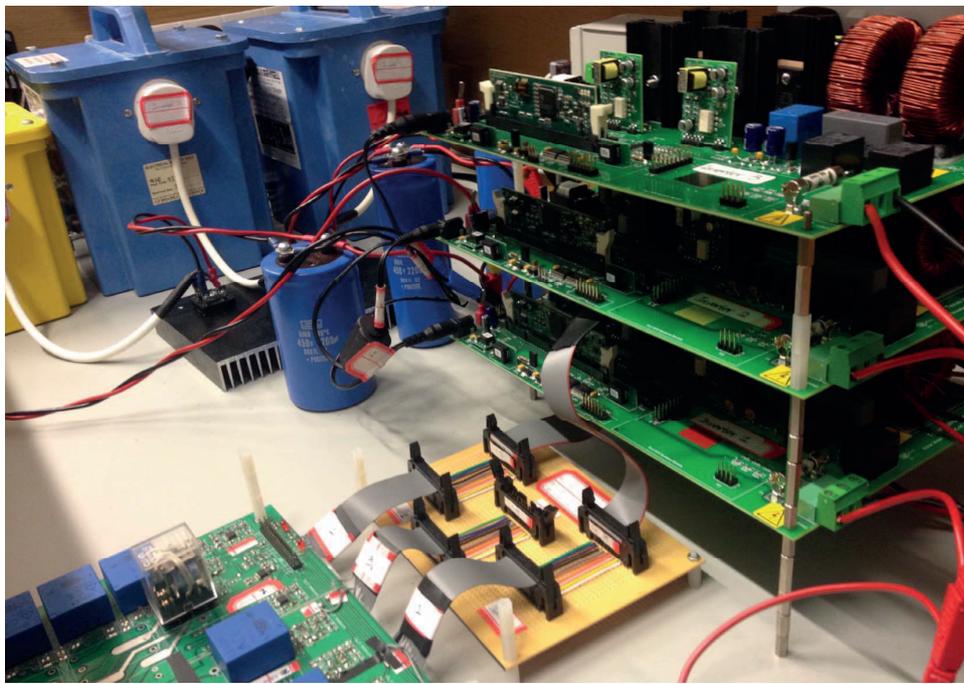


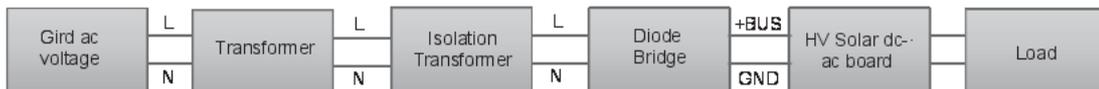
Figure A.10: J.3 CCS Configuration.

Appendix B

Experimental Setup



(a) The picture of the experimental set up



(b) The topology of the main circuit

Figure B.1: The experimental set up consisting of three inverters.

Experiments were carried out on a test rig consisting of three single-phase inverters powered by three separate dc voltage supplies, as shown in Figure B.1(a). According to Figure

B.1(b), the grid ac voltage was first transformed and isolated with the transformer and isolation transformer, respectively. Then, the ac voltage was converted to the dc voltage with the non-regulated diode bridge to power the inverter. A microcontroller TMS320F28335 from TI was adopted to control the TI HV solar dc/ac board, and the inverter output voltage was sent to the load. Note that the TI HV solar dc/ac board has its own LC filter, thus no extra LC filter is needed.

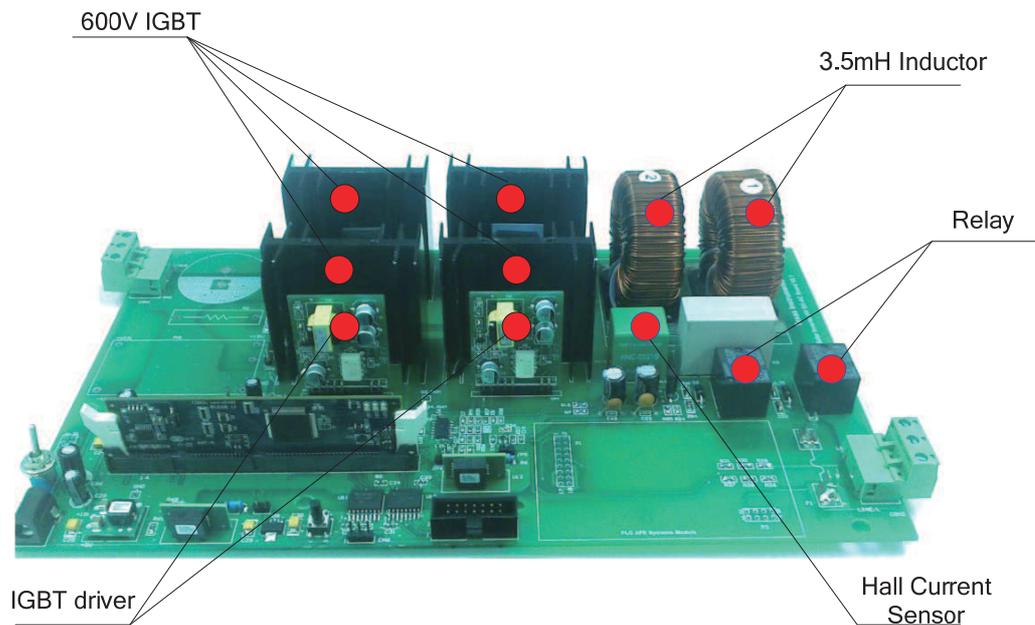


Figure B.2: The board picture of the TI dc/ac board (TI, 2015b).

Three TI high voltage solar inverter dc/ac boards were adopted, of which the board picture is shown in Figure B.2. As can be seen from Figure B.2 and Figure B.5, a $470\ \mu\text{F}/450\ \text{V}$ capacitor was used in the dc side to handle the ripple of the dc voltage generated by the non-regulated diode bridge. 4 IGBT (IRG4PC30FD) driven by 4 IGBT driver boards were used, which were optimised for medium operating frequencies. The maximum collector-to-emitter voltage of the IGBT (IRG4PC30FD) is 600 V, and the maximum continuous collector current is 17 A when the temperature of the collector is $100\ ^\circ\text{C}$. The onboard LC filter consisted of two 3.5 mH inductors and one $1\ \mu\text{F}$ capacitor. One hall current sensor was installed between the filter inductor and filter capacitor to measure the inductor current. Two relays were installed after the filter capacitor, and one 10 A/220 V ac fuse was installed after the relay.

B.0.1 PCB Layout

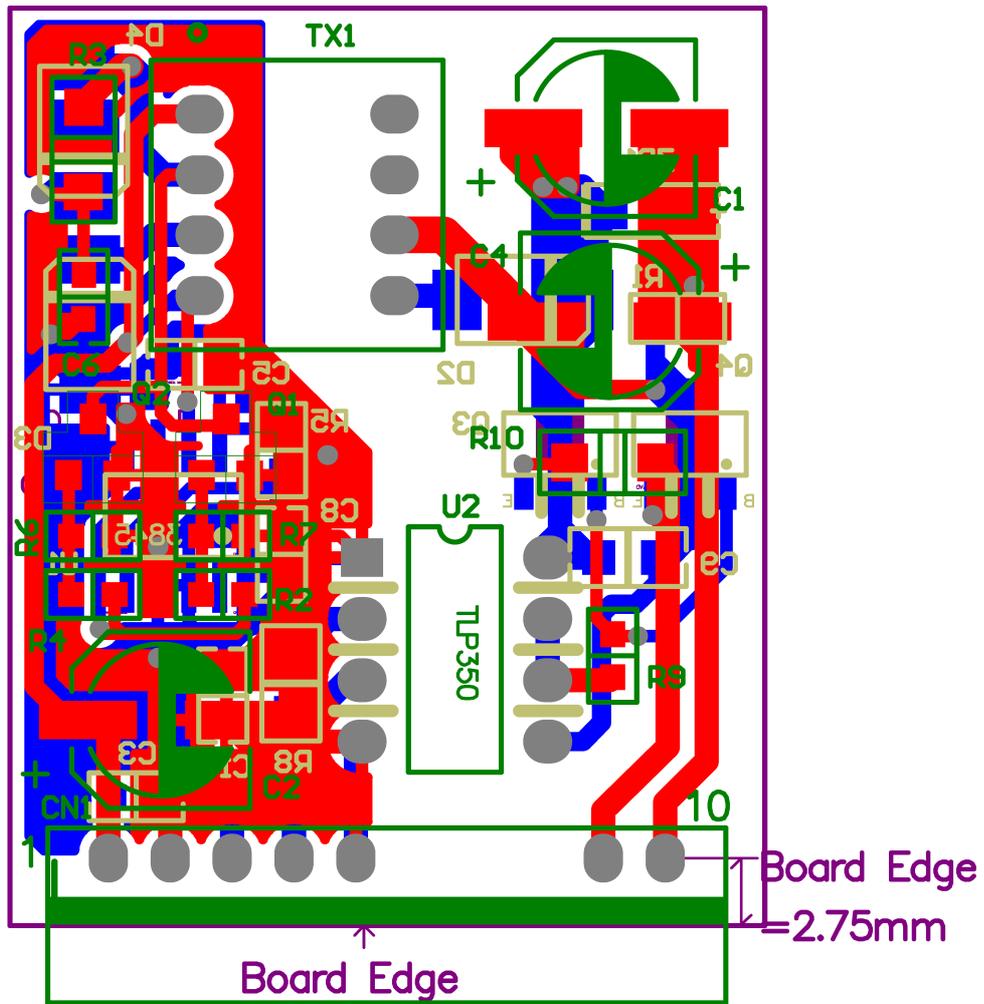


Figure B.3: The PCB layout of the IGBT driver board (TI, 2015a).

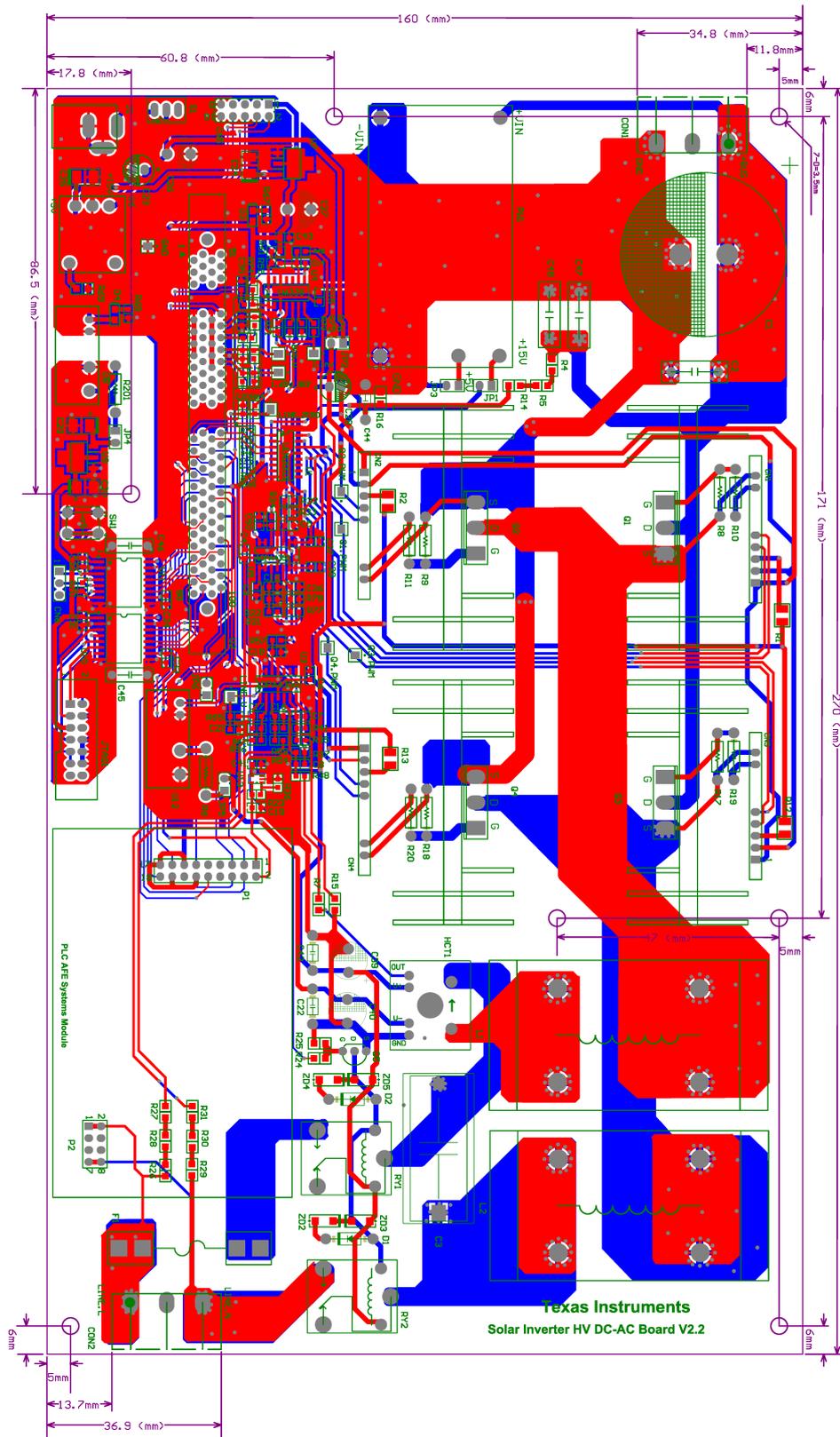


Figure B.4: The PCB layout of the TI HV solar dc/ac board (TI, 2015a).

B.0.2 Measurements of the Voltage and the Current

The inductor current is measured with the hall current sensor, while both the dc bus voltage and the ac output voltage were measured via resistors. According to Figure B.5, it is very simple to get the sample ratio of the dc bus voltage:

$$K_{rdc} = \frac{R_6}{R_4 + R_5 + R_{14} + R_6} = 0.003322. \quad (\text{B.1})$$

According to Figure B.5 and Figure B.6(a), for the ac output voltage, the differential circuit is used and the sample ratio is:

$$K_{rac} = \frac{R_{59}}{R_{26} + R_{27} + R_{28} + R_{54}} = 0.003311. \quad (\text{B.2})$$

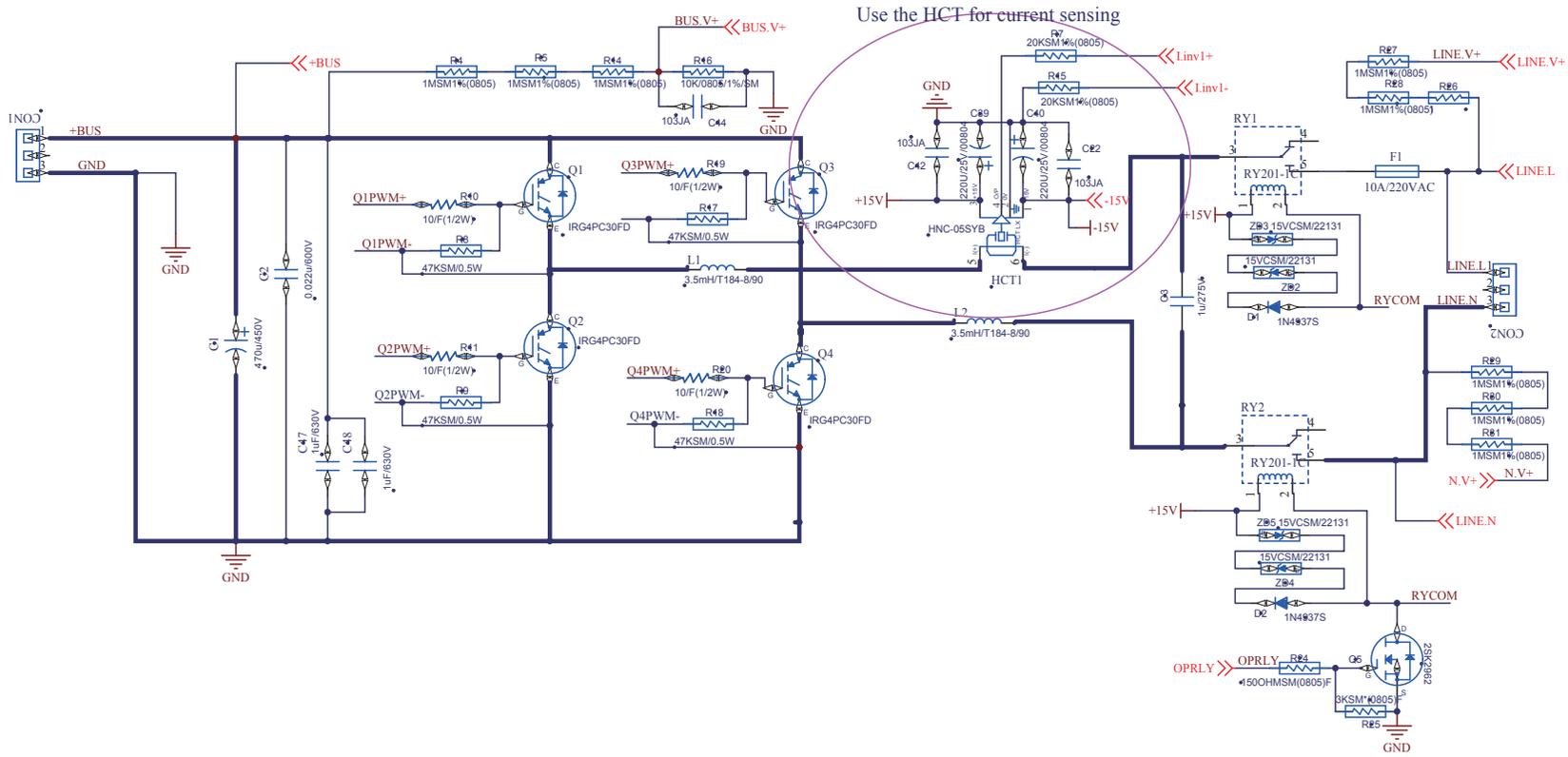
For the inductor current sensing, both the sample ratio of the hall sensor and the differential circuit need to be considered:

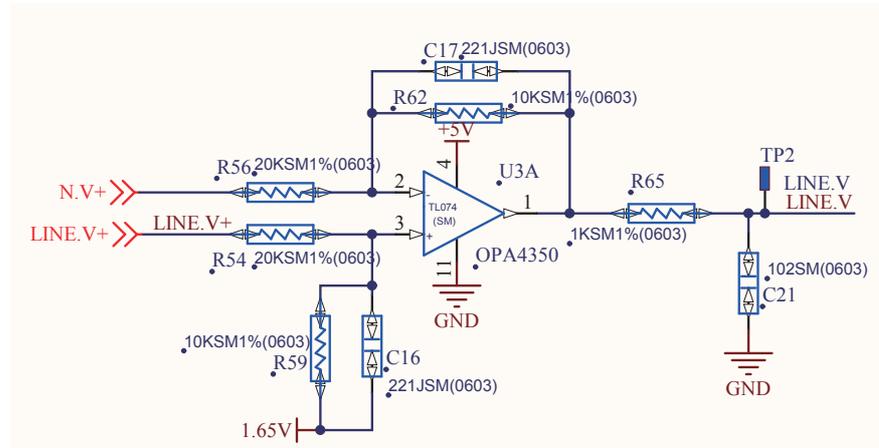
$$K_{rc} = K_{hall} \frac{R_{41}}{R_{35} + R_{15}} = 0.15974 \quad (\text{B.3})$$

where

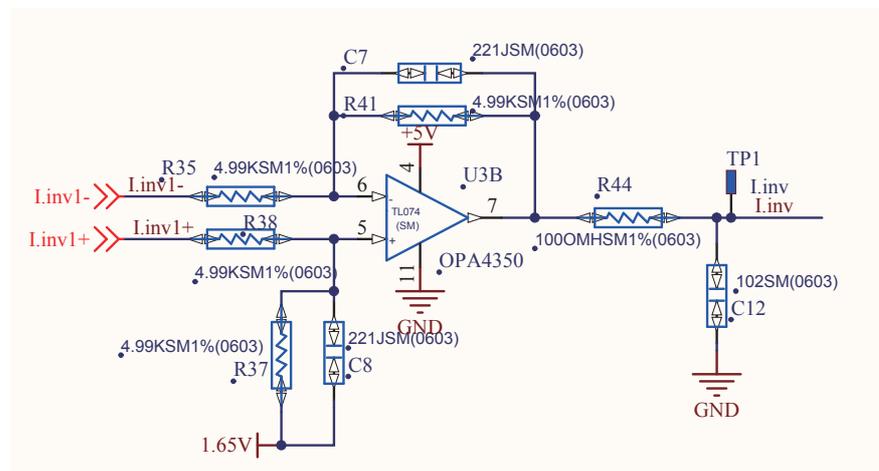
$$K_{hall} = 0.8. \quad (\text{B.4})$$

Figure B.5: The circuit of the TI dc/ac board (TI, 2015a).





(a) The measurement of the ac output voltage



(b) The measurement of the inductor current

Figure B.6: The measurement of the ac outout voltage and the inductor current (TI, 2015a).