Low-Cost Fabrication Techniques for RF Microelectromechanical systems (MEMS) Switches and Varactors

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Declaration of Academic Integrity

The candidate confirms that the work submitted is his own and that appropriate credit has been given where reference has been made to the work of others.

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Chapter 4 and 5 of this thesis includes work published in the co-authored journal.

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Abstract

A novel low-cost microfabrication technique for manufacturing RF MEMS switches and varactors is proposed. The fabrication process entails laser microstructuring and non-clean room micro-lithography standard wet bench techniques. An optimized laser microstructuring technique was employed to fabricate the MEMS component members and masks with readily available materials that include, Aluminum foils, sheets, and copper clad PCB boards. The non-clean room micro-lithography process was optimized to make for the patterning of the MEMS dielectric and bridge support layers, which were derived from deposits of negative-tone photosensitive epoxy-based polymers, SU-8 resins (glycidyl-ether-bisphenol-A novolac) and photoacid activated ADEX™ dry films. The novel microfabrication technique offers comparatively reasonably yields without intensive cleanroom manufacturing techniques and their associated equipment and processing costs. It is an optimized hybrid rapid prototyping manufacturing process that makes for a reduction in build cycles while ensuring good turnarounds.

The techniques are characterized by analysing each contributing technology and dependent parameters: laser structuring, lithography and spin coating and thin film emboss. They are developed for planar substrates and can be modified to suit specific work material for optimized outcomes. The optimized laser structuring process offers ablation for pitches as small as 75 µm (track width of 50 µm and gap 25 µm), with a deviation of 3.5 % in the structured vector's dimensions relative to design. The lithography process also developed for planar and microchannel applications makes for the realization of highly resolved patterned deposits of the SU-8 resin and the laminated ADEX™ polymer from 1 µm to 6 µm and with an accuracy $\pm$0.2 µm.

The complete micro-fabrication technique fabrication techniques are demonstrated by realizing test structures consisting of RF MEMS switches and varactors on FR4 substrates. Both MEMS structures and FR4 substrate were integrated by employing the micro-patterned polymers, developed from dry-film ADEX™ and SU-8 deposits, to make for a functional composite assembly. Average fabrication yield up to 60 % was achieved, calculated from ten fabrication attempts. The RF measurement results show that the RF MEMS devices fabricated by using the novel micro-fabrication process have good figure-of-merits, at much lower overall fabrication costs, as compared to the devices fabricated by conventional cleanroom process, enabling it to be used as a very good micro-fabrication process for cost-effective rapid prototyping of MEMS.

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List of Abbreviations

ALD	Atomic layer deposition
APCVD	Atmospheric and Low-Pressure Chemical Vapour Deposition
ARE	Activated Reactive Evaporation
CAD	Computer-aided design
CAM	Computer-aided manufacturing
CPW	Coplanar waveguide
CVD	Chemical vapour deposition
DUV	Deep ultraviolet
ED	Electrodeposition
FCA	Filtered and unfiltered arc cathodic deposition
ICP	Ion Coupled Plasma
IPA	Isopropyl alcohol
LICVD	Laser Induced Chemical Vapour Deposition
MEMS	Microelectromechanical systems
MMIC	Monolithic Microwave Integrated Circuits
MOCVD	Metalorganic CVD
OFAT	One factor a time
PCB	Printed circuit board
PEB	Post-exposure bake
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PET	Polyethylene terephthalate
PGMEA	Propylene glycol methyl ether acetate
PLD	Pulsed laser deposition
PVD	Physical vapour deposition
RIE	Reactive ion etching
RTCVD	Rapid thermal CVD
S-parameter	Scattering parameter

Chapter 1
Introduction

Microelectromechanical systems (MEMS) is the integration of mechanical, sensing and electrical elements on the substrate through the utilization of microfabrication technology to produce miniature devices. These devices are batch fabricated with integrated circuit process sequences and micromachining processes to form their mechanical and electrical elements. They are broadly classified into sensors and actuators, with the former converting physical stimuli, events, and parameters into electrical, optical and mechanical signals, whereas the latter performs a conversion to mechanical motion of the applied electrical stimuli.

Extant fabrication process for MEMS devices is described by clean room techniques. These processes are complex, require advanced equipment are markedly costly to install and maintain; demand significant footprint, and are encumbered by long-term cost of ownership, in relation to utilization and throughput [1, 2].

Applications for MEMS devices are in inkjet heads, microfluidics, aerospace, satellite, planar array antennas, filters, and automation, with a global 2017 market value estimated at $12.5 billion, up from $10.35 billion in 2016. The RF market share of this market is reported to be the highest contribution at 17.3 %, with a compound annual growth rate (CAGR) of 9.8 % [3]. Major drivers of this sector are from: increased demand for smartphone and wearable devices; augmented reality (AR) and virtual reality (VR) market penetration; the rise in concerns for passenger safety and regulatory norms-leading to opportunities in the efficiency of vehicular safety features e.g. airbags, electronic stability control, tire pressure monitoring. Additional market drivers include new potentials for growth in automation, healthcare applications, space tourism, the increasingly expanding ecosystem of the internet of things (IoT), which comprises connected vehicles and unmanned aerial vehicles (UAVs), among others [3].

The global MEMS market can be segmented based on functional characteristics and industry vertical. Under functional characteristics, the market is bifurcated into sensors (accelerometers, pressure sensors, inertial combos, microphones among other) and actuators (inkjet systems, optical MEMS, oscillators, RF MEMS, microfluidic etc. The market can also be

categorized by industrial applications into consumer electronics, telecommunications, healthcare, automotive, industrial, aerospace and defence [3,4].

Radant MEMS, DelfMEMS, Robert Bosch GmbH, Denso, STMicroelectronics, Qualcomm/NXP Semiconductors, Broadcom, Qorvo, Canon Inc., Omron Corporation, Texas Instrument Inc., Honeywell International Inc., Taiwan Semiconductor Manufacturing Co. Ltd., and Panasonic Corp, are among the principal members of the supply chain, comprising device makers, integrators, research and developments, and verticals. Growth in the MEMS and sensors market is however encumbered by highly complex manufacturing processes and the absence of standardized fabrication techniques [3,5].

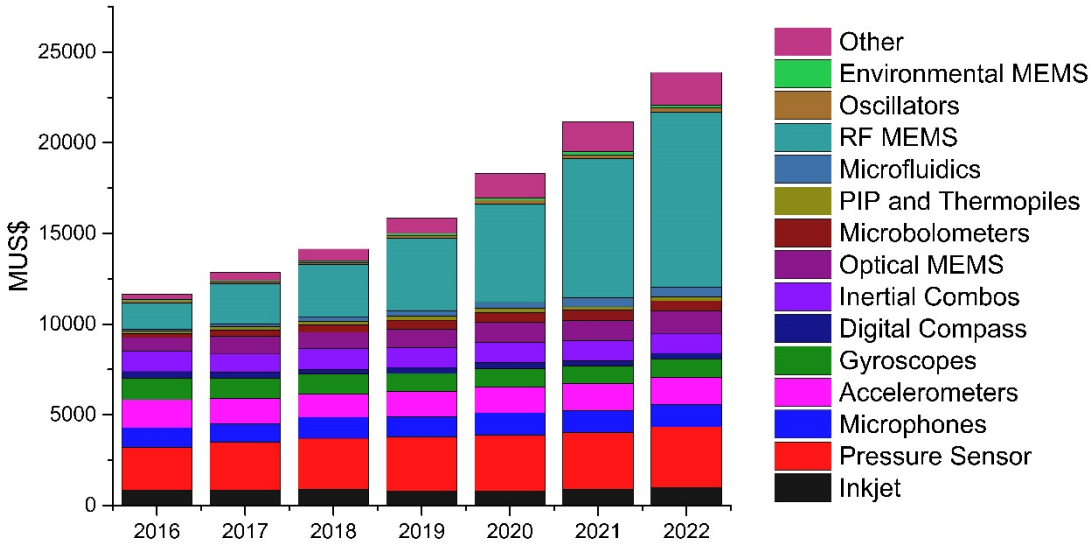

Figure 1.1 MEMS and sensor device market share forecast from 2016 to 2022 [5].

The sectorial market share chart is shown in Fig. 1.1 [5], delineates MEMS devices by functions and a global size value. As observed, RF MEMS devices enjoy a consolidated market size, with up to 50 % of yearly revenue, due to its application to a wide range of electronics. This large market share value has enamoured this sector to strategic investments, and complementary research into improving functional characteristics, manufacturing processes, device value chain and yields, to make for increased return on investments. 2018 to 2022 market forecasts and projected growth are hinged on improved yields with simplified fabrication processes, that would, in turn, lead to more compact efficient, economic MEMS production lines [3].

MEMS switches, varactors and phase shifters constitute principal MEMS RF devices and are employed to achieve signal isolation and transmission line impedance variation with loaded and distributive capacitive sections. These

responses are with minimal power requirements, intermodulation products and relative ease of integration to ancillary components. An RF MEMS switch marketed by Omron is shown in Fig. 1.2 a) with the external casing and the internal electrode assembly b), includes two switches housed in a ceramic surface-mount package with external contact pads, constituting a single-pole-double-throw (SPDT) switch.

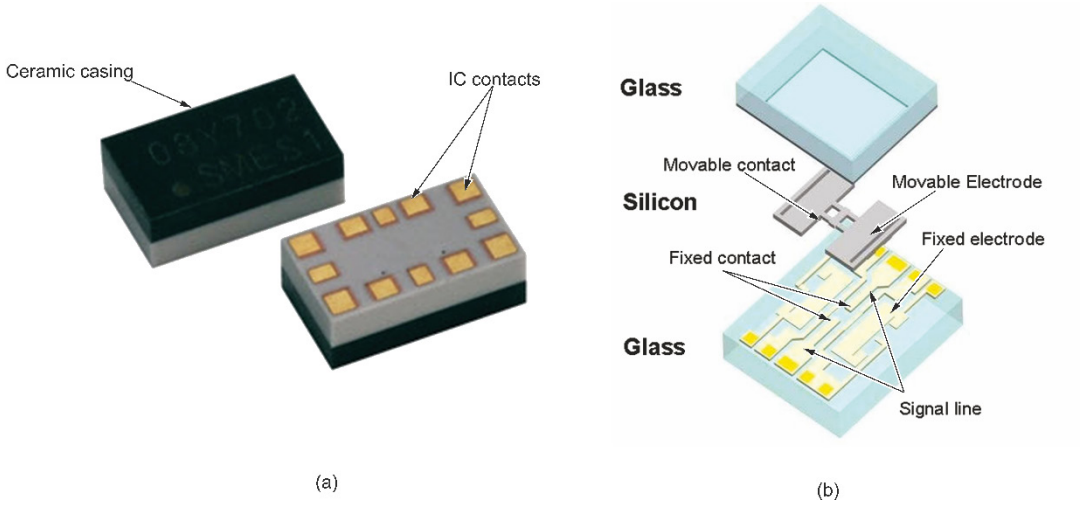

Figure 1.2 Omron SPDT MEMS RF switch [6].

1.1 Motivation and Objectives

Expanding rapidly from the 1990's, the field of MEMS has grown from polysilicon based materials as deflecting members and wafers to embracing metal actuators and printed circuit board (PCB) substrates. Studies into the development of low-loss low power controlled circuits, including SPST (Single Pole-Single-Throw), and switched line phase shifters have been reported in [7]. These devices while offering inherent advantages over semiconductor junction based analogues, operate in their design frequency range without intermodulation distortions and other accompanying non-linearity challenges, which become markedly pronounced in RF applications, unlike p-type, intrinsic, n-type (PIN) junction devices.

Microfabrication technologies are employed to realize these devices and make for system-wide integration while meeting the desired design objectives. This thus allows for the monolithic development of whole communication systems at reduced cost and a minimization of associated build losses with the possibility of extension into bulk yields [8].

Extant microfabrication techniques for RF MEMS are clean room based, and consist of intricate development cycles, which includes metal and dielectric film depositions, material etching and chemical processes. Cleanroom

fabrication process and equipment requirements as well as the associated investment and operational costs, ensure relatively steep budgets are required to manufacture MEMS structures.

Recent efforts aimed at cost reduction for MEMS micro-fabrication involved polymer-based materials employed as both dielectric and adhesive bonds, with layer transfer facilitated by volume stamping or spin coating [2]. In addition, interest in alternatives to traditional cleanroom based substrates has been reported with studies involving ceramics and fibreglass-based PCB substrates [2], [9-13].

This work derives from these efforts and aims to present a novel micro-fabrication method for realizing MEMS devices, without intensive clean room techniques and the associated mitigating equipment cost. The process developed aims to ensure sufficient bonding, with minimal packaging requirement of additional RF devices on PCB. The proposed method also seeks to maximize yields at each point of the fabrication process, and with simple development cycles. This thesis presents the MEMS device design topologies, and optimization techniques employed to realize this cost-effective process. A comparison of the response of devices fabricated using this method relative to those reported in other works is also presented.

1.2 Thesis Outline

Chapter 2 presents a literature overview of MEMS device technology, the operational principles of MEMS switches and varactors, is explored. While a discussion on the intricacies that attend conventional clean room fabrication methods, alongside a definitive examination of fabrication evaluation metrics, the background theory of extant optimization routines are presented in Chapter 3.

Chapter 4 examines the adopted layout designs for both MEMS shunt switch and varactor devices, including a detailed presentation of design steps from the CPW transmission line to the bridge.

Chapter 5 discusses the characterization of the equipment to be employed and presents the novel fabrication technique with an examination of the laser ablation and structuring method of the LPKF ProtoLaser U3™, used to fabricate the MEMS devices and transmission lines. The wet bench process consisting of standard lithography components, equipment, and a dry film resist emboss for the MEMS shunt switch device is also discussed here. The optimized routine for the proposed process is presented in this chapter.

Chapter 6 reports on the RF response of the MEMS devices, with measurements obtained from the Agilent E8361A Performance Network Analyser, and the actuation by applied bias from a DC voltage generator. The associated yield of this wet bench dry film emboss process is also presented. The performance of our fabricated device compared with those obtained from clean room based fabrication methods is also examined.

Chapter 7 concludes this work with a summary of achievements and recommends potential areas for improvements.

Chapter 2
MEMS literature review: Switching and design

Microelectromechanical systems (MEMS) have been developed for microwave and millimetre circuits where low-loss performance and tunable characteristics are desired. RF MEMS devices have been employed as switches [14]; phase shifters [15, 16], varactors in tunable coplanar patch antenna [17] and as resonators [1]. Their inherent advantages over solid state analogues have ensured their deployment in phase array circuits, LC filters, in-line switches, and in advanced applications like beam steering and robotics.

In this chapter, the underlying principle of operation of MEMS switches, are examined, alongside adopted bridge designs.

2.1 MEMS switches: An introduction

MEMS switches developed as offshoots of microsensor elements and fabrication techniques. They are used for signal processing, where a discrimination into binary states of an RF transmission line is required. They make ideal substitutes for solid state device like PIN diodes and field effect transistors (FETS) and are comparatively advantageous in comparison with their semiconductor analogues. These include superior isolation response, minimal power requirements being passive devices, and extended RF range capabilities due to minimal parasitics. They also offer high linear RF responses without intermodulation challenges or phase distortion. Major drawbacks associated with MEMS switches include higher actuation voltages, comparatively slower switching times relative to p-type, intrinsic, n-type (PIN) diodes and FETs, reliability concerns with repeated actuation cycles. Improvements in the switching speed down to nanosecond speeds has been reported in [18], with increased miniaturization to obtain faster speeds for use as Distributed MEMS phase shifters, reported in [19]. Reduced actuation alongside improved cycles was reported in [20] with a bridge design that made for lower spring constant contribution. Work on significantly reduced actuation voltages, less than 5 V, facilitated with a design that employed a freely moving contact pad, where actuation was obtained without deformation was reported in [21]. A shunt switch with serpentine suspensions to the bridge to make for lower actuation voltages was examined in [14]. Additional work by [22] focused on improving the device power handling capabilities, up to 40 dBm, with further work reported in [23] and [24].

Areas of application include redundancy switches, phase shifter matrices and space systems. RF MEMS switches find ready application due to their ease of integration in wireless communication systems, as switching devices, phase shifters, reconfigurable integrated circuits, electronic warfare (EW) equipment, and missile tracking radar, incorporating electronic steering-phased array antennas, where phase distortion is not acceptable [25].

The impedance ratio of the switch in it's on state relative to the off state is frequency dependent since it is dependent on the capacitance. It is expressed as the product, CR, a characteristic number and can be used as a figure of merit (FOM) for the device. A smaller FOM is better as it implies a small on impedance relative to the off impedance. The reciprocal of the FOM is called the cut off frequency and is also used as a metric. Thus we can make a better switch by reducing either R or C. The FOM was given a physical meaning as the description of the channel electron mobility and an assigned number to facilitate the ranking of switches in [26]. For various indicated switch geometries and materials in Table 2.1, substitution of expressions of C and R as functions of electron charge mobility allowed for ranking based on the derived assigned numbers. This analysis concluded that with MEMS switches, there is a degree of freedom available to the designer that does not exist with a semiconductor switch, which is the ability to set the gap independently of the materials. Thus the FOM can be reduced by as much as the bridge mechanical travel distance or gap. In addition, the change in dielectric from semiconductor to air gives a lower order magnitude for the capacitance. And thirdly that the effective area factor, $\mathrm{a_e}$, the dominant material property from $\mathrm{FOM{=}CR{=}(\varepsilon_0 A/G)\cdot(\rho l/A a_e)}$, has a theoretical limit of 10^{-4} since the resistivity of metal is in that order, relative to semiconductors. From the expression for FOM, ε_0, is the permittivity of free space, G is the conductance, ρ represents resistivity, and l is the length of the bridge geometry.

A tabular comparison of switches by family, with delineation along power consumption, switching speed, in line resistance, and capacitance, tabulated by [26].

Table 2.1 Comparison of families of switches [26].

Device	Class	Figure of Merit (fs)	Power (mW)	Capacitance (fF)	Resistance (Ω)
IMS-Small	Opto activated	4000	5	80	50
IMS-Large	Opto activated	3000	5	30	100
NE3290	FET	500	0	100	5
Blackwell	AlGaAs FET	270	0	170	1.6
Ma4gp022	GaAs PIN 4.5	220	5	110	2
MA4GP022	GaAs PIN 20	110	25	110	1
Raytheon	MEMS membrane	12	0	35	0.35
Rockwell	MEMS cantilever	2.5	0	11	0.22
COM DEV	Coaxial	0.07	0	0.35	0.2
ARPA-project.	MEMS	0.01	0	0.05	0.2

2.1.1 Classification of MEMS switches

RF MEMS switches can be categorized broadly by the direction of signal path flow as series or shunt switches. Additional classification can be made based on membrane structure configuration including bridges and cantilevers. They can also be delineated by contact type as ohmic or capacitive. While another classification distinguishes switches by the actuation mechanism into electrostatic, electromagnetic or thermal switch systems.

Bridge configurations are the most popular of switch membrane structure types, and terminations of the switch relative to the signal path can be in series

or shunt. In the former, the actuation of the electrode completes the signal path, whereas, with the latter, the signal path is shorted to the ground [16].

Electromagnetic actuation refers to the inducement of magnetic effect through the application of electricity, while magnetic actuation employs permanent magnets to allow for operation of the actuator. This actuation relies on the Lorentz force, F_L, induced and is defined as,

$$\overrightarrow{F_L} = L\vec{I} \times \vec{B} \tag{2.1}$$

where, L, refers to the conductor length, and B, defines the magnetic field from moving charges. Power requirements are relatively high, and the fabrication process can also be complicated, with the displacement range proportional to the actuator size. Table 2.2 shows the categorization of MEMS switches by the indicated subtypes.

Table 2.2 MEMS switch classification

Circuit type configuration	Actuation type	Contact type	Mechanical configuration	Armature direction
Series	Electrostatic	Ohmic	Cantilever	Broadside
Shunt	Electro-thermal	Capacitive	Bridge	In-line
	Electromagnetic Piezoelectric Shape Memory Alloy			

Electrothermal actuation consists of the application of current to the movable MEMs member such that heating results in the accompanying expansion or buckling of the beam and consequent lateral displacement. The process requires a significant amount of power and switching speeds are relatively slow [27].

Piezoelectric actuation relies on the response of compositional thin-film lead zirconium titanate (PZT) films on target regions, that deflect on the application of an electric field. They are limited in part by cycles of usage with regional stress at concentration points alongside issues with durability [28, 29].

Shape memory actuators rely on the materials which return to a predetermined shape when subjected to heat. The most readily employed memory alloy is NiTi, SMAs, At low temperatures, the material is martensite, i.e ductile and easily deformed. Heating the deformed material results in an austenite state, with the deformation induced at low temperatures being fully

recoverable. This phenomenon referred to as pseudo-elasticity, lends itself for use in actuators, with repeats of the deformation and heating cycle. This family of actuators is limited by the two-way effect, where an antagonistic mechanism is required to return the deformed NiTi to its initial shape for the next cyclic cycle. There is also the additional manufacturing requirement for a bias force or spring mechanism. In addition, the manufacturing of the NiTi film into specific shapes using available processes is limited, and lately, narrow forays into dome shapes with 3D hot shaping have been reported [30].

Electrostatic actuation of the bridges is often preferred as no current flows in the device, and consequently, no power absorption is involved in the process [31]. Transmission conductor lines used to implement electrostatic actuation include microstrip lines and coplanar waveguides. Of the two, the latter is the most frequently employed. Coplanar waveguide (CPW) transmission line based switch configurations, exist as series or shunt terminations, and their RF and mechanical analysis are well described in several works [31]. CPWs consist of three conductor transmission lines, with the centre conductor sharing the same plane with two grounds on either side. In the ideal series configuration, an open circuit results when in the zero bias or up-state condition, with infinite isolation presented, whereas a short circuit occurs when the bridge is actuated, with zero insertion loss response. A coplanar RF shunt switch consists of a thin metallic membrane suspended over a CPW signal transmission line, with either end anchored to ground planes. By definition, the ideal shunt switch presents zero loading and reflection effect in the upstate, i.e., with the beam not deflected, and in the absence of actuating forces, until when applied between the bridge and the centre line, which cause beam deflection, the down-state condition, with high isolation presented to the travelling signals. A dielectric film deposited at the switch-transmission line interface limits stiction effects, where the metal surfaces should have been in contact. It also makes for an increase in the capacitive loading of the line [32]. Stiction refers to the tendency of moving parts of micromechanical parts to adhere to contact points, due to friction and capacitive static forces, with device failure occurring when restoring forces are incapable of counteracting the adhesive forces. The shunt switch configuration is preferred over series termination, due to minimal parasitics involved in the switch operation. It also allows for ease of fabrication, and the switches in this configuration can handle four times more RF power and operate in the higher frequency region compared to series switch. Series switches are more suited for lower frequencies, due to the propagation of surface modes at higher frequencies beyond 4 GHz, which hinders their operation [33]. High MEMS isolation

switches with 40 dB isolation in the downstate, and -15 dB return loss in the upstate at 40 GHz, effectively tuning out reflections, and improving isolation and return loss was reported in [34, 35].

The degree of isolation provided by a MEMS switch describes a performance metric or figure of merit and is the ratio of the up-state capacitance to down-state capacitance. For switches, this value is typical, 30 to 150, while another variation of the capacitive switch called a varactor, operates in ratios between 1.5 to 6 [18]. A compendium of seminal works of studies of MEMS switches compiled by [36] provides pivotal insight into early research into the late twentieth century, alongside accompanying background theory and various applications of these micro-devices.

2.1.1.1 MEMS shunt switch model and equivalent circuit

A MEMS shunt switch is illustrated in Fig. 2.1, in both isometric, cross-sectional views, with the accompanying equivalent circuit model. The device geometry parameters follow similar definitions as presented in Chapter 4.

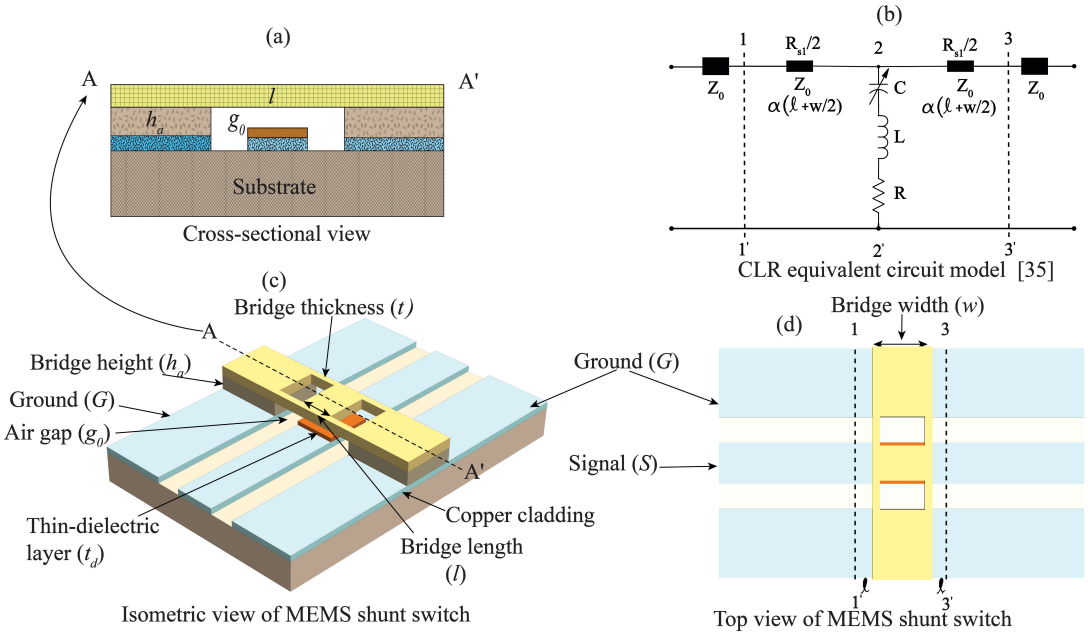

Figure 2.1 Isometric, cross-sectional views and equivalent circuit representation of a MEMS shunt switch.

The MEMS shunt switch depicted in Fig. 2.1 is l μm long, w μm wide, t μm thickness, is suspended, h_a μm, above a coplanar waveguide (CPW), with an effective air gap, g_0 μm, from a thin dielectic layer of thickness, t_d μm, on the CPW signal line. Typical bridge height is up to 5 μm, and materials often employed in the fabrication of the bridge include, Copper, Gold, Aluminium, Titanuim, Ruthenium, and Silver. The coplanar waveguide consists of a planar transmission line composed of two ground planes and a signal line on

a substrate. This transmission line geometry, defined by the ratio of slot-signal-slot widths, $G/S/G$, the substrate dielectric value, and thickness determine its characteristic impedance, Z_0. Typical substrate materials employed in MEMS include quartz, PCB glass fibre, ceramic, silicon, Gallium Arsenide (GaAs), Alumina, Aluminium titanium carbide ($\mathrm{AlTi_2C}$). The coplanar waveguide can be a conventional ungrounded CPW, or one backed by a conductor, CBCPW, or can consist of derivatives of either with multilayer dielectric compositions.

2.1.1.1.1 CLR impedance model of MEMS shunt switch

The MEMS switch is modelled by the lumped impedance network [35] shown in Fig. 2.1 (b). Two short sections of the transmission line and a lumped CLR model describe the bridge capacitance having the up-state (OFF) and down-state (ON) values. The length of the transmission line sections are is $\ell + {}^{W}/_{2}$, where ℓ, is the distance from the MEMS edge to the line reference plane. The shunt impedance of the switch is given by series element sum of the resistive, inductive and capacitive sections describing the bridge,

$$Z_s = R_s + j\omega L + \frac{1}{j\omega C_{u,d}} \tag{2.1}$$

where the capacitance of the bridge in both OFF and ON states are represented by C_u, and C_d respectively. At resonance the resonant frequency, f_0, of the lumped CLR loop is given as [37],

$$f_0 = \left(2\pi\sqrt{LC}\right)^{-1} \tag{2.2}$$

and the CLR model reduces to the series resistance of the MEMS bridge.

An approximation for the impedance of the shunt switch in (2.1) is defined by operational frequency relative to this resonant frequency [37],

$$Z_s = \begin{cases} (j\omega C)^{-1} & \text{for } f \ll f_0 \\ R_s & \text{for } f = f_0 \\ j\omega L & \text{for } f \gg f_0 \end{cases} \tag{2.3}$$

The impedance response of the switch approximates that of an inductor for frequencies above the resonant frequency, and a capacitor for frequencies below this frequency. Typical values of capacitance for MEMS switches are from 35 fF to 3 pF, with inductance values around 8 pH [35].

The upstate capacitance of the bridge of the parallel bridge capacitor in series with the thin dielectric layer, of thickness, t_d, is given by [35],

$$C_u = \frac{\varepsilon_0 wS}{\left(g + {}^{t_d}/_{\varepsilon_r}\right)} \quad (2.4),$$

and, the downstate capacitance by [35],

$$C_d = \frac{\varepsilon_0 wS}{t_d} \quad (2.5)$$

The equivalent circuit of the MEMS shunt switch is a two-port shunt element matrix. The impedance components of this two-port circuit can be expressed as functions of S-parameters where, $V_p{}^+$ and $V_p{}^-$, are the incident and reflected components of impressed voltages at ports $p = 1,2$ [38].

$$V_1 = V_2 \quad (2.6)$$

$$I_1 + I_2 = Y_s V_2 \quad (2.7)$$

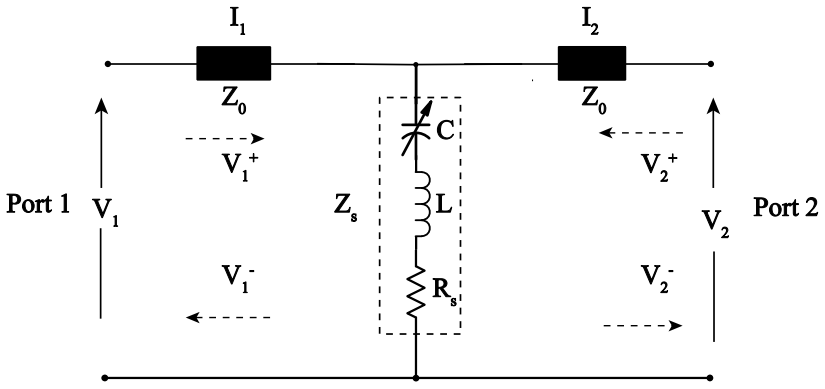

Figure 2.2 Two port equivalent representation of a MEMS shunt switch [35, 38- 39].

The return loss, S_{11}, is derived by terminating port two, thus reducing $V_2{}^+$ to zero. Consequently, the voltage impressed on port 2 is given as [38, 39],

$$V_1{}^+ + V_1{}^- = V_2{}^- \quad (2.8)$$

Hence,

$$Y_0\left(V_1{}^+ - V_1{}^-\right) = Y_0 V_2{}^- + Y_s V_2{}^- = V_2{}^-(Y_0 + Y_s) \quad (2.9)$$

From (2.8),

$$V_1{}^- = V_2{}^- - V_1{}^+ \quad (2.10)$$

Substituting, (2.9) in (2.10) results in [38],

$$V_1{}^- = \frac{Y_0}{(Y_0 + Y_s)}\left(V_1{}^+ - V_1{}^-\right) - V_1{}^+ \quad (2.11a)$$

Hence (2.11a) can be rewritten to indicate the reflection coefficient, S_{11}, observed in port 1 and is given as [38],

$$S_{11} = \frac{V_1{}^-}{V_1{}^+} = \frac{Y_0 - (Y_0 + Y_s)}{Y_0 + (Y_0 + Y_s)} = \frac{Z_0 \parallel Z_s - Z_0}{Z_0 \parallel Z_s + Z_0} \quad (2.11b)$$

By the same token, the insertion loss, S_{21} is given as [38],

$$S_{21} = \frac{V_2^-}{V_1^+} = \frac{V_1^+ + V_1^-}{V_1^+} = 1 + S_{11} = \frac{2Z_s \parallel Z_0}{Z_0 \parallel Z_s + Z_0} \tag{2.12}$$

For symmetrical networks, $S_{11} = S_{22}$, and $S_{21} = S_{12}$. In addition, the series resistance of the MEMS bridge at this resonant frequency, when $Z_s = R_s$, is related to the insertion loss by [35],

$$S_{21f_0} = \frac{2R_s \parallel Z_0}{Z_0 \parallel R_s + Z_0} \simeq \frac{2R_s}{R_s + Z_0} \tag{2.13}$$

The power loss of the shunt switch consists not only of the insertion component, $|S_{21}|^2$ but also the reflected power impressed on the switch, $|S_{11}|^2$ [35],

$$Loss = \frac{Power\ loss\ in\ the\ MEMS\ bridge}{Power\ impressed\ on\ the\ switch} = \frac{{I_s}^2 R_s}{{|V_1^+|^2}/{Z_0}} \tag{2.14}$$

Equation (2.14) can be rewritten with both numerator and denominator multiplied by $|Z_s|^2$, with , $V_2^- = I_s Z_s$, and expressed as,

$$= \frac{{I_s}^2 R_s}{|V_1^+|^2/Z_0} \cdot \left|\frac{Z_s}{Z_s}\right|^2 \tag{2.15}$$

$$= \left|\frac{V_2^-}{V_1^+}\right|^2 \cdot \frac{R_s Z_0}{|Z_s|^2} = \left|\frac{2Z_s \| Z_0}{Z_0 \| Z_s + Z_0}\right|^2 \cdot \frac{R_s Z_0}{|Z_s|^2} \tag{2.16}$$

Extraction of the upstate capacitance from S-parameter measurements can be obtained from two conditions indicated in (2.17) while neglecting the negligible LR_s in this state [37],

$$S_{11} = \begin{cases} -j\omega C_u Z_0/2 + j\omega C_u Z_0 & \text{for} \quad \omega C_u Z_0 > 2 \\ \left|\omega C_u Z_0/2\right| & \text{for} \quad \omega C_u Z_0 \ll 2 \end{cases} \tag{2.17}$$

And for conditions indicated in (2.3) and (2.13) the relationship between the transmission loss and the two port circuit parameters is given as [37],

$$S_{21} \simeq \begin{cases} 2/\omega C_d Z_0 & \text{for} \quad f \ll f_0 \\ 2R_s/Z_0 & \text{for} \quad f = f_0 \\ 4\omega L/Z_0 & \text{for} \quad f \gg f_0 \end{cases} \tag{2.18}$$

The degree of discrimination by the switch is indicated by the capacitance ratio, C_r, with values up to 100. It is defined as the ratio of down state to off state, with the former impacted by the roughness of the contact surface area [40].

$$C_r = \frac{\frac{\varepsilon_0 wS}{t_d}}{\frac{\varepsilon_0 wS}{\left(g + {}^{t_d}/_{\varepsilon_r}\right)}} \tag{2.19}$$

where, ε_0, is the permittivity of free space; w, is the MEMS bridge width; S, is the signal line width; g is the zero bias air gap height, and t_d, is the signal line dielectric thickness. A typical MEMS switch capacitance contains a substantial amount of fringe capacitance, C_f, typically, 20 % to 60 % of the off state capacitance and must be account for in the design of the switch.

The resistance associated with a MEMS switch consists of two components, the transmission line loss, and the other due to the MEMS bridge. The former is both ohmic and dielectric, is defined as a function of the line attenuation, and its magnitude is dependent on the measurement reference plane [35].

$$\alpha = \frac{{}^{R_{s1}}/_{\ell}}{2Z_0} \tag{2.20}$$

Attenuation measured from the transmission line can be used to derive R_{s1}, with measured losses of 0.06 Ω reported by [35], on a 0.8 μm Au CPW transmission line. The resistive loss component due to the bridge can be extracted from measured scattering parameters (S-parameters), and based on the assumption of uniform current distribution, the associated skin depth,$\delta = \left(\sqrt{f\pi\mu\sigma}\right)^{-1}$, allows for an estimation of the bridge resistance at the measured frequency of interest.

The bridge inductance is modelled as series inductance, and due to the localization of the CPW current distribution at the edge of both signal and ground planes, portions of the bridge over these planes do not contribute inductance. MEMS bridge inductances are typically low, in the pH range, due to this phenomenon, with the highest inductance contribution coming from the portion of the bridge above the CPW gap [35].

2.1.1.1.2 Electro-mechanical model of MEMS switches

The switch is anchored to the ground planes with actuation brought about by the application of a DC voltage between the bridge and the centre signal line. The mechanical response of the switch under electrostatic forces is a dynamic system and can be modelled by a mass damped spring model indicated in Fig. 2.3.

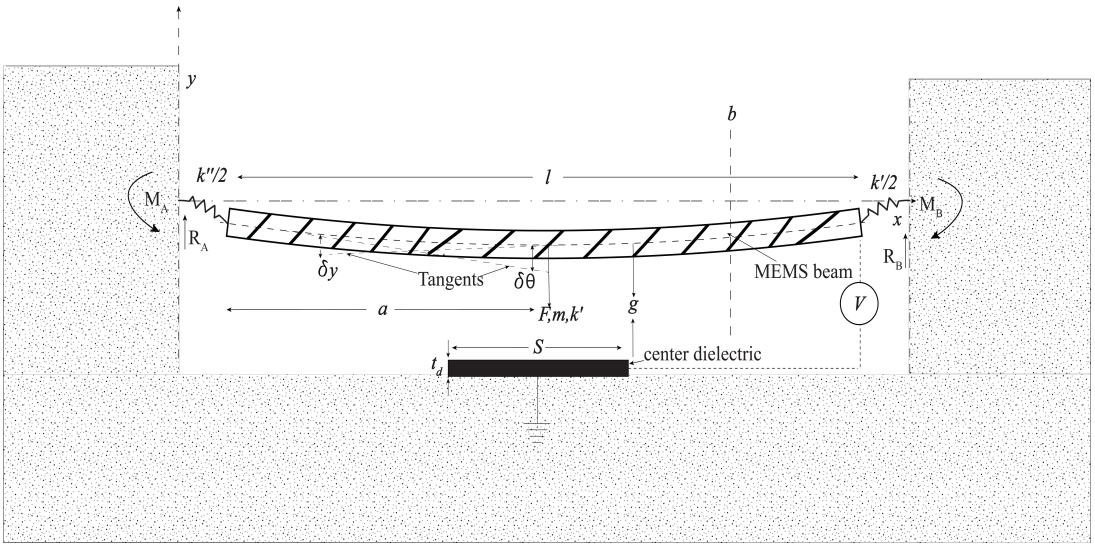

Figure 2.3 Sectional view of the electro-mechanical model of a MEMS shunt switch [37, 43].

The inertia of this system derives from the homogeneity of the beam's material properties, such as Young Modulus, $E\ (Pa)$, and is referred to as the single point lumped mass effect. The spring system stores energy in compressed states, and consists of spring constant $k\ (^{N}/_{m})$, which is composed of two parts, the stiffness of the bridge, k', and the biaxial residual stress constant, k'' . The former is dependent on the Young modulus, $E\ (Pa)$, and the moment of inertia, $I\ (m^4)$. The latter is derives from the residual stress, $\sigma\ (Pa)$ within the beam and is defined by the fabrication process employed [7].

The fixed to fixed bridge structure is represented by a rigid rectangular mass system with four massless springs at the corners of the mass section. Cartesian coordinates are in the x, y, and z-direction, with angles of rotation in the θ, ϕ, and φ. Dimensions, L_{kx}, and L_{ky}, are distances from the mass centroid along the x and y axis. $k_x{}'$, $k_y{}'$, and $k_z{}'$, are the stiffness constants in the x, y and z directions. The free body diagram of the fixed to fixed switch bridge is indicated in fig. 2.4.

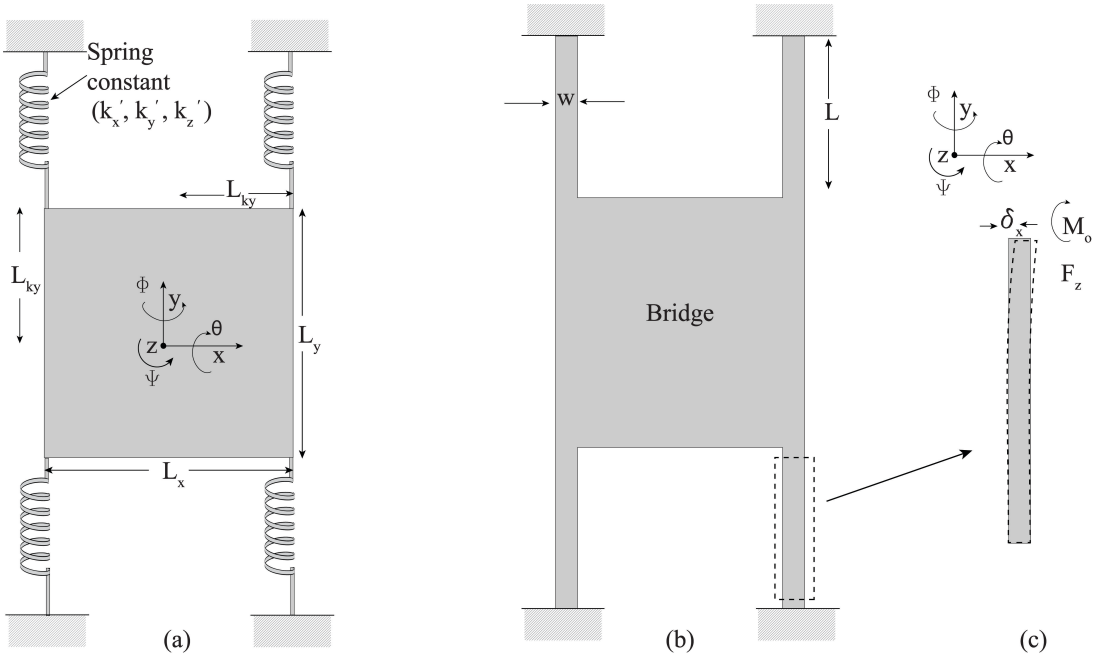

Figure 2.4 Mechanical mass-spring model of the MEMS shunt switch with an expanded guided beam end section [41].

A derivation of the spring constants in [41] follows from exploiting the symmetry of the system. Since the system is a four spring, two-fold symmetry structure, an analysis of one spring returns the spring constant which is a quarter of the total system spring constant. Equations employed to derive the spring constant is based on Castigliano's second theorem, which states that when a linearly elastic system is statically loaded, the distribution of stress is such as to make the strain energy a minimum consistent with equilibrium and imposed boundary conditions. It can be restated for structures in the mathematical form, as the partial derivative of the strain energy with respect to an applied force (or couple) is equal to the displacement or rotation of the force (or couple) along its line of action [42]. Thus by neglecting the residual and extensional stress, it can be defined as the partial derivative of the strain energy of a structure, U, with respect to an applied force equal to the displacement at the point of application of the load, P. This also extends to moments M, and the resulting angular displacement, θ, from the couple. The mathematical expression for the Castigliano's second theorem is given as follows [41],

$$\delta_i = \frac{\partial U}{\partial P_i} \tag{2.21}$$

$$\theta_i = \frac{\partial U}{\partial M_i} \tag{2.22}$$

where, δ_i and θ_i are infinitely small lateral and angular displacements of the beam respectively along the x-axis. The applied perpendicular force or load

along the z axis, for a bending moment, $M = M_0 - F_z\xi$, and the resultant displacement δ_z; ξ, is the distance from the guided beam end. The resultant strain energy of the beam under this force is given by (2.23) and the moment of inertia by (2.24),

$$U = \int_0^L \frac{M^2}{2EI_x} d\xi \tag{2.23}$$

$$I_x = \int_{-w/2}^{w/2} \int_{-t/2}^{t/2} x^2 dx dz = \frac{t^3 w}{12} \tag{2.24}$$

With initial constraints, $\psi_0 = 0$, and $M = M_0 - F_z\xi$,

$$\psi_0 = \frac{\partial U}{\partial M_0} = \int_0^L \frac{M}{EI_x} \frac{\partial M}{\partial M_0} d\xi = \frac{1}{EI_x} \int_0^L (M_0 - F_z\xi) d\xi = 0 \tag{2.25}$$

results in,

$$M_0 = F_z \frac{L}{2} \tag{2.26}$$

$$M = F_z \left(\frac{L}{2} - \xi\right) \tag{2.27},$$

with $\frac{\partial M}{\partial M_0}$, described as the moment per unit load [41].

Thus the deflection δ_z, is given as,

$$\delta_z = \frac{\partial U}{\partial F_z} = \int_0^L \frac{M}{EI_x} \frac{\partial M}{\partial F_z} d\xi \tag{2.28}$$

From (2.27),

$$\frac{\partial M}{\partial F_z} = \left(\frac{L}{2} - \xi\right) \tag{2.29}$$

Substituting, (2.27) and (2.29) in (2.28) results in,

$$\delta_z = \frac{F_z}{EI_x} \int_0^L \left(\frac{L}{2} - \xi\right)^2 d\xi = \frac{F_z L^3}{12EI_x} \tag{2.30}$$

With, $F_z = k' \delta_z$ [41],

$$k' = \frac{F_z}{\delta_z} = \frac{12EI_x}{L^3} = \frac{12E}{L^3} \cdot \frac{t^3 w}{12} = \frac{Ewt^3}{L^3} \tag{2.31}$$

and for a total of four springs,

$$k' = \frac{4Ewt^3}{L^3} \tag{2.32}$$

The applied force results in biaxial planar stress that is described by an extension of Hooke's law, in equations (2.33) [42],

$$\epsilon = \frac{1}{E}\sigma(1 - \nu) \tag{2.33},$$

and can be rewritten as,

$$\frac{F}{tw} = \sigma(1 - \nu) \tag{2.34}$$

where, the strain ϵ, is directional and is related to the strain, σ by the Young Modulus, E, and Poisson's ratio, ν. The associated spring constant, k'', for this biaxial stress derived is derived in [40], for a uniformly distributed load, obtained from the integral over the full length of the beam is given as,

$$k'' = \frac{8\sigma tw}{l}(1-\nu) \tag{2.35}$$

The supposition of the reaction moment and the vertical reactions of one end of the fixed non-compressive beam results in a general expression for spring constants. It is obtained as the sum of the beam stiffness and biaxial stress components for the beam suspended over a CPW centre conductor, with width, $S\ (m)$. The loaded beam with force distributed at the end of the beam of length, $l\ (m)$ results in the total spring constant given in (2.37), after a substitution of the beam stiffness and biaxial stress components is made,

$$k = k' + k'' \tag{2.36}$$

$$k = \frac{4Ewt^3}{L^3} + \frac{8\sigma(1-\nu)wt}{l} \tag{2.37}$$

An electrostatic force between the centre conductor and the bridge, brings about the deflection of the bridge towards the signal line, with an accompanying significant and abrupt change in the air-bridge capacitance interface. This electrostatic force is time-dependent and derived from the general expression of power applied to a parallel plate capacitor. It is given as,

$$F = \frac{1}{2}V^2\frac{dC(g)}{dg} \tag{2.38},$$

The parallel plate capacitance of the bridge capacitor provided by the width of the bridge, w, the CPW centre conductor, S, and the dielectric with thickness, t_d, is given as [35],

$$C = \frac{\varepsilon_0 wS}{g + {}^{t_d}/_{\varepsilon_r}} \tag{2.39}$$

This capacitance, C, from (2.39), is substituted in (2.38) which results in the associated electrostatic force,

$$F = -\frac{1}{2}V^2\frac{Sw\varepsilon_0}{\left(g + {}^{t_d}/_{\varepsilon_r}\right)^2} \tag{2.40}$$

This force is distributed uniformly across the bridge and for a system in equilibrium, the restoring mechanical force, F_k, obtained from the stiffness of the bridge, the vertical displacement from a zero bias height, g_0 is given as,

$$F_k = -k(g_0 - g) \quad (2.41),$$

Thus when both forces are equal we obtain,

$$-\frac{1}{2}V^2 \frac{Sw\varepsilon_0}{\left(g+{}^{t_d}/_{\varepsilon_r}\right)^2} = -k(g_0 - g) \quad (2.42),$$

From which, $V,$ is derived as,

$$V = \sqrt{\frac{2k}{Sw\varepsilon_0}\left(g + {}^{t_d}/_{\varepsilon_r}\right)^2 (g_0 - g)} \quad (2.43)$$

The critical point of the curve is an inflection, and thus unstable point for the second derivative of (2.43), which produces a maximum for $g = {}^{2g_0}/_{3}$.

This voltage corresponding to this point is referred to as the pull-in voltage and is given as,

$$V_p = \sqrt{\frac{8k}{27\varepsilon_0 A}\left(g_0 + \frac{t_d}{\varepsilon_r}\right)^3} \quad (2.44)$$

Thus the pull-in voltage is dependent on the air gap, g_0, effective bridge spring constant, $k,$ derived in (2.40), the permittivity of air, ε_0, and thin dielectric, ε_r, and the capacitive area of the bridge, A.

2.1.1.1.3 Frequency and switching time response

The behaviour of the bridge in the frequency domain can be examined during its resonant frequency response when it is subject to an applied force. It is derived from the general equation describing motion in the 1-D mass-spring damp system, with the planar direction in the x-axis for the lumped mass, m, of a uniformly distributed bridge, under the damping factor, b, and spring stiffness, k,

$$F(x,t) = mx'' + bx' + kx \quad (2.45),$$

The frequency domain solution of (2.45) derived from the Laplacian transform, $\mathcal{L}\big(F(x,t)\big)$, is given as,

$$F(s) = kX(s) + b[sX(s) - x[0] + m[s^2X(s) - sx[0] - x'[0] \quad (2.46),$$

By substituting $s = jw,$ and with initial conditions set to zero, (2.45) reduces (2.46) to,

$$\frac{X(jw)}{F(jw)} = \frac{1}{k}.\left[\frac{1}{1+j\frac{w}{w_0}-\left(\frac{w}{w_0}\right)^2}\right] \quad (2.47)$$

Equation (2.47) is the ratio defining describing the average deflection of the beam as a function of an applied force. The resonant frequency for this second order equation is given as,

$$w_0 = \sqrt{\frac{k}{m}} \quad (2.48),$$

k, derived in (2.37) is substituted in (2.48) to obtain the resonant frequency for a uniformly distributed MEMS bridge under zero biaxial stress results in,

$$w_0 = \frac{2t}{l^2}\sqrt{\frac{E}{\rho}} \quad (2.49)$$

The resonant frequency from (2.49) is dependent on the bridge thickness, t, length, l, Young Modulus, E, and bridge density, ρ.

The time taken during actuation to ensure a displacement of the top plate or electrode down to the bottom electrode is called the switching time, whereas the time taken for the electrode from the pulled state to reach its unactuated rest position is called the release time. These parameters can be used as design rules for selecting the performance of a switch for a required turn on and off time response. Thus we proceed by considering the mass-spring damp system equation system for a parallel plate capacitor with x displacement in the vertical direction. The capacitance due to this displacement is given as [44],

$$C = {\varepsilon A}/{(g - x)} \quad (2.50)$$

where ε is the effective permittivity, A is the area of parallel plate capacitance, g is the initial state plate separation distance. For the parallel plate system with applied initial actuation voltage, V, equation (2.45) can be rewritten as,

$$\varepsilon \frac{AV^2}{2(g - x)^2} = mx'' + bx' + kx \quad (2.51)$$

The capacitive switch displacement is thus a function of time, and the following assumptions can be made to obtain a closed form expression for the switching time [44].

1. Due to inertia, the switch moves initially slowly and the damping limits the switching velocity.
2. The gap is relatively large and the gap dependent damping coefficient is constant. The switch spends the majority of the time reaching the halfway point, the final half is travelled rapidly.

Thus the work done, W, by the capacitive actuator in moving from its initial position to location x_a is given by,

$$W = \int_0^{x_a} F(x)dx = \frac{1}{2}V^2\, {dC}/{dx} = \varepsilon \frac{AV^2 x_a}{2(g - x_a)^2 g} \quad (2.52)$$

The inertia limited switch actuation time, t_e, due to work done against the switch mass is obtained with the assumption that both the damping coefficient and the spring constant contributions are negligible. Thus (2.51) when expressed as work done over the distance , x , and with, W, substituted from (2.52), we obtain,

$$\frac{m(x')^2}{2} = \varepsilon \frac{AV^2 x_a}{2(g - x_a)^2 g} \tag{2.53}$$

From (2.53) the system velocity, x' is derived as [44],

$$x' = \sqrt{\frac{\varepsilon}{m} \frac{AV^2 x_a}{(g - x_a)^2 g}} \tag{2.54}$$

Thus,t_e, is derived as [44],

$$\int_0^d \sqrt{\frac{m(d - x_a)^2 d}{\varepsilon AV^2 x_a}} = \frac{\pi}{2V} \sqrt{\frac{d^3}{\varepsilon Am}} \tag{2.55}$$

The switch closing time is limited by another case under the condition where the inertia is negligible, by setting $m = 0$. Thus (2.51) when solved for the velocity can be rewritten as,

$$x' = \frac{1}{b}\left(\varepsilon \frac{AV^2}{2(g - x)^2} - kx\right) \tag{2.56}$$

Thus the damping limited actuation time derived from (2.56) is given as,

$$t_y = \int_0^d \frac{dx}{x'}$$
$$= \int_0^d 2b(d - x)^2 \Big/ \varepsilon AV^2 \left(1 - 2kx(g - x)^2 \Big/ \varepsilon AV^2\right) dx \tag{2.57}$$

which results in [44],

$$t_y = \frac{2bg^3}{315} \frac{5g^6k^2 + 21g^3k\varepsilon AV^2 + 105\varepsilon^2 A^2 V^4}{\varepsilon^3 A^3 V^6} \tag{2.60}$$

Hence with inertial and damping limited switch times, a close approximation of the switch actuation time is given by,

$$t_{close} = t_e + t_y = \frac{\pi}{2V} \sqrt{\frac{g^3}{\varepsilon Am}} + \frac{2bg^3}{315} \frac{5g^6k^2 + 21g^3k\varepsilon AV^2 + 105\varepsilon^2 A^2 V^4}{\varepsilon^3 A^3 V^6} \tag{2.59}$$

Besides the switch closing time, the opening time can be estimated in a similar manner. By ignoring the damping time, the switch release time, t_{pu}, is derived

from the plate distance travel, g, due to the release of energy post actuation. Thus from the principle of conservation of energy, with the total energy at time, t_m, equated to the total energy at the pulled-in condition, we get [44],

$$\frac{mx'^2}{2} = \frac{kg^2}{2} - \frac{kx^2}{2} \tag{2.60}$$

Hence, velocity, x', can be derived from (2.60) as,

$$x' = \sqrt{(kg^2 - kx^2)/m} \tag{2.61}$$

The opening time, t_{pu}, is obtained as [44],

$$t_{pu} = \int_d^0 \frac{dx}{x'} = \frac{\sqrt{\frac{m}{k}}}{\sqrt{(g^2 - x^2)}} dx = \frac{\pi}{2\omega_0} \tag{2.62}$$

Work reported by [45] also indicated another expression for a general switching time, t_s, derived from the 1-D mass spring equation (2.48), by neglecting the inertial terms, and assuming linear damping, b. The switching time, t_s, is independent of the materials mechanical properties, which reduces the first order differential equation to,

$$t_s \approx \frac{2b{g_0}^3}{3\varepsilon_0 AV^2} \tag{2.63}$$

Equation (2.63) is valid for when, V_A, the applied voltage, is $V_A \gg V_P$, the pull-in voltage, V_P [45].

Another parameter related to the damping factor and the bridge resonance frequency is the switch quality factor. The switch quality factor is the ratio of maximum energy stored to dissipated energy per period. From (2.47) the quality factor is given as,

$$Q = \frac{k}{w_0 b} \tag{2.64}$$

For small beam displacements in atmospheric pressure, we can employ the viscous regime classification examined by Newell in [46]. Thus by employing Stokes' law, which describes the viscous drag (friction) effect at the surface of a solid moving with steady velocity in a viscous medium. This viscous drag effect can be related to damping experienced by a mechanical resonator to derive the quality factor, Q, for a MEMS beam in close proximity to the substrate producing a parallel walled duct as [46],

$$Q = \frac{\sqrt{Ep}}{\mu}\left(\frac{t}{wl}\right)^2 g^3 \tag{2.65}$$

Equation (2.65) describes the squeeze film damping model, (SQFD) dependent on, μ, the viscosity coefficient of air, the bridge height above the substrate, g and remains valid for $g < w/3$. The damping factor, b, obtained with (2.64) substituted in (2.65) and is shown be proportional to $1/g^3$.

This conclusion has been found to be in agreement with newer models, Drag force and slide film damping, used to account for the damping in microstructures. The SQFD remains the most dominant model and, describes by virtue of the area between the beam and substrate under actuation, the squeezing of the volume of air in that space, such that massive movement of the trapped fluid, in this case, air motion is resisted by its own viscosity. This friction causes dissipation of energy, towards both electrode and air, which results in the damping of the movable electrode [46]. This damping force dominates at lower frequencies relative to the spring force, whereas the latter dominates at higher frequencies [46].

2.2 Conclusion

In this chapter a brief discussion of the underlying principles governing the operation of MEMS switches was undertaken. The classification and attendant figure of merit that has made MEMS switches the allure in RF applications was examined. The equivalent electro-mechanical model and mathematical definition of the operation of MEMS switches was also reviewed.

The work examined in this chapter has established MEMS switches as a well-defined system of actuators with aim of providing isolation along an RF signal path. The degree of isolation makes for a performance metric and is the ratio of two distinct capacitive states (ON and OFF). A matrix of conditions and the desired response define MEMS switch design and entails reviewed mathematical work in this chapter. The response of a switch comprises this required isolation, switching and frequency time, RF loss, attenuation, actuation requirements which must be factored in the MEMS design to make for a well-described switch.

With the underlying principle described, it is pertinent to explore MEMS fabrication methods employed in realising the devices as embarked upon in chapter three.

Chapter 3
MEMS literature review: Fabrication techniques and methods

MEMS switches consists of moving, rotating, free-standing and vibrating parts, as opposed to solid-state devices, and coupled with their inherent small size, fabrication processes and packaging are specialized and relatively expensive. The general body of microfabrication related techniques developed to realize sensors and silicon on insulator (SOI) transistors, has been adopted as process templates with variations broadly dependent on the design, materials and project goals [47].

In this chapter, the peculiarities that attend conventional clean room fabrication methods are explored, alongside relevant optimization theories. We also examine related work which analyses the performance metric of these established fabrication methods.

3.1 Early fabrication work

Early development of MEMS fabrication techniques can be traced to work embarked by Honeywell Corporation that resulted in a Wheatstone bridge of piezoresistors developed with photolithography techniques on Si, with etching facilitated by Ammonium Fluoride, NH_4F [1]. This process sprung a method of on-wafer beam development that saw the elimination of creep and hysteresis issues with bonding agents previously employed in the beam to wafer transition. Metallic vapour deposition of Gold as a gate electrode for a transistor was also reported in 1967 [36], one of few early records for enhanced deposition techniques. A consensus on MEMS terminologies and the surface machining on Silicon wafers of cantilever beams with widths from $25\ \mu m$ in [48] was heralded in [1,36], as marking the foundation for much of latter-day cleanroom microfabrication techniques.

3.1.1 Substrate classification

Cleanroom microfabrication techniques consist of intricate development cycles, which includes metal and dielectric film depositions, material etching, chemical processes with photolithographic defined routines and masks. Cleanroom-based processes require well-controlled air-circulation, ventilation, and filtering systems with the goal to minimize contaminants that may interfere with the fabrication process.

The first step in the MEMS fabrication process is defining and developing the substrate layer. Silicon-based wafers constitute the largest substrate type

group used in MEMS and are primarily classified as crystalline, polycrystalline or amorphous [2,49].

Single crystal silicon is still the prevalent substrate material employed in MEMS. This is due to its mechanical strength, high resistivity, smoothness, availability of wafers in various standardized shapes, sizes, particle counts, crystal orientation. In addition, most of the cleanroom machinery is co-opted as offshoots of silicon IC microfabrication processes. Silicon wafer sizes are standardized and include in 3 inches, 100 mm to 300 mm diameters. Its use was reported in earlier works [36,45] and in a compendium of recent works in [40,50].

Quartz $(\mathrm{SiO_2})$, finds ready application as MEMS substrate material [16,51] and reportedly employed in [35, 52], on account of the surface smoothness, rigidity, ease of availability, its low thermal conductivity and long-term stability. Being chemically stable, quartz has the least of available etching techniques reported for MEMS structures. Wet etching is by $\mathrm{HF/NH_4F}$, with rates dependent on the crystallographic orientation, while surface micromachining and dry etching are rarely exploited. Majority of quartz substrates employed for cleanroom and wet bench processes are cut along the z-axis, since quartz plates cut along this axis exhibits highest etching rates [49]. Quartz also allows for easy incorporation as the mask base, where an absorber pattern is generated by an e-beam incident on the fused coating of chromium and the quartz crystals. This extended application also ensures its allure for use in MEMS photolithography [49].

Gallium Arsenide, (GaAs), is another popular Si-based substrate with properties described as a merger of both nominal silicon and quartz. It possesses a higher density than silicon and quartz, and this property plays a role in the mechanical response, e.g., resonance and acceleration of the actuator. This is due to its crystal lattice arrangement, which maintains a relatively low noise floor at high frequencies [53]. Although mechanically inferior to silicon and quartz, due to its lower endurance to wear and fatigue, it enjoys the highest variety use for both dry and wet etching processes-especially for non-planar substrates topologies [54,55]. Another factor leading to increasing use of GaAs substrates and hybrids such as GaN/Si and GaN/SiC, employed in high power applications, is the ease of integration of additional wireless communication systems, such as antennas, ultrahigh-speed electronic and photonics, all which are implementable with the same fabrication technology. The technology associated with GaAs substrate is reportedly growing faster than integrated circuit (IC) fabrication technology,

due to the growth of digital cellular phones driving investment and research in this area, and in part, due to the possibility of forming compatible ternary and quaternary compounds with III-V technologies, such as Al_xGa_{1-x}. These compounds are reported as having high efficiencies when employed as solar cells, and in photo electronics at frequencies in excess of 250 GHz [49, 56].

Amorphous silicon-based wafers like glass and alumina are also used as substrates. Glass substrates have been employed as substrates from early studies as noted in [36], and in recent work [57] due to ease of availability, excellent surface smoothness, and good RF response. They also allow for ease of integration to inductors with high Q [58]. It is particularly suited for temperature related MEMS fabrication processes due to its relatively low thermal expansion [59]. Alumina substrates are highly thermal stable, hard, wear and corrosion resistance, with an acceptable thermal conductivity that makes it attractive for use in space-bound electronic and in microwave circuit applications [60].

Additional substrate types including LTCC [60-63] which can be stacked to modular heights in the fabrication process, and printed circuit boards (PCB) [9-13] have opened up possibilities for reduced process cost, integration and packaging with components for specific front-end applications like planar antennas. This packaging is without mismatch and RF loss challenges associated with silicon and GaAs [10]. A tabular comparison of the most popular MEMS substrates is provided by cost and characteristics in Table 3.1.

Table 3.1 Comparison of common MEMS substrates [49, 53, 64, 65].

Property	Si	GaAs	PCB (4350b)	LTCC	Quartz
Dielectric constant	11.9	13.1	3.6	9.8	3.8
Thermal coefficient of expansion ($\times\ 10^{-6}C^{-1}$)	2.35	5.9	16	6	13.7
Thermal conductivity ($W/cm\,^{\circ}C$)	1.57	0.5	0.1	3	0.02
Physical stability	Good	Fair	Good	Good	Fair
Breakdown voltage ($V/\mu m$)	30	40	40	> 40	20 to 40
Loss tangent	0.004	0.0004	0.003	0.005	0.0001
Density (gm/cm^3)	2.3	5.3	1.86	3.1	2.65
Flexural strength (MPa)	100	55	255	210	70
Moisture absorption (%)	0	0	0.06	0	0
Young Modulus (GPa)	190	75	16.8	120	86.8
Cost	Low	High	Low	Low	Low
Bonding to other substrates	Easy	Difficult	Easy	Difficult	Difficult

3.1.2 Substrate films and deposition techniques

Films are deposited, transferred, patterned on substrates to serve as transmission lines, dielectric, sacrificial layers and the MEMS bridge membrane. Elemental materials are deposited on substrates as thin layers or films and patterned as RF transmission line paths. Deposition of thin elemental material films is obtained broadly by physical and chemical means.

3.1.2.1 Physical vapour deposition

Physical vapour deposition (PVD) processes describe sets of methods used to deposit thin solid films through condensation of the vaporized form of the solid material onto the substrate. The basic PVD processes include evaporation, sputtering, and ion plating. The gaseous state of these elements travels from source to destination substrate under controlled environments, and deposition induced as physical films, or from intended chemical reactions of two precursors introduced in the gaseous states. On arrival at the target substrate, film growth is fostered by bombardments of additional atoms in their gaseous phase, with more sputtering and condensation to make for increased film thickness [1,66]. The following physical processes that force source materials into their gaseous states, to make for material deposition are examined in the follow-up subsections.

3.1.2.1.1 Sputtering

This process consists of a fast-moving ion which on hitting the target causes atoms to be ejected by momentum transfer, and the ejected atoms condensed on the substrate to form the surface coating. This physical phenomenon produces a microscopic spray effect, that is directed at the substrate in a vacuum to produce graduated growth of the thin films. DC diode magnetron and RF diode sputtering are mostly employed, to make for this energy transfer to the ion. The distinction being the source power type applied to energize the electrodes of the diode system in the sputtering vacuum chamber [1].

Sputtering allows the deposition of films with the same composition as the source, hence it the preferred process for depositing alloys [1]. Applications of this deposition technique for silicon, glass, quartz, alumina, aluminium nitride substrates have been reported for sputtered conductive layers of Gold, Copper and Aluminium.

3.1.2.1.2 Thermal and electron beam evaporation

In this technique, boiling of the coating material in a vacuum is carried out, with thermal or electron beam sources, and the escaping vapour directed towards the target substrate. This boiling off in the source material is conducted under vacuum conditions, to minimize the interference from impurities in the evaporation, travel and condensation of the coating material on the substrate. The thickness of the film deposited is a function of evaporation rate/flux, and deposition time, and uniformity dependent on the substrate geometry and orientation in the vacuum chamber [1].

Thermal resistive, induction and electron beam sources provide heat to the coating materials in the chamber. Resistive source elements include wire and sheet metal, crucible shaped topologies, with the evaporant in proximity or within the structure for heat transfer. A more efficient RF energy heating system is the induction-heated system with eddy currents coupled directly into the coating material which is subsequently heated up to make for coating of the substrate. With electron beam, a stream of ions is deflected by transverse magnetic field electrons between energized cathode and anodes and focused onto the evaporant surface. This energy focussed stream is used for heating the evaporant. It minimizes the drawback of contamination of the evaporant by resistive element support systems and optimizes energy for excitations of the electrons and heating of the evaporant [1].

3.1.2.1.3 Pulsed laser deposition techniques (PLD)

With Pulsed Laser Deposition (PLD), high power laser beam pulses are used to ablate a small amount of the solid coating material, to produce particulate amounts of ions and molecules, from energy absorbed in the laser to material interaction in vacuum conditions. These particulates are further excited by bursts of the laser beam to produce plumes or hot plasma and are expanded from the source material towards the oppositely positioned substrate, to produce the thin film deposit. It is the preferred method for depositing material with complex stoichiometry. In [49] this method was employed to realise deposits of ferroelectric layers of $\mathrm{LiNbO_3}$ on Si.

3.1.2.1.4 Filtered and unfiltered arc cathodic deposition (FCA)

This process entails the plating of the substrate with the plasma phase of coating material, generated as microexplosions, at the surface of a solid cathode by vacuum arc ion sources. Deposition rates are substantial and excel where film adhesion and density are required. Micro and nanodroplets, containing high energy ions as co-products are created in addition to neutral and ionized atom. The former poses a challenge where film smoothness is

crucial and is eliminated in the filtered cathodic arc deposition method. High energy ions droplet from the ion beam employed for deposition, are filtering from neutral ions, as they are subjected to a travel path in a quarter torus effected with electromagnetic coils serving as ion control. The neutral particle and droplets are not affected by the force exerted and fly right into the torus' walls. Thus leaving only the high energy ions at the exit of the torus and deposited on the substrate [1].

3.1.2.1.5 Ion beam plating

The film to be deposited is bombarded by microsized inert or reactive particles, which results in the controlled growth of the thickness and properties of the resultant coating film. The particulate molecules or atoms can be sourced from vacuum, arc or chemical evaporation precursors. An additional ion beam can be included to make for modification of the growing film's structure and the substrate surface, thus enabling control over thin film coat on impinging the substrate. This ancillary beam system is described as ion assisted ion beam plating and is mostly applied in MEMS filter structures [1].

3.1.2.2 Chemical vapour deposition processes

Chemical vapour deposition (CVD) consists of the reaction or decomposition of one or more volatile precursors to produce the desired film on the substrate. Fundamental steps associated with CVD, leading to film growth consist of reactants in travel from the main gas flow inlet region to the reaction zone, and the production of by-products and precursors. These reactants and products travel to the substrate surface and are chemically or physically absorbed, with reactions proceeding, resulting in the deposit of a film island. This is followed by step-wise growth with continuous reactant gas travel and follow-up reactions. A transport system conveys volatile by-products from the surface and reaction zone back into the main gas flow region making for a cyclic process [1,66]. Basic chemical reaction types exploited to produce films include pyrolysis, reduction and oxidation reactions.

Pyrolysis refers to thermochemical decomposition of volatile reagents to produce films. Reduction and oxidation reactions depend on the electron transfers between reactive agents, to produce associated film products. The former requires a gain of an electron in the oxidative states of the reactants whereas the latter a loss of electrons [1].

Chemical vapour deposition process techniques include, Atmospheric and Low Pressure Chemical Vapour Deposition (APCVD/RPCVD), Plasma-Enhanced Chemical Vapour deposition (PECVD, Atomic layer deposition

(ALD), Laser Induced Chemical Vapour Deposition (LICVD), Metalorganic CVD (MOCVD), Vapour phase epitaxy (VPE), and Rapid thermal CVD (RTCVD) [1].

3.1.2.2.1 Atmospheric and Low-Pressure Chemical Vapour Deposition (APCVD/LPCVD)

As their names suggest, both of these chemical vapour deposition techniques operate at atmospheric (10^5 Pa) or reduced pressures (20 to 85 Pa) in a reactor, with heating provided by induction elements. The film deposition rates and uniformity employed with these methods are dependent on the gas flow conditions in the reactor relative to substrate orientation. With LPCVD, the process temperature is lower and it allows for a tight control of film uniformity and step coverage. Its major drawback is with the deposition rate which is much smaller than APCVD, in the range of 2.5 to 10 $\mathrm{nm/s}$ [1].

3.1.2.2.2 Plasma-Enhanced Chemical Vapour deposition (PECVD)

Plasma enhanced chemical vapour deposition (PECVD) is a variant of the CVD technique. It entails RF, DC or microwave generated plasma particulates and precursors of reacting gases, with their accompanying diffusion and deposition onto the substrate [1]. The process is set up in a vacuum, with a gas supply system, accompanied by separate heating of the substrate by resistive elements to make for elevation to deposition temperatures dependent on the film. Deposition rates in a plasma enhanced process are greater relative to thermal induced processes, due to the smaller activation energies involved [1]. Films deposited with PECVD include Aluminium, Silicon, Alumina, Quartz, Silicon Nitride, Titanium Nitride, Silicon Carbide, and Titanium Carbide [1,49].

3.1.2.2.3 Atomic Layer Deposition (ALD)

Atomic layer deposition (ALD) is a derivative of the chemical vapour phase deposition technique and relies on surface-controlled reactions to create thin-film atomic layers deposited with each pulse of reactant gases. By selecting temperature and flush gas pulse rates, layers are conditioned to function as stable chemisorbed, or as attending physisorbed layers derived from reactant gases species and precursors agents. Thus as opposed to conventional CVD, ALD is based on sequential deposition of monolayers on a substrate surface, alternatively exposed to only one of two complementary precursors supplied one at a time. The deposited material thickness is dependent on the number of cycles. Thermal and plasma ALD are the two main families distinguished by the exposure step makeup. In the former, a reactant exposure step is

Table 3.2 Summary of chemical vapour deposition (CVD) process family [49].

Process	Description	Advantage	Disadvantage	Pressure/Temperature
APCVD	Processes at atmospheric pressure, mass transport controlled.	Simple, high deposition rate	Poorer step coverage, particle contamination	100-10 kPa/250-450 ℃
LPCVD	Processes at sub-atmospheric pressures, surface reaction controlled.	Excellent purity and uniformity. Conformable step and large wafer capacity	High temperature and lower deposition rate	100 Pa/ 550-650 ℃
PECVD	Uses plasma to enhance chemical reaction rates of the precursors. Allows deposition at lower temperatures	Lower substrate temperatures, good adhesion, fast, good step coverage	Chemical and particulate contamination	266-666 Pa/-200 -400 ℃
MOCVD	Based metal organic precursors	Excellent for epi on large surfaces	Safety concerns, expensive source materials	
ALD	Deposits successive layers of different substances to produce layered, crystalline films	Thin conformal films, with thickness control and composition possible at the atomic level	Slow-monolayer fraction is deposited in one cycle	Room temperature (23℃) -400 ℃

utilised, whereas, in the latter, a plasma exposure step is employed. With plasma ALD, depositions are possible at lower temperatures relative to thermal ALD requirements. High-k dielectrics, i.e materials with high dielectric constants, like Al_2O_3, SiO_2, ZnO, TiO_2, are typical materials deposited with this

method [49]. A summary of chemical vapour deposition (CVD) processes explored in this section is presented in Table 3.2.

3.1.2.3 Hybrid physical-chemical deposition processes

Hybrid deposition processes combine both physical and chemical features, co-opting the best attributes from such combinations as [66],

- magnetron and e-beam evaporation
- magnetron sputtering and filtered cathodic arc deposition
- e-beam sputtering and filtered cathodic arc deposition
- polymer flash evaporation and magnetron sputtering/evaporation

Hybrid physical-chemical deposition processes include activated reactive evaporation (ARE) and reactive sputtering.

3.1.2.3.1 Activated Reactive Evaporation (ARE)

Activated reactive evaporation involves the evaporation of a metal or an alloy in the presence of a sustained plasma of a reactive gas, produced by electrode configuration driven by AC or DC which is then directed towards the substrates. Evaporation of metal, alloy or compound can be by electron beam or resistance heated sources. The latter is prohibitive and unsuited for low melting point and high vapour pressure materials. The evaporated metal or compound reacts with the gaseous species in the plasma area and is deposited on the substrate [1,66]. Variants of the basic ARE method include the enhanced ARE with thermionic heating, ARE using plasma electron-beam guns, and the biased activated reactive evaporation (BARE). Materials deposited with this method include Ni, TiC, TiNi, $\mathrm{Al_2O_3}$, $\mathrm{SiO_2}$ and ZnO [1].

3.1.2.3.2 Reactive Sputtering

Reactive Sputter is sputter deposition that entails the use of the partial pressure of a reactive gas which reacts with the sputtered material to form a compound surface coating on a substrate. A key component of reactive sputtering is to have good control of the partial pressures of the reactive gases in the chamber. The introduction of small amounts of N_2 or O_2 in Ar plasma transforms the target surface after the critical partial pressure is reached into a nitride of oxide, with discharge following at set equilibrium point [1,66]. TiNi, Ta_2O_5, ZnO, AlN, TiW:N, and WO_3 are typical material deposited using this method, in reactive atmospheric compositions of Ar/N or Ar/O_2 [1].

Delineations of reactive sputtering are in terms of power supply methods, DC and RF, with DC reactive magnetron sputtering accounting for the most prevalent with substrates, due to high deposition rates and comparatively

lower cost. Challenges with control and process stability undercut the aforementioned advantages, one of such is target poisoning due to the partial pressure required to form insulating films and process shift. It derives from the build-up of insulating materials in the vacuum system, driving the electrical resistance plasma to the return path up, with higher power supply demands. These issues are overcome with a dual rotary magnetron system, in which the target is rotated in a stationary magnetic assembly, and the sputtering plasma is supported by arched magnetic fields causing the target material to be deposited on the substrate [1].

3.1.2.4 Liquid phase deposition processes

Liquid phase deposition techniques refer to methods unrelated to physic-chemical means, in which the coating liquid is used to obtain a uniform, adherent, defect-free film over the entire substrate. Liquid phase deposition methods include spray-coating, spin-coating, and dip-coating.

3.1.2.4.1 Spin coating

Spin coating is used to apply uniform coatings to flat substrates or wafers. The material to be deposited is applied in rationed amounts relative to substrate size and rotated in two step-wise speeds consisting of a dispensing step and a high thinning speed [49]. The dispensing speed enables the spread of the coating fluid over the substrate, after which the fluid and substrate are ramped up to higher speeds to thin the fluid near it's desired thickness by centrifugal forces. Typical dispensing speeds are 500 rpm, and finally ramped speeds, 1500-6000 rpm. The centrifugal force ensures a flow to the edges of the fluidic solution, where it is expelled after build up, with solvents evaporating simultaneously due to volatility [66].

Spin coating is employed to create thin films including mesoporous oxides of TiO_2 with thicknesses up to 5 nm, and is by far the widely used in photolithography to deposit layers of photoresist from 1 μm thickness [49]. The resulting thickness, T, is a function of spin speed, solution concentration, and molecular weight (intrinsic viscosity), and is given as [1,49],

$$T = {KC^{\beta}\eta^{\gamma}}/{\omega^{\alpha}} \tag{3.1}$$

where K is the overall calibration constant, C is the polymer concentration in g/100 mL, η is the intrinsic viscosity, and ω is the number of rotations per minute. Exponential factors α, β, and γ are determined from curve fitting, from which a coating thickness can be predicted for various speeds and other given parameters. An approximation can be inferred if all other factors are invariable

for a given resist/resin, such that the resulting coat thickness, T, as inversely proportional to the ω^{α}.

3.1.2.4.2 Spray coating

As opposed to spin coating, the spray coating process consists of an aerosol form of the coating material being sprayed on slowly rotating substrates, thus minimizing the influence of centrifugal forces. Spin speeds are usually 30-60 rpm, allowing for coverage in substrate and MEMS cavities [1]. This process can be automated and ideal for side-wall coverage of high aspect ratio MEMS structures. It does not suffer from thickness variations on account of droplets staying where deposited. It is mostly applied to deposit a conformal photoresist layer even over non-uniform surfaces, thus lending it forward for use in MEMS. However, control over the film thickness is imprecise, relative to deposits obtained through spin coating. In addition, it is marked by a relatively higher accompanying waste of the coating material and is rarely employed to deposit resists thicker than 20 μm [49]. A variant of spray coating called electrodeposition (ED), is described by a process in which the coating droplets are given static charges on the application of a large potential in the air or nitrogen pressure chamber. The charged droplets follow electric flux lines and overspray is minimized, due to confinement to the desired coating area.

2.2.2.4.3 Dip coating

In dip coating, the substrate is submerged in the coating solution and then withdrawn at a controlled velocity, leaving a thin film coat on the substrate after evaporation of the solvent, and mild baking [1]. It is most suited for depositing double sided resists on odd-sized substrates, with the desired thickness dependent on the withdrawal rate, viscosity, and fluid contents makeup. It is unsuited for thicknesses greater than 10 μm and does not ensure control in thickness uniformity. It is a relatively inexpensive coating method and can be executed without clean environments [1,49]. A comparison of the liquid phase deposition techniques is indicated in Table 3.3.

Table 3.3 Summary of liquid phase deposition techniques [49].

	Spin Coating	**Spray Coating**	**Dip coating**
Process	Simple Difficult to automate	Simple Batch production friendly	Simple Batch production friendly
Surface materials	Insulating or conductive	Insulating or conductive	Insulating or conductive
Parameters	Viscosity Spin speed	Spray pressure Scanning speed Solid content of solution Dispensed volume	Fluid viscosity and density Withdrawal speed Surface tension Solid content of solution
Layer uniformity	Difficult to control Poor reproducibility Dependent on the position of cavities in wafer	Controllable Reproducible Independent on position of cavities	Difficult to control Ease of reproducibility Suited for odd shaped cavities

3.1.2.5 Electrolytic and electroless chemical reaction deposition processes

Electrolytic and electroless chemical reaction deposition processes consist of the deposition of materials in a conductive media through electron transfer or exchange. They include electrolytic deposition and electroless plating techniques.

3.1.2.5.1 Electrolytic deposition

Electrochemical deposition processes entail coating by electrolysis of an electrically conductive object submerged in an electrolyte. This system comprising coating material, electrolyte, and target material constitute the electrochemical cell. The passage of electric current in the electrolyte brings about changes in the oxidation states of the materials immersed, by electron transfer [1]. The fundamental relationships governing electrochemical deposition is expressed by two Faraday laws, stated as follows:

1) The mass, m, of the material deposited or liberated at an electrode is directly proportional to the quantity of electricity or charge, Q, passed in the cell.
2) The masses of different substances liberated by a given amount of electricity is proportional to the chemical equivalent weights.

This relationship is summarized by (3.2) [1],

$$m = {QM}/{Fz} \qquad (3.2),$$

where m is the mass of liberated material in grams, Q is the electric charge in Coulombs, M is the molar mass of the material deposited, z is the valence change of the deposited material (number of electrons transferred per ion).

Deposition is initiated with an external electrical source applied to the electrolytic cell to overcome an electromotive force, with the liberation of the coating material occurring at the positive terminal, anode, and a thin film growth taking place at the negative terminal, cathode. This deposition process is most suited to metallic or seeded portions of the MEMS device, as conductivity is required. Materials and their alloys capable of being deposited to include, Cu, Au, Ni, Co, As, Sb, Cu/Zn, Cu/Sn, Ni/Fe, Sn/Ni, NiCo, and NiFe [1].

3.1.2.5.2 Electroless Plating

With electroless plating, electrons participating in the reaction are provided by a chemical reducing agent, as opposed to electrochemical deposition with

depends on an external current source [66]. A sustainable oxidation-reduction reaction ensues when the electrons in the metal to be deposited are supplied in the bath, effectively acting as the reducing agent, alongside the target MEMS substrate or device region. The base metal donates electrons to the metal being plated, becomes oxidized goes into the cell solution, and gets deposited in molecular amounts until the whole substrate is covered or there is none of the base metal. Materials coated using this method include Ni, NiB, Cu, and CoP [49].

3.1.3 Pattern generation: etching and photolithography techniques

Pattern transfer on MEMS substrates and members can be by subtractive or additive means. Subtractive techniques include etching and lithography processes, whereas additive techniques consist of deposition processes discussed in 2.2.2 alongside masks defining design or target regions.

3.1.3.1 Etching

Etching describes the controlled removal of defined portions of the substrate and thin films at the surface or a preferred material layer in a particular manner so that the desired shape pattern or shape is obtained [67]. The region not intended to be removed is protected by a mask, typically made of photoresists or another material resistant to the etching agent.

Etching of solid surfaces can be by wet processes, dry processes, or by mechanical processes. Wet etching can be chemical and initiated by a liquid etchant, or electrochemical by an electrolyte impressed by electric current. Dry etching processes can be physical, where the target surface material is bombarded by ions; or chemical, which may involve plasma enhanced material removal through dissociation of the etchant's volatile chemical species; or by vapour, where is it described as vapour phase etching. Physical-chemical processes combine bombardment of the surface by ions with dissociated chemical species, while mechanical processes entail the use of powder blasting in conjunction with cluster beam technologies [1].

Another criterion of classification describes the etching direction and the resultant profile. Thus the etching direction can be isotropic, where it is even in all directions; anisotropic, where is follows the crystal directions of single crystal materials; directional, where the feature is a preferred direction.

3.1.3.1.1 Wet-chemical etching

Wet chemical etching processes include immersion or dip etching, spray etching, and electrochemical etching.

With immersion etching, the masked or unmasked substrate is exposed to an etchant by immersion in an etch bath. It may be diffusion limited or reaction limited, with the former ascribed to the degree of displacement of the etchants to target surface and the latter where the etch reaction dominated the etching time. Immersion is often accompanied by agitation, to make for the supply of the spent solution with a fresh one at the target surface, thus enhancing uniformity, improved process control, and the prevention of localized heat in the case of exothermal reactions.

In spay etching, the etchant is applied in aerosol forms, as opposed to an immersion bath. It makes for more faster and uniform spread, due to a continuous supply of fresh etchant to the target region [1]. While in electrochemical etching, a redox reaction converts the material to be etched to a soluble higher oxidation state.

Common materials employed in MEMS microfabrication processes and matching etchants are as indicated in Table 3.4.

Table 3.4 Common etchants and materials [68].

Etchant	Target material	Remarks
KOH solutions	Si/ SiO_2	For patterning recessed and planar Si structures, and for anisotropic etching of bulk crystals.
TMAH	Si/ SiO_2	For alkali-free Si etching, with CVD SiO_2 mask.
HF solutions	Ti /SiO_2/Si_3N_4/Al_2O_3/TiO_2/ PSG	For general etching, and polishing.
EDP	Si/ SiO_2	For shaping Si films
NaOH	AlN/ GaN	General etching
H_2SO_4	TiO_2	-
BHF	Al_2O_3/ PSG	-
$4H_3PO_4$, $4CH_3COOH$, HNO_3	Al	Polishing etch
$2FeCl_3$, $HCl/20CH_3COOH$, $HClO_4$	Cr	Good for plated Cr; photoresist mask can be used.
$3HCl$, HNO_3	Au	-
$9NaOH$, H_2O_2	Ta	
$FeCl_3$	Cu/ Ni/ Pb	Use dilute solutions for slower etching of Cu.
H_3PO_4	Al_2O_3/ TiO_2	-
$8H_2O_2$, $7HCl$, $1HNO_3$	Pt	-
$Fe(NO_3)_3$	Ag	Photoresist mask can be used.
$9H_2O$,1 HF	Ti	Photoresist mask can be used.

3.1.3.1.2 Dry etching

Dry etching refers to a family of methods by which the target surface is etched without wet chemicals or rinsing, with physical etching techniques consisting of gas or vapour phase ion bombardment, or chemically by a chemical reaction through a reactive species at the surface, or by combined physical and chemical mechanisms or reactive ion etching (RIE) [49]. The creation of plasma is a key ingredient of dry etching, with additional classification based on setup, which can be either through glow discharge from the diode setup for ion-beam etching, or alternatively from a triode configuration setup.

In physical etching, the etching occurs as a consequence of a physical effect; as in IBE, where there is momentum transfer between inert energetic Ar+ ions

and the target surface. It can also be sputter/ion etching, where a reversal of the connections with regular sputtering accomplishes removal of H_2O films, and adsorbates, and for surface cleaning [1].

Whereas in chemical dry etching, neutral chemical species diffuse to the target sold surface, where they react to form volatile products with the layer to be removed. Gaseous species like F and Cl can be excited by plasma, in which case it is referred to as plasma etching; and as vapour phase etching, where HF and XeF_2 are employed as etchant gases without the need for plasma excitation, notably in etching sacrificial layers [1,49].

In the case of physical-chemical etching, a combination of physical and chemical attack on the bonds of the atoms make for stronger and faster etching results. Variations of this technique include the reactive ion etching (RIE) and the deep reactive ion etching (DRIE), where impacting ions travelling in line of sight damage the target surface, inducing highly anisotropic chemical reactions of the surface with plasma neutrals, or where a passivating layer is cleared by the ion bombardment, thus clearing only horizontal surfaces. The latter is makes for deep channel and sidewall etching of silicon, by employing F plasmas and sidewall passivation to enhance directionality [49].

Cheaper alternatives to both wet and dry etching techniques for macroscopic application include like powder blasting derived from the dated sandblasting technique, in which the abrasive material is a fine grid of glass., can be employed in creating cavities lower than 100 µm for MEMS applications [49].

3.1.3.2 Photolithography

Lithography process refers to a family of techniques used to transfer a pattern onto the surface of a thin film material or solid material such as a wafer. The transfer of microscopic patterns in any one routine lends the use of lithographic techniques to batch fabrication and packaging of multiple micro-sized devices on fitting substrates or wafers. The number of fabrication steps, materials, and device size dictated by the process sequence allows for a delineation of the lithographic technique [1].

Lithographic processes employed in MEMS fabrication processes include electron and ion beam lithography, X-ray lithography and Optical photolithography. In electron and ion beam lithography, a broad beam projects on a patterned mask, consisting of thick areas (blocking) and thin (transparent) areas. X-ray lithography employs x-ray sources illuminating derived from synchrotron radiation rings and laser plasma masks, patterned

into blocking and thin areas. The exposure field is large is insensitive to small particles, but encumbered by enormous starting costs. Optical photolithography or photolithography consists of the application of UV light through a mask onto a photoresist to create patterned structures and is the most commonly employed form. As opposed to other lithography techniques, photolithography: uses photons to induce chemical reactions in photoresists; entails the use of transmission photomasks; has the potential for image reduction with the use of projection optics. The last two components distinguish optical photolithography from X-ray lithography, and an advanced optical lithography process called extreme ultraviolet lithography, which employs light spectrum between deep ultraviolet (DUV) light and X-ray.

A photoresist is a light-sensitive polymer which undergoes a differential change in property on exposure to UV light. The change in solubility of the resist material in a suitable medium on exposure to UV is the most predominant property explored. Photoresists are broadly classified as positive or negative, with negative resists losing their solubility in a developer on post-exposure to UV light, as opposed to positive photoresists [69].

The mask creating the pattern is typically a UV transparent flat plate, made of quartz or glass, with an absorber pattern on one side that is opaque to UV light [49]. Masks classifications include delineation based on exposure-response, and they can be a positive (dark field) or negative (clear field), and the degree of contact; physical and soft contact masks. E-beam lithography is used to generate the mask absorber pattern, due to flexibility with the design write process, while also having higher resolution than photolithography. The pattern is drawn with computer-aided systems and then exposed to the mask [1].

3.1.3.2.1 Photolithography Process Sequence

An overview of the photolithography fabrication process is as indicated in Fig. 3.1. The process is executed under yellow light to avoid unintended photoresist exposure to ambient light, and in clean room conditions to minimize the presence of contaminants which may interfere with the pattern transfer process. Further discussion of these process steps would follow in the accompanying sections.

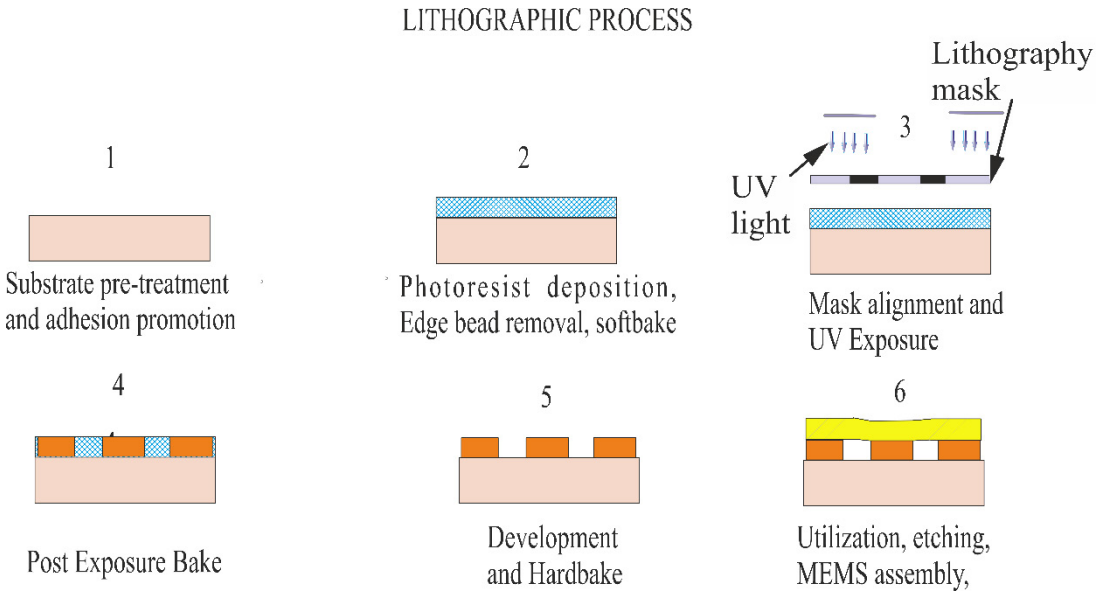

Figure 3.1 Typical MEMS photolithographic process

3.1.3.2.1. 1. Substrate preparation-cleaning and adhesion promotion

As indicated in the preceding section, patterns are created in with resists coated on wafers. These resists do not stick properly to untreated surfaces and it is required that wafer surfaces are treatment precede resist coating. The adhesion promotion process consists of wafer or substrate cleaning, often with solvents or in some case aggressive etchants. Isopropyl alcohol (IPA) and Methyl Chloride, CH_3Cl, are established solvents employed for removing grease, dust and other particulates that may cause adhesion issues and errors in the pattern transfer. Adhesion promotion agents like hexamethyldisilazane (HDMS), $[(CH_3)_3Si]_2NH$ can be employed in both liquid and vapour priming techniques to improve adhesion. In the former, it is applied during the resist coating process as an additive in propylene glycol methyl ether acetate (PGMEA), while in the latter the agent is applied alongside the substrate during exposure in a vacuum [1]. HDMS forms a film on the surface to which water does not adhere, while also preventing the developer from weakening the resist during the development step.

Adhesion promotion is also enhanced by substrate dehydration under vacuum conditions, by heating the substrate to temperatures up to 200 ℃, as resists, which are typically hydrophobic, when developed with trapped moisture on the wafer surface interface would result in poor adherence [1].

3.1.3.2.1. 2. Resist application

Resists are commonly deposited on wafers by spin coating. The wafer is coated with resists first applied in small volumes with an applicator and

dispensed with speeds of about 500 rpm, causing the spread of the fluid over the substrate and then spun at high rates, up to 6000 rpm, flinging off resist excess by centrifugal forces to the substrate edge, down to the desired film thickness consistent with spin speed and time excursion curve [69]. The rate of thinning caused by the centrifugal force is reduced by the degree of viscosity which also derives from the attractive molecular forces. Thus a resist with higher viscosity would produce thicker film layers for the same routine and chemical platform, than those of lower viscosity. When coating thick resists, beads formed from flung resists due to centrifugal forces, at the substrate may cause undesired proximity gap and stickiness between the mask and substrate. These beads are removed by rotating the substrate on the coater at low speeds and applying a solvent or by selective exposure of the bead region [1,69]. The spin coat process produces good homogeneity of the resist thickness over a short process period with an optimized routine. This is not without the drawback of poor material utilization with some waste in spurn resists [1].

3.1.3.2.1. 3. Softbake (Prebake)

After the coating of the wafer by the resist, the density is often insufficient to support additional processing due to the solvent present, and the resist may still be subject to built-in stress. A softbake is used to densify the resist film, drive off the residual solvent, to make for annealing of potential film stress regions. This step also improves adhesion of the resist to the wafer and minimizes stickiness issues at the mask to coat interface.

Typical soft bake temperatures are between 90 ℃ to 100 ℃, in convection ovens or hotplates. The latter provides best temperature control and is the mainstay for leading-edge processing, while the former is more suited for thick resists (5-100 µm) range, allowing for solvent evolution from the depth of the resist film. Thicker resists subjected to inadequate softbake result in pitting in the resist profile, due to non-removal of the solvents or insufficient time to percolate through the polymer matrix. It is also imperative that cooling of the wafer post soft bake occurs in a controlled way with a transfer to a chill plate [1,69].

3.1.3.2.1. 4. Alignment and Exposure

MEMS devices are fabricated by a series of patterned layers atop each other. Each new pattern must be properly aligned and proper overlay to the preceding layout or circuit pattern already on the wafer. Alignment is required between the mask bearing these patterns and the substrate for as many

deposited layers and exposure cycles, with markers on both substrate and mask. Markers often employed include vernier marks for rotational alignment, grating markers and additional reticles for fiducials so accurate placement of the layers relative to the preceding can be conducted.

After alignment is completed, exposure of the resist to UV light proceeds. The commonly used light source is a high-pressure mercury (Hg) vapour lamp and wavelengths to which the resists are reactive to include 435 nm (G-line), 410 nm (H-line), and 365 nm (I-line). The UV dose or incident energy ($\mathrm{J/cm^2}$) across the surface of the resist film is given as a function of the incident light intensity ($\mathrm{W/cm^2}$) multiplied by the exposure time (s) [1]. Photochemical reactions result in a change in solubility of the resist after exposure to the UV light, thus allowing transfer of selective imaging with patterns of the circuit created in the overlying mask to the resist film.

3.1.3.2.1. 5. Post-exposure Bake (PEB)

Light distribution during exposure within the depth of the photoresist varies rapidly due contributions from the incident and reflected components of the light, giving rise to varying rapidly intensities in the vertical direction, and of varied light energy coupled to the resist the film stack. This results in a phenomenon called standing wave light wavefront, with alternating levels of resist with high and low exposure, and a degradation of the lithographic performance.

After exposure, the concentration of the photoactive compound or photoacid generator in chemically amplified resists varies in direct proportion to the light energy after exposure. Where these photoactive compounds/photoacid generators are not bonded to the resin, thus free moieties, diffusion from high to low-density regions in the resin may be induced by baking the wafer after exposure.

It is thus desirable to bake the wafer as an additional step, allowing for a furtherance of chemical amplification reactions induced by the photoactive compound or photoacid generator in the resin, which in turn reduces the effects of standing wave in the resin, while also making for mechanical relaxation of thicker resists [69].

3.1.3.2.1. 6. Development

Exposed patterns are converted into three dimension relief images with the dissolution of unpolymerized resists in a developing agent. Development can be through two main techniques, wet or dry development [49].

In wet development techniques, immersion, spray and puddle developments methods are used. With immersion methods, the wafer is soaked in a bath containing the developer and agitated at a specific temperature. Whereas in spray development, fan-type sprayers or nozzles deploy fresh developing solutions across the wafer surface spun at moderate speeds. A derived method called the puddling process dispenses 100 to 200 cc of the developer on the wafer forming a puddle that covers the surface. It is left for a defined period of time, typically 30 to 75 s, before being spun off [69]. This method is the most commonly employed process as it allows for better process control with the continuous use of fresh developers on the wafer surface, as well as better time and temperature control. Developers are matched to a type of photoresist and may be interchangeable in some cases. Negative photoresists are developed in organic solutions, for example, PGMEA, while positive resists are typically developed in alkaline solutions like NaOH. Rinsing with deionized water typically follows to complete the wet development procedure [1, 49].

On the other hand, dry development techniques are based on vapour phase or plasma-based processes. Dry development techniques are seen as emerging replacement technologies of wet techniques owing to precise line-width resolutions that are realizable. In plasma-based processes, oxygen reactive ion etching is used to develop the pattern or image in the film. Thus the visible pattern formed during exposure evinces a differential etch rate to the reactive ion as opposed to solubility to a solvent [49].

3.1.3.2.1. 7. Hardbake

After development, it is desirable to bake the wafers before the photomask is ready to use in a process called hardbake. As with softbake, the process tool is either hotplate or convection oven, This bake serves to drive off volatile organic, low-molecular-weight materials, and water that might otherwise outgas or undermine the integrity of post lithographic processing equipment. This baking process also serves to anneal the film thus promoting adhesion, and the required temperature is often above the decomposition temperature of the photoresist key components, including the photoactive compound or photoacid generators. Consequently, it is one of the last steps in the lithography process [69].

After hardbake, the patterned resist is ready for use in applications ranging from etching to additional layer and MEMS assembly. Solvents including acetone are often employed to strip resists from the wafer where required, alternatively an O2 plasma etch may be applied for resist ashing [1].

3.1.3.2.2 Performance and figure of merit

A given lithographic process must be consistent and reproducible in order to be appropriate for use in production, regardless of varied resist pattern sizes and shape requirements which may differ from one technology to another. The performance of a photolithographic process is described in terms of the resolution; depth of focus (DOF) and minimum feature size transferable with high accuracy; the overlay and registration, which describes the degree of alignment with patterns from successive masks; and the cost of ownership, which is an estimate of all costs associated with a piece of equipment, and is often employed to compare different combinations of fixed and running costs [2,70].

3.1.3.2.2. 1. Resolution and depth of focus

Resolution is the minimum printable feature size. It is determined by the ratio of the product of the wavelength and the resolution scaling factor,k_1, to the numerical aperture, and can be expressed as [69],

$$k_1 \frac{\lambda}{NA} \tag{3.3}$$

where k_1 is the scaling factor ratio relative to a given process. Given the physics of light travel and the relationship between the refractive index, of the intervening medium, typically air (n≈ 1), the theoretical limit of NA in air is 1. The expression derived is an extension of the Rayleigh criterion, for k_1 with values greater than 0.61. Resolution enhancement techniques include: phase-shifting masks, in which optical proximity corrections play an integral part and is implemented as part of mask generation; immersion lithography which employs a stand-in medium such as water with a higher refractive index; and double patterning, which doubles the number of nominal process steps required to generate a layer of a circuit. The use of these techniques to extend the resolution limits comes with the added cost needed for lens refinement, exposure tools and masks [69].

As with geometrical optics, the object is imaged by an optical system consisting of a lens and light source, to a point in the focal plane, and a broadening outside this point. Generally, an amount of broadening is acceptable, for a range of separation distance values, referred to as the depth of focus. The depth of focus (DOF) in optical lithography is the range of lens-wafer distances over which impressed resist line widths patterns and profiles are within specifications and adequate. There is a trade-off between resolution and depth of focus, as lenses have decreased depths of focus with higher values of numerical aperture. The light source intensity should not drop by

more than 20 % for a given lithography system, and when this criterion is met, the depth of focus for such a system also called the Rayleigh depth of focus. It is given as [69],

$$\pm 0.5\,{}^{\lambda}/_{(NA)^2} \tag{3.4}$$

3.1.3.2.2. Registration and overlay

Registration and overlay deviations are associated with errors in a MEMS alignment system. Overlay refers to the lateral positioning between layers comprising integrated circuits, while registration is the measured error distance of a defined point on the wafer or layer outlay [69].

In typical alignment systems, alignment marks are placed on the wafer and may also be inscribed in exposure fields. Alignment marks include scribe lines, reticles, or crosshairs. The relationship between the positions of these alignment marks and dies is established in the design. Thus it is imperative a knowledge of their locations on the wafer coupled with design data are employed in the mechanical alignment of MEMS device or wafer. Misalignment can occur due to poor optics in the alignment system, often from defocus as wafer and lens distance changes. In addition, a misregistration of alignment reticles in the layer and stage assembly can produce overlay errors. Overlay errors are broadly classified into two intra-field and inter-field. The former refers to the variation of overlay errors within exposure fields, while the latter refers to errors from exposure fields across wafers. Imprecision in an alignment system can induce residual errors that contribute to increased deviations [69].

In addressing overlay challenges, the key objective is to place the wafer under projection optics, such that new exposures overlay pre-existing ones. Locating points on the wafer can be accomplished by the stepper's alignment system. The system consists of specially designs structures called alignment marks or targets placed on a wafer. Their positions are specified in the coordinate system of the wafer, and the steppers alignment system designed to recognize the alignment targets optically and their locations on the stage. In addition, positioning the wafer with identifications of the wafer's centre, edges, notch or flat as mechanical references also lead to improved alignment [69].

Substantial increases in the number of wafer alignments and overlay measurements can help minimize the non-linear overlay errors. This is not without increased metrology costs and reduced throughput. Managing these costs may require applying large corrections obtained from measurements and alignment sites on a single wafer onto other wafers with fewer alignments.

A step and scan systems to correct for translation, rotational shifts between layers and reticles, can also help reduce misregistration issues [69].

The quality of overlay is thus dependent on the ability of the alignment system to acquire alignment targets accurately. An interplay between the alignment signal and the nature of the alignment targets depends on the overall process for fabricating the MEMS device, including film depositions, resist coating, etching and polishing techniques. This then requires a mechanism that promotes an optimization of targets at each fabrication stage [69].

3.1.3.2.2. 3. Process cost metrics

To meet consumer demands, it is imperative that lithography is cost-effective while also providing the desired technical output. Lithography costs components include consumables and capital equipment acquisitions with future term plan disposals costs, throughput, utilization, rework, yield, labour, metrology, and maintenance An assessment of these in a given lithography process is important for modelling the cost of ownership. The cost of lithography can be measured by scaling the wafer cost of ownership appropriately. This can be in terms of the cost per wafer, cost per chip or cost per unit function. Cost of ownership analysis is oriented towards a given time period for a constant wafer size, and the most commonly employed metric is the cost per wafer. This metric is in turn dependent on the equipment throughput. An expression for measuring the capital cost per wafer exposed is given as [69],

$$C_{ED}/T_P U \tag{3.5}$$

where C_{ED}, is the capital depreciation per hour, U is the fractional equipment utilization, and T_P is the raw throughout of the lithographic system (wafer aligned and exposed per hour).

The throughput mathematical model for a step and repeat exposure system given in [69] is expressed as,

$$\text{Throughput (s)} = 3600/\left(t_{OH} + N\left(t_{exp} + t_{step}\right)\right) \tag{3.6}$$

where, t_{exp} is the exposure time per field, t_{step} is the time for the die to die alignment, t_{OH} is the time required to remove the wafer from the chuck, replace and align with a new wafer, N is the number of exposure fields per wafer.

The exposure time per field is given as the ratio of the resist intensity to light intensity, thus allowing for throughput improvement with variations in light

intensity, and the use of chemically amplified resists. However, there are practical limits to how short the exposure time can be, due to doe control problems for short exposure times and field scan speeds. A fine line is sought with an optimized dose period for a lithographic process. Additional improvements in the throughput can be obtained in the stage design with control systems and techniques that result in the automated handling of wafer placements and alignments.

Productivity is enhanced through the maximum of the equipment. Equipment downtime and setup time detract from the output and is related to the utilization factor. Downtime is attributable to tools not being in functional states, due to unscheduled breakdowns and associated repairs, and planned or scheduled maintenance work for cleaning of the resist processing equipment, UV lamp changes, laser lens replacement etc. Another impediment to productivity is standby time when no operators are available, time spent waiting for ancillary production tests, and time during which no product is available. To the extent that these times are not spent with wafer processing or device fabrication, is valuable machine productivity lost. It is often required that productivity is maximized with production organization and planning.

3.1.3.2.3 Yield

During the manufacture of MEMS and submicron integrated circuits, processing steps can result in material parameter perturbations. These variations result in deviations in circuit metrics like performance and power. It is thus imperative to characterize the fabrication process for compliance with device design response and project forecast. This characterization is often in the form of yields, which is often employed interchangeably with productivity. The lithographic process yield can be calculated and obtained at different points and with different results. For instance, fabrication yields take into account the number of wafers completing the process, as a function of wafers deployed from start, or the lithographic process with a number of line widths meeting specification relative to rendered patterns. Typical fabrication and lithographic yields are 92 %, to 99 %. A general description of yield (Y) describes the fraction of devices that are functional at the end of the fabrication process. It can be expressed as the ratio of good outcomes to the total lot [2],

$$\mathrm{Y} = {}^{\text{Good outcomes}}/_{\text{Total}} \tag{3.7}$$

Thus a steep yield ramp implies a quicker path to high batch yield per unit volume. Yield loss results from, parameters that are improperly specified or

out of specifications, equipment or process failures, device defects, and chemical contaminations, among other factors. The number of defects is non-negative, and distributions are frequently classed as random and non-random. These distributions follow an exponential function in the former, log-normal, normal functions in latter, especially in lithographic processes for defects characterized by scratches per lot size [71].

Yield can also be defined in terms of loss mechanisms as a result of defects in outcomes, thus processes with lots of steps tend towards lower yields. Hence the yield (Y) of a fabrication process can be described as [2],

$$Y = \Pi_{i=1}^{m} Y_i \tag{3.8}$$

for, the ith step of a manufacturing process with the accompanying yield, Y_i. Each stage yield quantities are fractions between zero and one.

Defects can be from randomly distributed faults like particle contamination or systematic contribution due to predictable sources like a photoresist pattern collapse. For example with lithographic processes, defects are caused almost exclusively by resist processes which include coating, and development steps, although particulates impurities from broken or unclean tools do occasionally crop up. In lithographic processes, the absence of defects and by implication high yields is defined by a near infinite electrical resistance between deposited dielectric films and conductive surfaces [71]. Yield loss resulting in fewer good outcomes can also be from catastrophic failures or from parametric failures. In the former, a missing material particle or defect are primary causes of failures, whereas, in the latter, the device while functionally correct but however fails to meet performance criteria [72].

3.1.3.2.3. 1. Models for yield analysis

Yield models describe the relationship between measured defect densities to product yield, to make for lot and tool output prediction and improvements. Yield prediction entails modelling of physical and statistical phenomena and can be distilled into the analysis of parametric yield analysis and random defect modelling and critical area computation [71, 72]. A MEMS fabrication process with m stages is most described by separate suiting models, and can be challenging in some cases. For example, predicting the parametric yield of a lithographic process is varied as it is difficult, and is rarely attempted. Yield estimation components for making decisions lack an accurate method for the lithographic step, and are often described by the cost of ownership modelling methods with assumptions of a near constant value estimate of 97 % for lots with reproducible pattern line widths and overlays [73].

Parametric yield analysis entails the use of statistical timing analysis methods to predict failures, power limited yields, and minimize the systemic component of process variations. It is thus used to measure the quality of functioning systems. A common method used to measure parametric yield is Monte Carlo based simulation routine which forms the basis of simulation tools like PROLITH™ and TEMPTATION™ (Temperature Simulation) used in optimizing a lithographic process [74], and VLSI Layout Simulator for Integrated Circuits (VLASIC™) used to model local effects. Another powerful simulation tool used in evaluating parametric yield called FABRication of Integrated Circuits Simulator (FABRICS™) can be used to model global effects. Spatial and logical correlations play important roles in statistical timing analysis [72, 75].

Models employed to predict the yield of a lithographic process from fabrication random defects are based on a measure of the critical area of the device. This area indicates the degree of the sensitivity of the design to random defects in the fabrication process. Models used to compute random defect yield include Seed's, the negative binomial, the Poisson, and Murphy's model. Distinctions between these models are in the choice of statistics assumed to govern the spatial distribution of lot defects [75].

The Poisson yield model is the simplest model and is valid for a small number of devices and defects. It requires that each defect results in a fault and that defects are considered as perfect points that are spatially uncorrelated and uniformly distributed across the wafer [2, 75]. It is given as [75],

$$Y = e^{(-dA_c)} \tag{3.9}$$

where d is represents the average number of defects per unit area, and A_c is the defined critical area.

A more general model called the negative binomial model employs negative binomial statistics and is based on the gamma density function resulting in the equation yield model for a single step as and critical area, A_c [72],

$$Y = \left(1 + {dA_c}/{\alpha}\right)^{-\alpha} \tag{3.10}$$

$$A_c = \int_0^{\infty} A(r)\, D(r) dr \tag{3.11}$$

where α is the clustering parameter which increases with decreasing variance in the distribution of defect, $A(r)$ is the area where the centre of a defect of radius r must fall in order to cause circuit failure, and $\mathrm{D(r)}$ is the density function of the defect size. It is seen that for the cluster parameter, $\alpha = \infty$,

(high amounts) the negative binomial model approaches the Poisson yield model.

The Seeds model can be derived from the negative binomial model and corresponds to clustering parameter $\alpha = 1$ (low) based on the theory high yields are caused by population sizes with low defect densities and a small proportion of high defect densities. Which implies that the probability of measuring a low defect density is markedly higher than that of observing a high defect density [75]. It is given as [2],

$$Y = (1 + dA_c)^{-1} \tag{3.12}$$

Murphy's model proposes a nonconstant defect density and asserting alongside that this density is summed over all devices and substrates using the Gaussian distribution of defects. A closed form approximation using a triangular probability distribution function is given as [75],

$$Y = \left(1 - e^{-dA_c}/_{dA_c}\right)^2 \tag{3.13}$$

It is the most widely used model in the industry for determining the effect of manufacturing process defect density. However, it is not uncommon to implement either of these yield formulas for each turn of the fabrication process. Ultimately each model's merit can only be judged for its performance and suitability when compared with tangible process outcomes.

3.1.3.2.3. 2. Yield Optimization

Techniques for optimizing process yields include measurements of reference test structures over several build cycles, to make for the aggregation of process parameters, models extraction, recalibration and mitigation of identifiable failure-prone mechanisms.

Critical area reduction includes optimization of two complementary categories that can be integrated into the design cycle. One of which is an alteration of the layout topology and another involves the adoption of improved post-processing step methods that keep the layout fixed while alleviating congestion with more wire spacing for MEMS and IC based wafers. The former is most representative as it takes into account the critical area in conjunction with nominal routing targets, alongside an assignment of a cost function to shorts, vias, opens, and pinhole defects. An optimized yield with such systems would consist of modified routes and channels which places a premium on a reduction of the critical area between wire segments, and a reduction of the number of vias. Vias are particularly problematic as they invariably increase manufacturing complexity, are inherently unreliable on

account of void related stress. In essence, they result in the degradation of otherwise nominal process yield [72]. With declustering techniques, there is an emphasis on a redistribution of adjacent cabling, without a change in layout topology. Redistribution can be by compaction or noncompaction of the circuit slacks and this challenge is appropriately framed as a one-dimensional layout optimization problem Compaction of circuit slacks with heuristic algorithms, can result in optimized yields in a given layout, whereas noncompaction employs the rubber band wiring model [72].

Evaluation and improvement of design rules employed for a process can also lead to improved yields. Typical design rules entail line width constraints, spacing, or pattern density imposed by fabrication steps such as lithography, resist deposition, etch and implants. Additional factors influencing design rules include scaling, area overhead, layout migration and limits in design tool tolerances. Deterministic physical designs tend towards a greater amount of slack, and as this number of uncorrelated critical paths increase, any one of them can become the determinant of circuit related issues. Intentional under-optimization through the assignment of penalties to circuits close to critical paths is recommended as a design technique that increases the prospect of higher yields [72].

Opportunities for improved modelling of the MEMS device with commercial optimization tools, to more accurately reflect the physical reality of the operating conditions with parametric and correlation variables has been assessed as beneficial to improving yield. This is not without high computational demands and cost that are brought to bear on existing simulation stations due to these from the run of complex routines [75].

3.2 Conclusion

In this chapter, various fabrication methods and techniques have been discussed. Typical MEMS materials and factors governing their choice for use in these described methods were presented. We examined substrates, bridge layout compositions, dielectric and bridge support materials. The techniques examined here are cleanroom based, and each has had their advantages and limitations explained. They are broadly classified into deposition and film pattern generation techniques.

The performance metric employed in evaluating MEMS microfabrication process techniques was also reviewed. Typical metrics consist of process cost, equipment productivity and yields. Models for analysing, predicting and

optimising yields were examined, and opportunities for a holistic optimisation method beneficial to MEMS design and fabrication throughput were discussed.

This reviewed work on fabrication methods in this chapter and the discussion of the underlying principle of the operation of MEMS switches in chapter two allow for the development of a low-cost micro-fabrication technique for manufacturing RF MEMS switches and varactors without intensive cleanroom environments while using readily available materials. The proposal proceeds with a design methodology that incorporates the goals in view, and with the novel microfabrication technique to be developed. This design and considerations are presented in chapter four.

Chapter 4
MEMS shunt switch and varactor design

This chapter presents the design procedure adopted for the novel low-cost nonclean room fabrication method while still achieving considerable yields and a response that is consistent with specifications. We proceed with design considerations and guidelines developed for a capacitive MEMS shunt switch and varactor, against the backdrop of constraints imposed by fabrication and measurement range limits. Both switch and varactor design presented here are based on the underlying theory presented in chapter two.

4.1 MEMS shunt switch design

The fixed to fixed beam micromechanical shunt switch consists of an Aluminium bridge, clamped at both ends on the CPW ground through anchors,

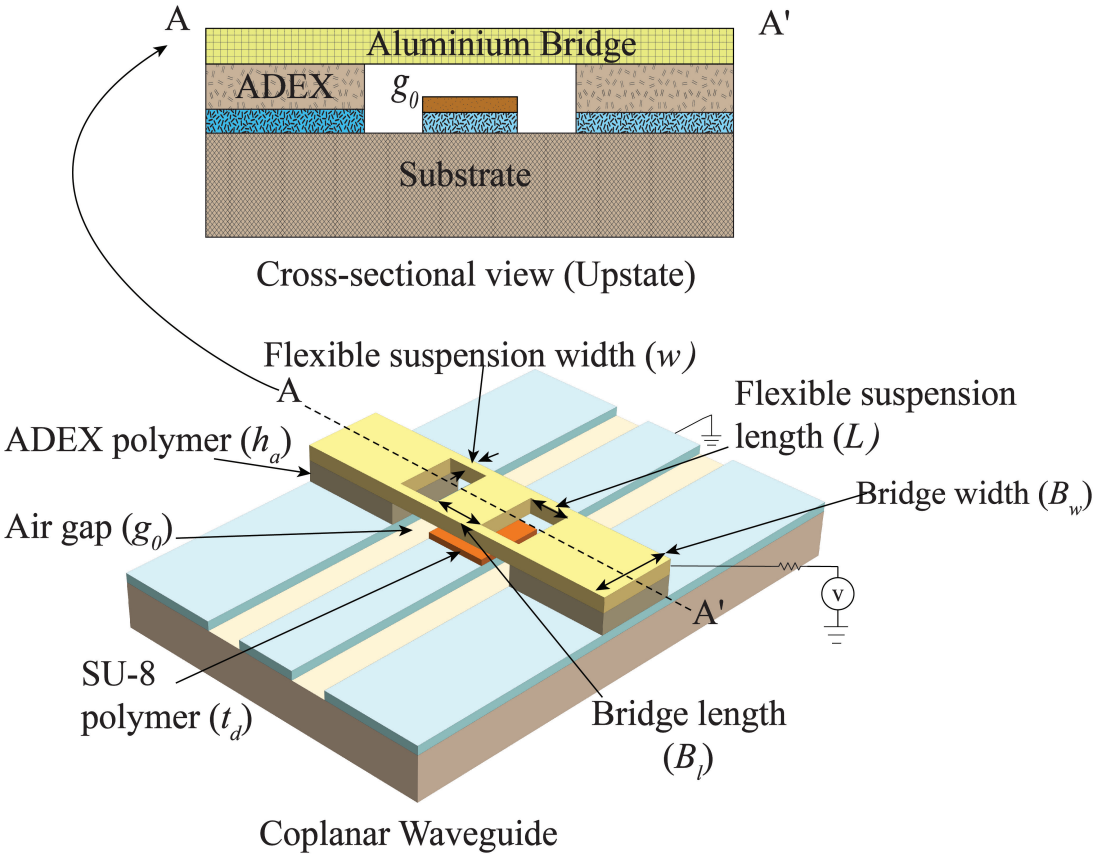

Figure 4.1a) 3D model of fixed-fixed flexural clamped MEMS shunt switch in the upstate position.

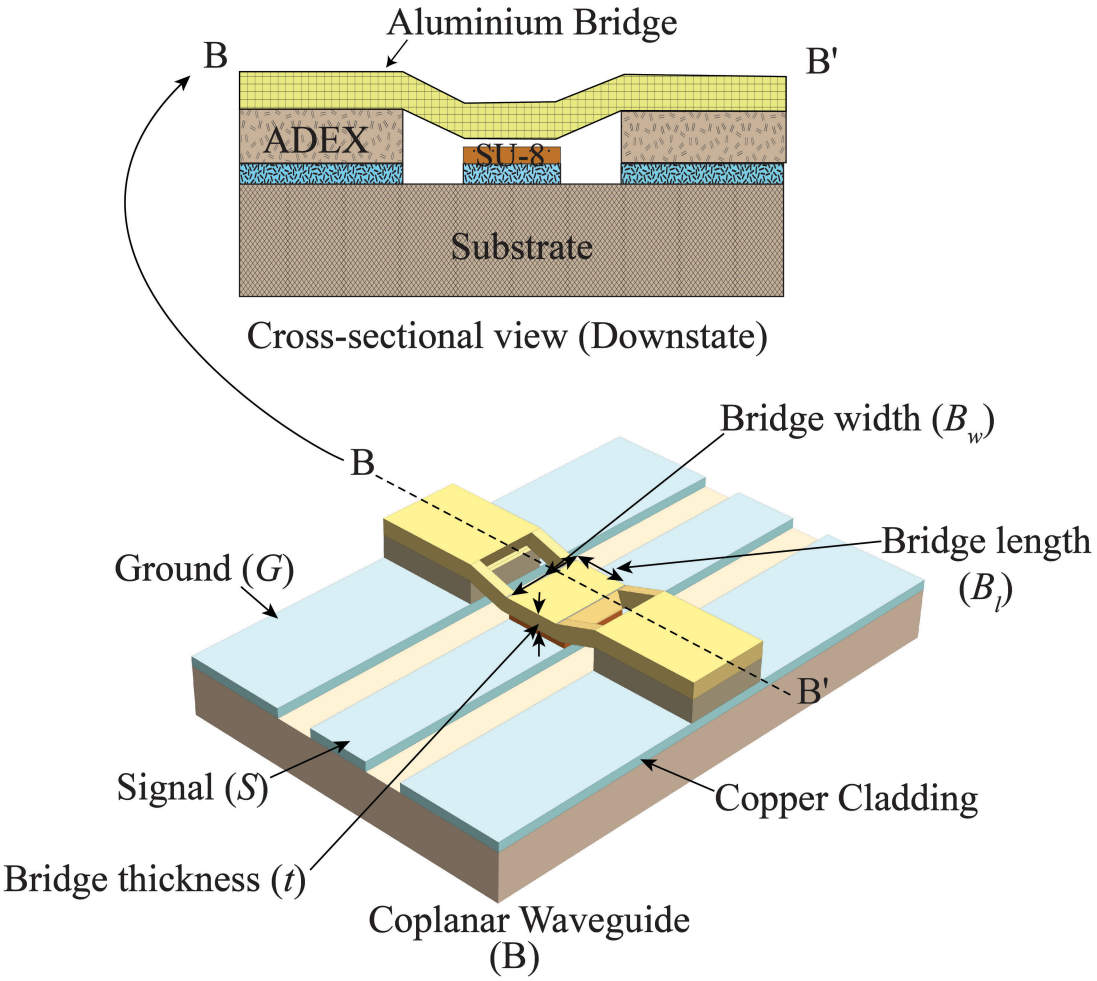

Figure 4.1b) 3D model of fixed-fixed flexural clamped MEMS shunt switch in the downstate position.

and a drive potential applied between the signal line and bridge as indicated in the 3D model shown in Fig. 4.1 a). This model also illustrates the shunt switch position in the OFF or upstate, and the 3D model of the downstate or ON position is illustrated in Fig 4.1 b).

The fixed to fixed Aluminium bridge of length, l µm, is suspended h_a µm over a coplanar waveguide transmission line, and is attached at both anchor ends by ADEX epoxy polymers. These polymer posts also serve to electrically isolate the MEMS Aluminium bridge from the CPW ground. An SU-8 resist layer of thickness, t_d, fabricated on top the centre signal conductor, serves as the dielectric providing additional capacitive coupling in the bridge-air-signal line interface, It helps prevents stiction during the mechanical travel of the bridge due to capacitive and frictional forces at that interface by preventing the build-up of static charges. The capacitive region of the switch consists of the gap, g_0, exist between the bridge, the centre conductor, the signal width (S µm), and the bridge width, w µm.

The design optimizes a matrix of conditions imposed by the fabrication and measurement limitations. These conditions are translated to include CPW dimension constraints, desired switching capacity, the dynamic response and anticipated RF performance. The CPW's dimension plays important roles in the waveguide's signal loss, bandwidth response [76] and determines the extent of the bridge length. The switching capacity, or the degree of isolation provided by the switch, is defined by its capacitance ratio. The mechanical and dynamic response of the fixed-fixed bridge is described by the d'Alembert's principle, which states that the aggregate of external forces, F, and the kinetic reaction acting on a constrained body equals zero [40]. These responses are related to the bridge stiffness, k, which in turn impacts on the pull-in DC potential, V_a. The underlying bridge mechanics and dynamic response theory has been discussed in chapter two.

4.1.1 CPW geometry design

The interconnection and packaging of Monolithic microwave integrated circuits (MMIC) on suitable substrates is mainly realized on planar transmission line structures, with conventional microstrip, slot, coplanar waveguide and coplanar strip receiving the most attention. Of the four transmission lines, microstrip and coplanar waveguide transmission line are considered most suitable for MMIC based on electrical performance and yield [77].

Coplanar waveguides consist of a centre conductor signal line, and adjoined on both sides by ground planes atop a substrate, and therefore forms a real planar waveguide [78]. Because it is a three conductor transmission line, it can carry two fundamental modes with zero cut-off frequency, the odd mode, and even mode. The desired even mode also called the coplanar mode is a low dispersion quasi-TEM mode, has even symmetry with respect to the symmetry plane, and is normally used for applications in circuit designs. The electric field lines begin or terminate at the centre conductor and they end or originate on the two surrounding ground planes. In this mode, the magnetic field lines enclose the centre conductor, and if the current is propagated on the signal conductor, the current densities in the ground planes are in the opposite direction. The low dispersion performance lends the CPW for use in broadband applications and makes it an allure for application involving MMIC circuits. Whereas in the parasitic odd mode, also termed slot line mode, the electric field lines start on one ground plane and end on the other ground plan, thus the potential of the two ground planes are opposite. In addition, not all of the electric field lines touch the centre conductor. If the substrate is metalized

or conductor backed, an additional parasitic parallel plate mode with zero cut-off frequency can be excited. Asymmetric discontinuities such as bends also induce parasitic slot line modes. These modes are suppressed with the use of bond wires or air bridges spaced a quarter wavelength or less apart, connecting the ground planes to force equal potentials. The bond wires also increase the cut-off frequency of the even mode, which reduces the prospect of their evolution into single higher TE modes at low frequencies. However, this single higher TE mode entails an elliptical polarization of the magnetic fields which makes it suited for wave propagation in non-reciprocal ferrite devices[1] [77]. Fig. 4.2 illustrates the electric field distribution for the

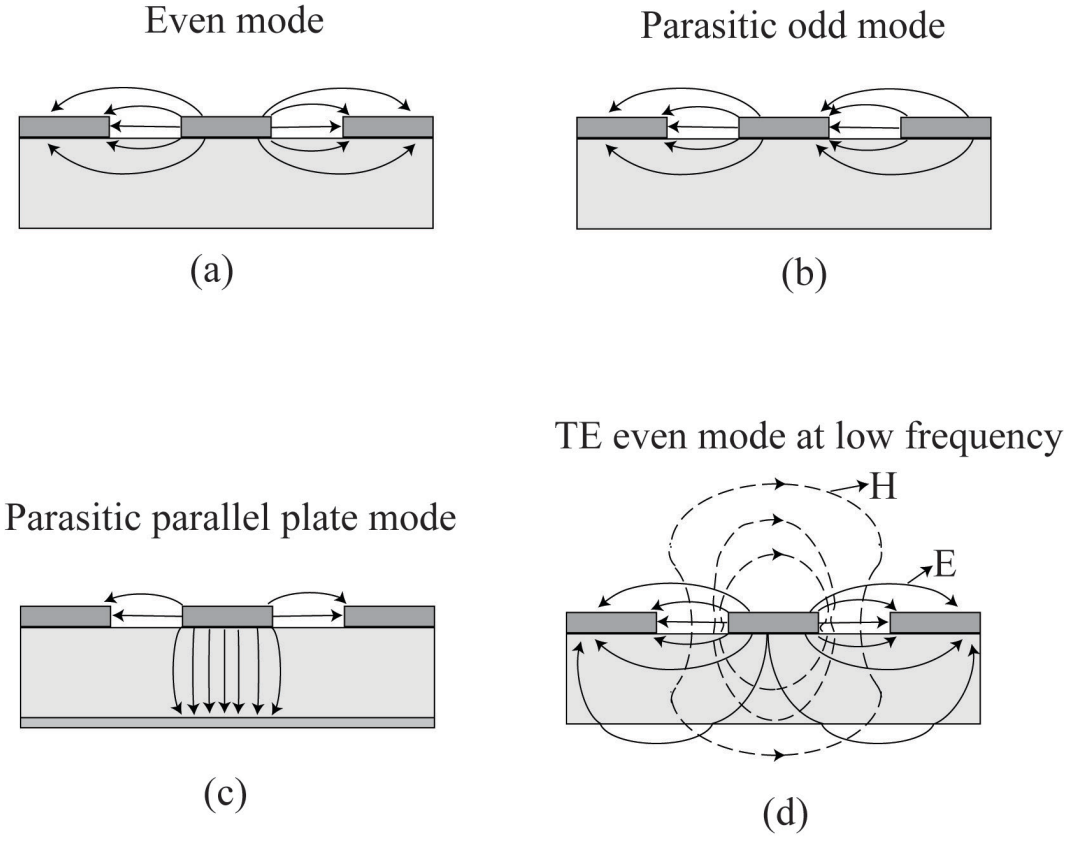

Figure 4.2 Coplanar Waveguide modes and their electric field distribution [79].

[1]The fundamental property of non-reciprocity is the capacity of ferrite materials biased by a static or switchable DC magnetic field, to produce a rotating magnetic field within the core, with its axis aligned in the direction of the bias field, when an RF signal is applied perpendicular to the biasing field. The sense of this rotation with respect to the bias field allows for dissimilar transmission coefficient through the ferrite for applied microwave signals.

corresponding CPW modes.

Coplanar waveguides offer unique advantages over microstrip lines in MMIC packaging due to the presence of a ground plane for active devices. Since they are devoid of via holes, they allow for a reduction in the number of processing steps and minimize critical region failure occurrence, hence improving the likelihood of increased yields. In addition, the presence of a pair of ground planes reduces crosstalk and coupling issues.

The shunt switch is designed to be fabricated on CPW transmission lines as it allows for ease of mounting. The lines also make for reduced radiation loss, and minimal crosstalk effects due to the presence of adjacent ground planes, alongside other advantages over microstrips. The closed-form expressions for the effective dielectric constant (ε_{eff}), and characteristic impedance (Z_0) of a CPW on a dielectric substrate of finite thickness, h_1 were derived in [76] using conformal mapping techniques which are functions of the ratio of modulus of the complete elliptic integral of the first kind and its complement. A CPW with finite dielectric height is as shown in Fig. 4.3, with the centre conductor width S, slot width G, and substrate thickness, h_1.

The effective dielectric constant ε_{eff} is shown to be [76],

$$\varepsilon_{\text{eff}} = 1 + \left(\varepsilon_{r1} - 1/2\right)\frac{K(k_1)K(k_0')}{K(k_1')K(k_0)} \tag{4.1}$$

where,

$$k_0 = S/(S + 2G) \tag{4.2}$$

$$k_1 = \frac{\sinh\left(\frac{\pi S}{4h_1}\right)}{\sinh\left(\pi^{(S+2G)}/_{4h_1}\right)} \tag{4.3}$$

$$k_1' = \sqrt{1 - {k_1}^2} \tag{4.4}$$

$$K(k_i) = K(k_i') = \int_0^{\pi/2} \frac{d\theta}{\sqrt{\left(1-k^2\sin^2\theta\right)}} = \int_0^1 \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}} \tag{4.5}$$[2]

and, the characteristic impedance is given as,

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} K(k_0')/K(k_0) \tag{4.6}$$

[2]Wolfram Mathematica, Ver. 10, 2014, Wolfram Research, IL., 2014.

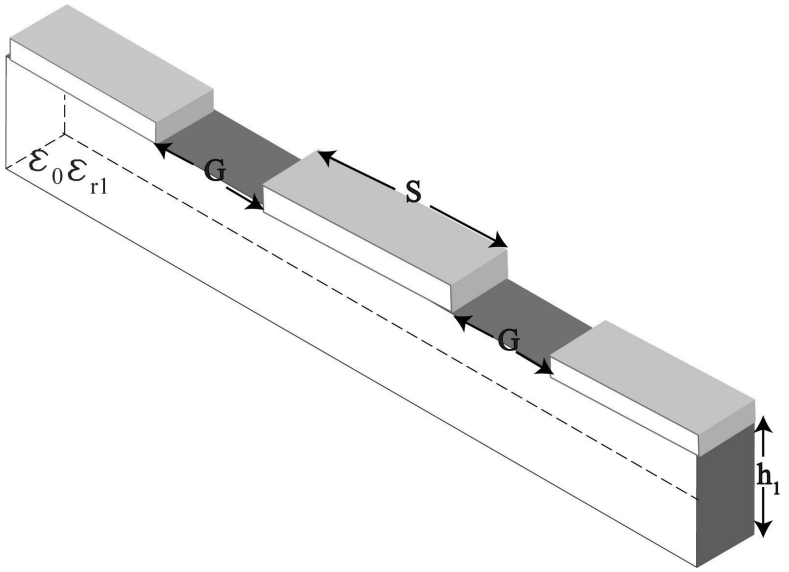

Figure 4.3 Isometric schematic of a CPW on a dielectric substrate of finite thickness [76].

The complex propagation constant for a transmission line, y, consists of the attenuation, α , and the phase constants, β. For a low loss CPW transmission line, these components are derived in [80] as,

$$y = \alpha + j\beta \tag{4.7}$$

$$\alpha \cong \frac{1}{2}\left(\frac{R}{Z_0} + GZ_0\right) \tag{4.8}$$

$$\beta \cong \omega\sqrt{LC} \tag{4.9}$$

where, ε_{r1} is the relative permittivity of the substrate, S is the centre conductor width, G is the gap between the centre conductor and the ground plane, h_1 is the substrate thickness, R is conductor loss, G is the dielectric loss, L and C are the series and shunt capacitance of the lumped element circuit model. The dielectric substrate thickness is usually set to about twice the gap width, to minimize radiation, and to concentrate the fields in the substrate area [81]. In addition, another important parameter in the design of CPW transmission lines is the total distance between the two ground conductors, S = W + 2G. As the centre conductor width (S) increases along with a widening of W, for each equivalent impedance a lower loss transmission line results [76].

The proposed CPW consists of an FR4 fibreglass dielectric substrate with copper cladded conductive top surface, in line with the low-cost premise of the project. Alternative substrates with low-cost possibilities for use include Roger 4350b and the Rogers 60xx family range of fibreglass substrates. Keysight's

Advanced Design System (ADS)[3] Linecal Kit was employed for various iterations of the CPW geometry, to make for an assessment of the design characteristic impedance and for ease of analysis.

Fabrication of the intended CPW transmission line would be by a laser ablation system with a minimum resolution of 15 μm. Given the need for miniaturization and that the guide wavelength λ_g in conventional printed circuits cannot be reduced more than $\sqrt{e_r}$ relative to the free space wavelength, lambda λ_0, it was decided that a slow-wave transmission line be employed. The slow-wave mechanism is generated by spatial separation of the electric and magnetic energy. Hasegawa in [82], proposed the realization of a cross-tie coplanar wave structure in which attenuation is predominantly due to conductor loss, with slow-a wave factor, λ_0/λ_g, as high as 15. It is also assumed that the geometrical size of the discontinuity or impedance step is very small compared to the waveguide wavelength [78]. It comprises periodica ally alternating high impedance Z_A and low impedance Z_A so the electric energy and magnetic energy are longitudinally and periodically stored in the high impedance region A and low impedance region B. The characteristic impedance presented to the voltage and current waves at the input reference terminal plane if this unit chamfered CPW transmission line was derived in [82] as,

$$Z_0 = \sqrt{Z_A \cdot Z_B} \tag{4.10}$$

Thus by appropriately choosing the combination of centre conductor width and slot gap width, G, control over the transmission line characteristic impedance presented at the input reference plan, and the associated slow-wave factor can be achieved.

In [78] it was proposed that a discontinuity in the waveguide can be minimized by using a linear taper between the waveguide sections structure for, $< 45^0$, with the accompanying reduction in the reflection coefficient, smaller than −10 dB over the frequency range, where an abrupt step was previously employed. It was thus decided that this angled transitioned ‘cross tie’ CPW transmission line structure be adopted, to make for reduced attenuation loss, and to also provide sufficient clearance for the MEMS switch while meeting in-house fabrication and measurement limitations. The linear chamfer makes for smooth RF signal transition between the two different impedance sections,

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[3]Advanced Design System, 2016 ver., Keysight Technologies, SR., CA, 2016.

and at the same time improves the capacitance ratio, by minimizing the upstate loading capacitance while maximizing the downstate loading capacitance [78].

The CPW transmission line parameters signal line width (S) and gap (G) are derived for a 1.524 mm thick FR4 substrate with er= 4.7, and determined to be 460 µm and 62 µm at the transmission feed input section, and 460 µm, and 340 µm respectively at the switch location corresponding to 40 Ω and 72 Ω, respectively. The saw shaped CPW transmission line is a periodic connection of two planar transmission lines, with different characteristic impedance Z_A and Z_B. The plan of this CPW layout is as indicated in Fig. 4.4.

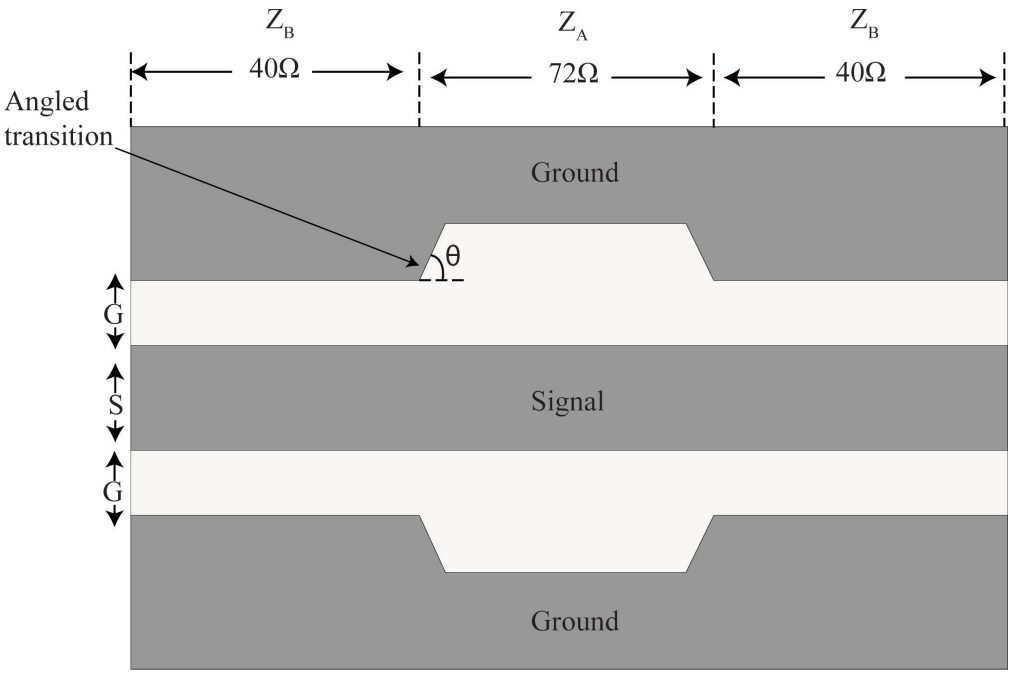


Figure 4.4 Top view of the CPW transmission line.

From [78], the impedance of this chamfered CPW transmission line is given as $Z_0 = \sqrt{Z_A \cdot Z_B}$ =53 Ω, and the tapered section designed to connect to the feed line through a 44^0 angled transition on the ground plane region. This section is introduced for smooth RF signal transition between the two different impedance (40Ω to 72Ω to 40Ω) waveguides to make for a transmission line with characteristic impedance $Z_0 \approx 50\ \Omega$. The unloaded CPW's performance was verified using the commercial 3D EM simulator Ansys HFSS[4].

[4]ANSYS HFSS Electromagnetic Suite, Release 2014, Ansys Inc., Canonsburg, PA, 2014.

4.1.2 Shunt switch bridge design

Chapter two of this thesis discussed background theory governing the models, operation, and analysis of electrostatic MEMS switches. Thus with the underlying theory already examined in the background, we proceed to present the adopted shunt switch design and to establish the design parameters which include: capacitance ratio, actuation voltage, and the dynamic response.

Proceeding from the CPW design and specifications, for an electrostatically actuated switch, the requirements of a large electrostatic area and accompanying surface to volume ratio favour a vertically moving bridge structure. This feature makes for ease of design of the mechanical travel distance, and accompanying flexibility in tuning range assignments from that excursion. The capacitive area of the proposed switch is bordered by the CPW signal width and vertical air interface excursion up from the signal line, to the bridge width.

The capacitive ratio, which was discussed in section two, describes the degree of discrimination between its ON and OFF states. This design choice of the capacitive ratio is considered with trade-offs between the bridge height and intended RF performance, as poor isolation characteristics are associated with low values of the bridge height, g, between the switch membrane and the fixed bottom electrode. The RF performance is limited by the roughness of the contact surface area, which in turn is dependent on the fabrication process employed. From (2.19), we observe that, C_r, depends also on the fringe factor, C_f, and can be expressed as [35],

$$C_r = \frac{\frac{\varepsilon_0 A}{t_d}}{\frac{\varepsilon_0 A}{\left(g + {}^{t_d}/_{\varepsilon_r}\right)} + C_f} \tag{4.11}$$

$$C_f = \gamma C_u \tag{4.12}$$

And as discussed in chapter two for shunt switches, it is customary for $\gamma < 1$, where C_u is the upstate capacitance. The capacitance area, $A\ \mu m^2 = w \cdot l\ \mu m^2$, is determined from (3.11) for a design dielectric thickness of 1 μm, and for set values of fringe factors, and ratios, $\gamma = 0.6$, and a capacitance ratio of 50. With $S + 2G$ obtained in section 3.1.1 as the limiting value of the capacitive region bridge length, the bridge width w is derived as 600 μm.

For electrostatic shunt switches, the pull-in voltage, V_p, as discussed in chapter two is dependent on the spring constant of the bridge, signal line width, bridge width, and the bridge height. As observed from (3.13), to realize a MEMS switch with a low pull in voltage, the air gap should be small, the

capacitance area should also be large. A large design capacitive area becomes problematic with fringe capacitance overriding benefits of reduced actuation voltages and compactness in design. After considering switch bridge geometries that were feasible with the fabrication method to be employed, and in order to actuate the bridge with manageable voltages of V_p, in the lower end range, it became imperative that a low spring constant, k, was required. The relationship between V_p and the bridge height, g_0, spring constant, k, was given in (2.44).

In addition, as discussed in chapter two, the switch opening time for an electrostatically actuated bridge is dominated by the release time, t_{pu}. The release time was derived in equation (2.62) of chapter two, it is related to the spring constant, and mechanical resonance frequency, f_0, by,

$$t_{pu} = \frac{\pi}{2}\sqrt{\frac{m}{k}} = \frac{\pi}{2}\sqrt{\frac{\rho v}{k}} \qquad (4.13)$$

where, m is the mass, ρ, is the density and v, is the volume of the bridge. From (2.44), it is required that the actuation voltage, $V_p < 150$ V, being the limit of the voltage measurement source, and due to limitations in the fabrication methods, g_0 is set to $5\ \mu\text{m}$ and t_d also chosen to be $1\ \mu\text{m}$. Hence the corresponding design spring constant design value, k, is obtained as ≤1.4 kN/m. Materials to be employed are ADEX™ dry film epoxy laminates which are catatonically cured polymers placed between two protective polyester sheets for the elevation of the bridge at the anchor posts to the required g_0, and SU-8 2002 deposits on the centre conductor for t_d.

MEMS bridge layout topologies have been discussed in [40], alongside their corresponding closed-form expressions for spring constant, k, contributions. The fixed-fixed beam topology was chosen as a result of the ease of fabrication with the laser ablation system, in addition to having the desired mechanical response and sufficient self-restoring force while making for reduced actuation voltages. The top view of this fixed to fixed bridge structure is as shown in Fig. 4.5. An analytical expression for the spring constant was discussed in chapter two from which an approximate expression for the spring constant derived in (2.37), with the biaxial stress term component neglected, is given as,

$$k = 4Ew\left(\frac{t}{L}\right)^3 \qquad (4.14)$$

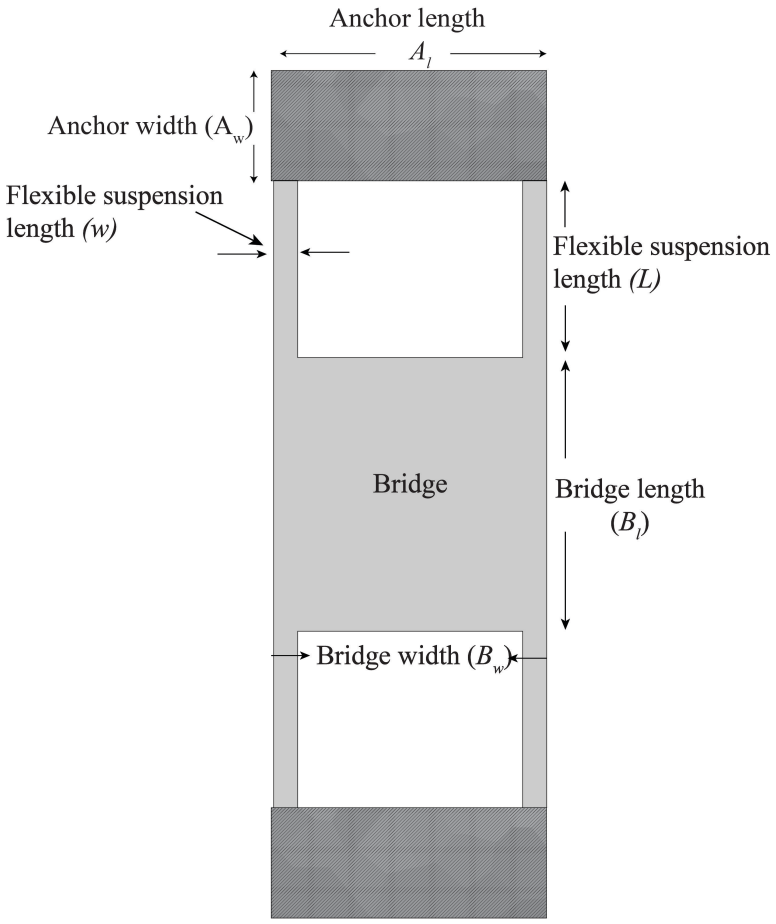


Figure 4.5 Plan view of MEMS shunt bridge.

where, E, is the Young Modulus of the Aluminium bridge, w, is the flexible suspension width, L, is the suspension length, and t is the bridge thickness.

The bridge is composed of a high purity Aluminium foil, with Young Modulus E=70 GPa, thickness $t = 14\ \mu\text{m}$, and density, $\rho = 2.70\ \text{g/cm}^3$. Thus, from (4.13) and (4.14) combinations of w and L, in the proposed layout are required to be derived to realize designed spring constant value $k \leq$1.4 kN/m, and reliable switching times, t_{pu}, for bridge volume, $v = t(l \cdot w + 4 \cdot w\, L) = (6.72 * 10^{-6}\text{cm}^3 + 5.6 * 10^{-3} wL\ \text{cm}^3)$.

From (4.14), for corresponding values of k, ρ and the derived equivalent expression for v, t_{pu} is given as,

$$t_{pu} = 0.0689\sqrt{(6.72 * 10^{-6}\text{cm}^3 + 5.6 * 10^{-3} wL\text{cm}^3)}\ \text{s} \qquad (4.15)$$

The switching time t_{pu} is set ≤ 200 μs, and if w is defined as $\leq {}^{L}/_{3}$, then we derive $w = 40\ \mu\text{m}$, and $L = 140\ \mu\text{m}$. It was decided that both w and L be set to 50 μm, since they still satisfy the desired spring constant constraint, but more importantly, because the widths of cut Al strips tend to be smaller as observed from prior laser structured experimental workpieces. This is due to the laser beam overlapping at either of the workpiece edge during the precut

and heat job phases of the structuring job phase cycle. It is thus appropriate that the design width of the Al strip is slightly wider than that obtained from theoretical computations.

Substituting derived values of w and L in (4.14), and (2.44) results in a design spring constant value, k of 1.12 kN/m and pull-in voltage values, $V_p = 135\,V$. The anchor posts are designed with to ensure a reasonable clearance at the bridge termination points on the ground plane with lengths, A_l of 600 µm, and A_w width, 250 µm.

A summary of the designed shunt switch geometry parameters and dimensions is as shown in Table 4.1.

Table 4.1 RF MEMS switch geometry and parameters

Symbol	Geometry and material parameter	Values
E	Young Modulus of Al	70 GPa
B_l	Bridge length	460 µm
B_w	Bridge width	600 µm
t	Bridge thickness	14 µm
h_a	Bridge height	6 µm
w	Suspension width	50 µm
L	Suspension length	140 µm
t_d	Dielectric height	1 µm
C_r	Capacitance ratio	50
V_p	Actuation voltage	135
A_l	Anchor length	600 µm
A_w	Anchor width	250 µm

4.1 MEMS shunt varactor design

Varactors are low capacitance ratio switches, and are incorporated in low power RF circuits to present limited tuning ranges for variable filters, antennas, and oscillators, and are described by capacitance ratios up to 4 [83]. It is derived from the variable capacitor and it is not uncommon to find varactors with extended tuning range and high power handling capabilities, by employing a bank of MEMS switches or stacked parallel plate architectures, or variations in the layout structure as reported in [84-86].

The vertical deflecting diaphragm or bridge describes the general layout of the architecture in electrostatically actuated MEMS varactors, and the equivalent lumped model also follows that discussed for the switch in section two. The

distinction is the degree of sensitivity and tuning range that is factored into the design and structural layout choice.

The proposed design of the MEMS varactor is the suspended crab-leg flexure diaphragm indicated in Fig. 4.6. The varactor consists of an Aluminium bridge membrane suspended over a coplanar waveguide transmission line, supported at both ends by anchors resting on the CPW ground plane. In addition, two polymer deposits isolate the diaphragm from the ground, and a thin layer on the CPW signal line protects against stiction.

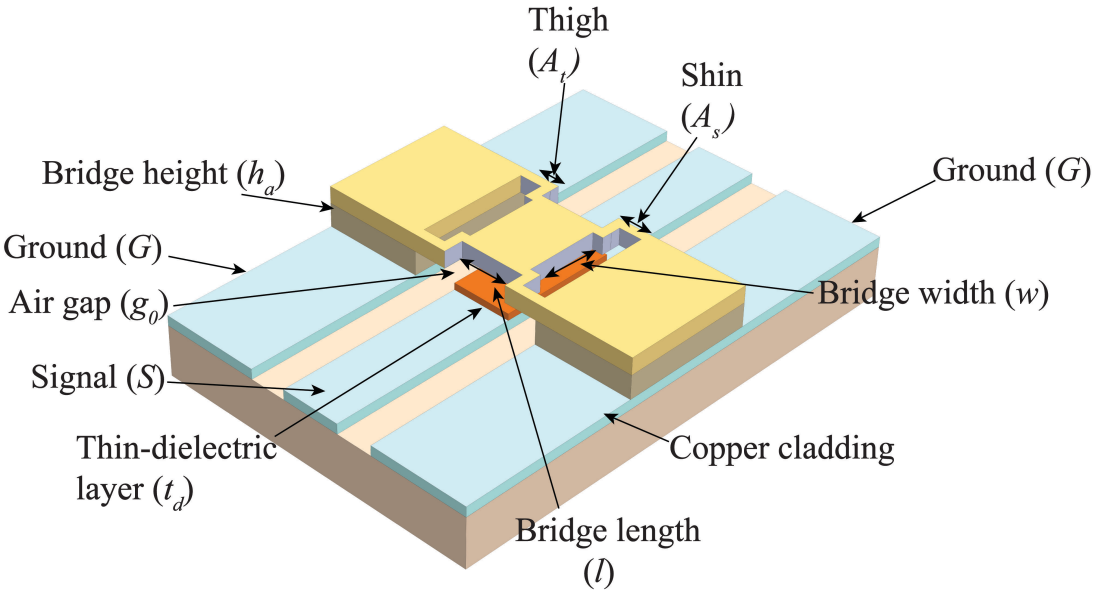


Figure 4.6 3D model of crab-leg flexure MEMS varactor.

The diaphragm geometry offers the highly required sensitivity and robustness that defines a varactor when in operation. As with micromachined structures, concerns about the impact of residual stress and reaction to imposed force contributes to design choice. Folded suspensions have the advantage of a higher degree of freedom to expand or contract where residual stress is present. In this design, the folded suspension architecture makes for ease of expansion and contraction and is considerably stress-free [87]. Under acceleration from an impressed perpendicular force, the bridge moves up and down in piston-like trajectory. During this travel electrostatic feedback ensures the mass centroid remains in its neutral position so that the stress in the suspension is minimized [87]. Four suspensions are symmetrically located at the four corners of the diaphragm to minimize any higher vibration modes while offering a compliant suspension system, while also allowing for compactness. An analysis of the mechanical properties can be executed with

an examination of on the suspensions and by a superposition of the overall suspension system.

The free body diagram of the crab-leg geometry is shown in Fig. 4.7, consists

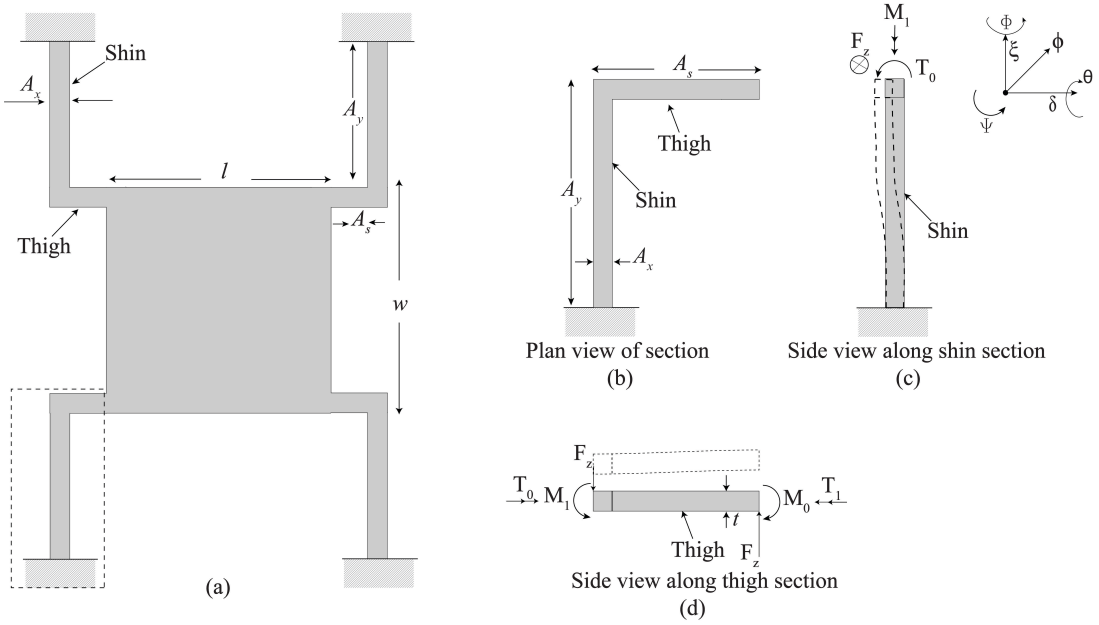


Figure 4.7 Free body diagram of crab-leg flexure MEMS varactor, with displacement due to electrostatic force, F_z [41].

of the shin section of length, A_y, and thigh of length, A_s., the bridge of length, l, and width, w. The shin and thigh sections are of uniform width, A_x, and thickness, t. The total deflection of the mass centroid along the z axis, consists of deflections, in dotted lines, and torsional reactions, T_i , of the shin and thigh sections due to the vertical acting force. The strain energy from the torsion is described as [41],

$$U = \int_0^{A_{x,y}} \left(\frac{M^2}{2EI_x} + \frac{T^2}{2GJ} \right) d\xi \qquad (4.16)$$

where, T, is the torsion, G is the torsion modulus of elasticity, and J is the torsion constant. The Young Modulus, E, is related to the torsion modulus, G, and Poisson's ratio, ν by,

$$G = {}^{E}/_{(1+2\nu)} \qquad (4.17)$$

And the torsional constant for a rectangular cross-section beam of thickness, t, and width, w, is given as [40, 41],

$$J = \frac{1}{3} t^3 w \left(1 - \frac{192t}{\pi^5 w} \sum_{i=1,\ i\ \text{odd}}^{\infty} \frac{1}{i^5} \tanh\left(\frac{i\pi w}{2t} \right) \right) \qquad (4.18)$$

The moment, M_i, and torsion, T_i in each beam segment in the free body diagram is then defined, and the guided end constrains, θ, and ϕ, are substituted in the Castigliano's second theorem to obtain associated vertical displacement and spring constant for one of the suspensions in [41]. In [87], an alternative route was employed with the short form expression for the stiffness constant for one of the suspensions given as [87],

$$k_1 = \left. EA_x\left(\frac{t}{A_y}\right)^3 \right/ 1 + \frac{A_y}{A_s}\left[\left(\frac{A_y}{A_s}\right)^2 + 12\frac{1+\nu}{\left(1+\left({}^{w}/_{t}\right)^2\right)}\right] \tag{4.19}$$

Since the bridge suspension system is the sum of the four suspensions, the spring constant for crab leg flexure is given as [87],

$$k = \left. 4EA_x\left(\frac{t}{A_y}\right)^3 \right/ 1 + \frac{A_y}{A_s}\left[\left(\frac{A_y}{A_s}\right)^2 + 12\frac{1+\nu}{\left(1+\left({}^{w}/_{t}\right)^2\right)}\right] \tag{4.20}$$

where E is the Young Modulus of the bridge, ν is the Poisson's ratio. When ${}^{A_y}/_{A_s} \gg 1$, the total spring constant approximates to analytical expression derived for the fixed beam to beam bridge [87] derived in chapter two. The capacitive characteristics of the varactor, with the design of the bridge area, capacitive ratio, and coupling gap would follow to make for a complete definition of the varactor.

4.2.1 Varactor bridge design

Following a similar design procedure employed in section 3.1.2, the shunt switch bridge design depends on the CPW line specifications and thus the capacitive area, and defined capacitive ratio. As previously discussed the pull-in voltage, V_p, is dependent on the spring constant of the bridge, signal line width, bridge width, and the bridge height. The signal line width and bridge width constitute the capacitance area, $A\ \mu\text{m}^2 = w \cdot l\ \mu\text{m}^2$, and is determined from (4.11) for a design dielectric thickness of 1 μm, and for a set fringe factor value, $\gamma = 0.25$, and a capacitance ratio of 4. In addition, the bridge width w is derived as 750 μm, for the corresponding limiting value of CPW signal line width, S.

The crab leg varactor bridge geometry adopted shown in Fig. 4.8, with anchor posts, makes for smaller values of spring constant, k, hence allowing for actuation with voltages of V_p, in the lower end range.

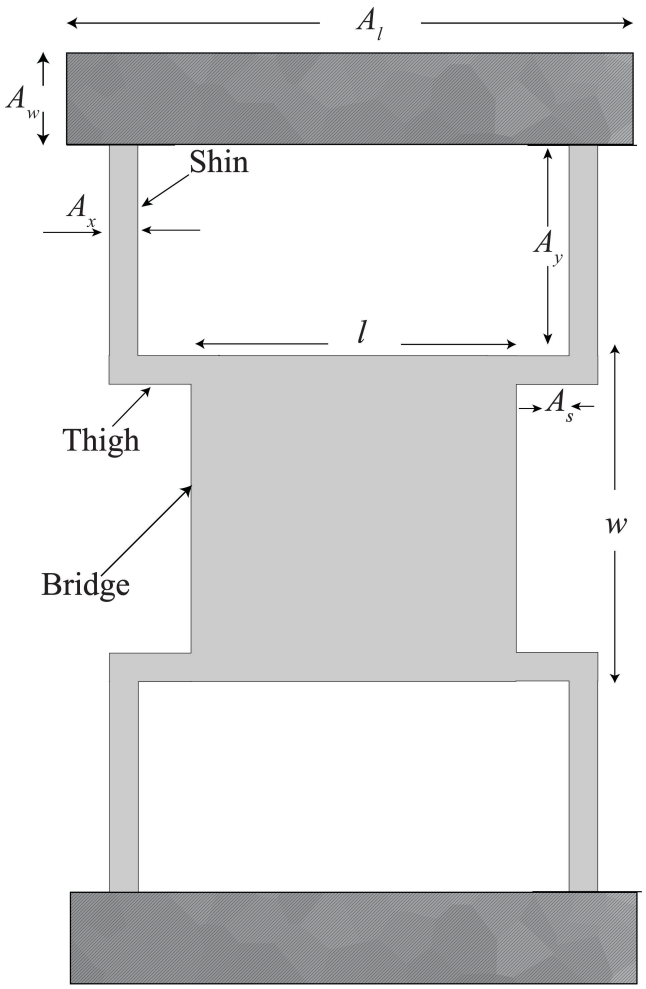


Figure 4.8 Plan view of the MEMS varactor.

Analysis of the mechanical parameters governing its dynamic response has been discussed in the preceding section. The actuation voltage is defined in (4.13), and dependent on the spring constant k, capacitance area, $A\ \mu\text{m}^2$, br idge gap height, g_0, and dielectric thickness, t_d. In addition, and from limitations in the fabrication methods, g_0 is set to $1\ \mu\text{m}$ and t_d defined as $1\ \mu\text{m}$ the actuation voltage is required to be, $V_p < 20$ V.

The spring constant also defines the switching speed and is related to the mechanical resonance frequency f_0 by (4.13), thus with limiting values defined, of k, can be obtained for V_p. Thus for an Aluminium bridge foil with Young Modulus E=70 GPa, thickness $t = 14\ \mu\text{m}$, and density, $\rho = 2.70\ \text{g/cm}^3$, combinations of A_x, A_y and A_s are required to be optimized for set release switch times, t_{pu}, to realize a limiting design spring constant value $k \leq 350$ N/m, for bridge volume $v = t\left(l \cdot w + 4 \cdot A_x\left(A_y + A_s\right)\right)\text{cm}^3 = \left(4.41 * 10^{-6}\ cm^3 + 5.6 * 10^{-3} A_x\left(A_y + A_s\right)\ cm^3\right)$.

From (4.13), for corresponding values of k and ρ,

$$t_{pu} = 0.15\sqrt{\left(4.41 * 10^{-6} cm^3 + 5.6 * 10^{-3} A_x \left(A_y + A_s\right) cm^3\right)}\ \text{s} \qquad (4.21)$$

As we can see from (4.13), a lower value of k, with other parameters kept constant conduces to higher switching times. Thus for this geometry, we set the release switch time to $t_{pu} \leq 400$ µs, and if A_x and A_s are both defined as $\leq {}^{A_y}/_{3}$, then we derive $A_x = A_s = 45$ µm, and $A_y = 140$ µm from the range of values possible under the inequality curve. These derived values were set to 50 µm for A_x and A_s, since they still satisfy the constraints set for k, and more importantly because Al laser structured widths are likely to be smaller due to the laser beam overlapping at either of the workpiece edge during the preheat and heat job phases of the structuring job phase cycle.

Substituting derived values of A_x, A_y and A_s in (4.20), and (2.44) results in a design spring constant value, k of 380 N/m and pull-in voltage values, $V_p = 21\,V$, which closely satisfies the conditions indicated while still allowing for geometries that are realizable with the fabrication methods. As with the shunt switch, the anchor posts are designed to allow for sufficient clearance at the bridge termination points on the ground plane for design lengths, A_l of 700 µm, and A_w width, 250 µm.

A summary of the varactor geometry parameters and dimensions is as shown in Table 4.2.

Table 4.2 MEMS varactor geometry and parameters.

Symbol	Geometry and material parameter	Values
E	Young Modulus of Al	70 GPa
l	Bridge length	450 µm
w	Bridge width	700 µm
t	Bridge thickness	14 µm
h_a	Bridge height	2 µm
A_x	Suspension width	50 µm
A_s	Thigh length	50 µm
A_y	Suspension length	140 µm
t_d	Dielectric height	1 µm
C_r	Capacitance ratio	4
V_p	Actuation voltage	20
A_l	Anchor length	700 µm
A_w	Anchor width	250 µm

4.3 Conclusion

In this chapter, the design of both the MEMS switch and varactor has been explained. The methodology derives from obtaining functional devices with governing operational principles reviewed in chapter two, and fabrication and measurement limitations in mind. The design process sought to optimize a set of conditions imposed by these limitations, to make for the determination of the CPW dimensions, the mechanical response, desired switching capacity and RF performance.

A chamfered shaped CPW layout designed on a 1.524-mm thick, low-cost, thermoset laminate FR4 substrate was employed with the angled transition to make for a characteristic impedance of 50 Ω. Fixed to fixed, H-shaped bridge and crab leg diaphragm topologies were adopted as configurations to realise designed MEMS switch and varactor respectively. The bridge specifications were for high purity 14 μm thick Aluminium foil. The capacitance ratio, C_r , and actuation voltage, V_p , were determined from reviewed equations, and they allowed for the determination of both bridge geometries adopted, with trade-off decisions to minimise material losses while making for ease of fabrication. C_r values of 50 and 4 were designed for the switch and varactor respectively. While the actuation voltage, V_p , were respectively determined to be 135 V and 20 V for the switch and varactor. The designed CPW and MEMS 3D models RF response were simulated using 3D EM simulator Ansys HFSS®, while the dynamic perfomance were examined using NASTRAN®.

With the bridge geometries now conveniently described, it is meet to employ the MEMS fabrication method developed in the course of this research to realise the devices, an endeavour embarked upon in chapter four.

Chapter 5
MEMS shunt switch and varactor fabrication technique

This work presents the novel fabrication technique for realizing MEMS devices, without intensive clean room requirements while achieving reasonable yields and performance response consistent with design specifications. We use a laser machining, wet bench dry film emboss fabrication process to fabricate these devices based on the non-clean methods, and from readily available materials. First, we proceed with a characterization of the equipment and optimized cost-effective experiment techniques which informed our choice, then the steps adopted to fabricate both MEMS devices are presented.

5.1 Fabrication equipment characterization

MEMS switches and varactors structures require the micromachining of bridge members, channels or gaps, and transmission lines according to design specifications, with some allowance for deviations in the fabricated component. The microfabrication method employed in this study entails techniques involving laser micromachining, spin coating, development, baking, hot film embossing, and lamination. The parameters studied and considered to have a direct effect on the output in each fabrication point in the cycle is discussed in the accompanying section.

5.1.1 Laser machining

Laser-induced direct patterning or machining refers to the process where an intense laser beam is used to affect an area resulting in patterns. Energy is absorbed and reflected on the incident target region. The absorbed laser energy heats up a volume of the target material, which is then transformed into liquid and or gaseous phase, with expulsion from the interaction region through hydrodynamic actions from a one or a combination of the effects of surface tension, capillary, equilibrium initiated drift toward cooler sites, vapour pressure, vapour driven splashing, the presence of intense light, etc. This material departing process is generally referred to as ablation. The volume of material ablated by a laser pulse depends among other factors on the area of the focused laser spot, environmental conditions, material surface characteristics; and the affected depth, which is determined by the heat penetration resulting from temperature distribution [88, 89].

Laser machining consists of surface patterning, structuring, drilling and ablation of target surfaces with radiation emitted from a laser source system.

Laser micromachining provides a cost-effective structuring alternative as opposed to cleanroom based traditional circuit patterning techniques which were discussed in chapter two. Another allure that makes for the embrace of laser micromachining is the ability to structure a wide range of materials making for a localized vertical production cycle. Laser ablation systems can be categorized according to the physical nature of the active medium used, and they include: solid-state lasers (Nd: YAG, Ruby, Nd: glass, Nd: YLF, Er: YAG), gas lasers (CO_2, HeNe, Argon, Krypton, XeF), semiconductor lasers (InGaAs, AlGaInP, AlGaAs, InGaAsP), and dye lasers (Rhodamine, Coumarin, Stilbene) [85]. Of these the most commonly employed are CO_2 (9.4 to 10.6 um), IR (1064 nm), excimer (248 nm) and UV (Nd: YAG, 355 nm) laser system.

The UV laser system operates at low power levels and structures materials through the cold ablation, from a reduced heat affected zone (HAZ), that minimizes burring, charring, and other negative effects associated thermals stress typically associated with high powered lasers like the CO_2. This reduction in stress is significant for miniaturization, as space saved after accounting for the diminished cut cushion, implies considerably more components can be packed onto a wafer, making for improved efficiency. This reduced packaging allows for research opportunities in circuit microfabrication. The excimer laser offers the best across board absorption rates for all laser types but is significantly pricier, than the UV laser, while the IR laser is primarily suited for processing metallic layers, and due to a higher reflectance (0.9 to 0.99) relative to UV laser (0.4 to 0.95), less metal is ablated [91]. The CO_2 laser beam is limited in its resolution power and is unsuited for track widths less than 250 µm [90].

The Nd: YAG laser consists of crystalline YAG with a chemical formula $Y_3Al_5O_{12}$ as the host material. Commercial Nd: YAG laser is available in frequency-tripled (355 nm) and frequency-quadrupled (266 nm) modes, and in a frequency-doubled mode where the laser output is in the green portion of the visible light spectrum at 532 nm. The process of achieving population inversion necessary for stimulated emission through excitation of the electrons to the higher energy states is referred to as pumping. Without this inversion, there will be a net absorption of emission instead of stimulated emission. The light source for pumping depends on the absorption characteristics of the crystal [88].

The output of the Nd: YAG laser can be continuous, constant amplitude (continuous wave mode), or periodic (pulsed beam mode). With continuous

beam operation, a constant laser energy is discharged uninterruptedly for long parses, from excitation provided by continuously krypton-filled or xenon-filled arc lamps or semiconductor diodes. In pulsed mode operations, flash lamps are generally used for the stored pumped energy that is held until a threshold is reached, after which the stored energy is rapidly discharged in short duration pulses of high energy density.

Another important parameter associated with laser beam outputs is the repetition rate, defined as the number of pulses emitted per unit time. With pulsed lasers, the pulsing may be executed via mode locking, Q-switching, and normal pulsing. In normal pulsing, typical pulse durations are of the order of microseconds to milliseconds, with control effected by changing the varying the inductance and capacitance in the circuitry of the flashlamp. Whereas in Q switching, short and intense laser pulses are obtained by changing the resonant properties, Q, of the flashlight crystal cavity after each pumping pulse in the laser output. It can be achieved by a rotating mirror method, passive Q-switching, electro-optic Q-switching The cavity Q value is a measure of its ability to store radiant energy. In Q-switching, pulse repetition rates are in the order of hundred kilohertz. In mode locking repetition operation, a train of extremely short and equally spaced pulses are produced, from a modulation of the gain or loss of the laser cavity at frequencies equalling that of the intermodal frequency operation. This conduces to a fixed phase relationship and oscillatory behaviour in the laser output. Typical repetition rates are in the range of megahertz to gigahertz [88].

Structures fabricated with traditional MEMS device fabrication processes discussed in chapter two are realizable with laser micromachining methods [92]. In addition, microstructuring of the MEMS switch with laser micromachining also allows for more capacitance variation as they are comparatively larger in size. It is the chosen technique for low-cost rapid prototyping and microelectronic packaging of MEMS structural members including Aluminium, stainless steel, polyimide films, for use on PCB, silicon and ceramic based substrates [92-94].

In this work, all device deflecting members, microlithography masks, and the CPW transmission lines are micromachined using the 355 nm Nd: YAG diode-pumped solid-state laser system in the LPKF ProtoLaser U3™. Key to process work with lasers is the transfer of the energy of an electromagnetic wave onto a target material. The total energy transferred depends among other things on the absorption of the laser beam by the processed material, and the amount of applied energy which accurately conduces to an interaction between the

target and often cited system specifications, which include laser beam intensity and pulse energy. The response of the target material to this applied energy with respect to absorption and other related effects includes indirect melting of the substrate, artefacts redeposition and resolidification [95]. These effects can interfere with other fabrication process and overall electrical integrity. This requires that as part of the machine tooling process, there is room for the ability to tailor and control the applied energy to specific areas necessary to structure the designed circuit geometries, in concert with a set of optimized process parameters.

5.1.1.1 LPKF ProtoLaser U3 characterization

The LPKF ProtoLaser U3 system consists of the laser source, cooling unit, laser beam processing system, positioning system and the camera system. The LPKF ProtoLaser U3 positioning system is as indicated in Fig. 5.1.

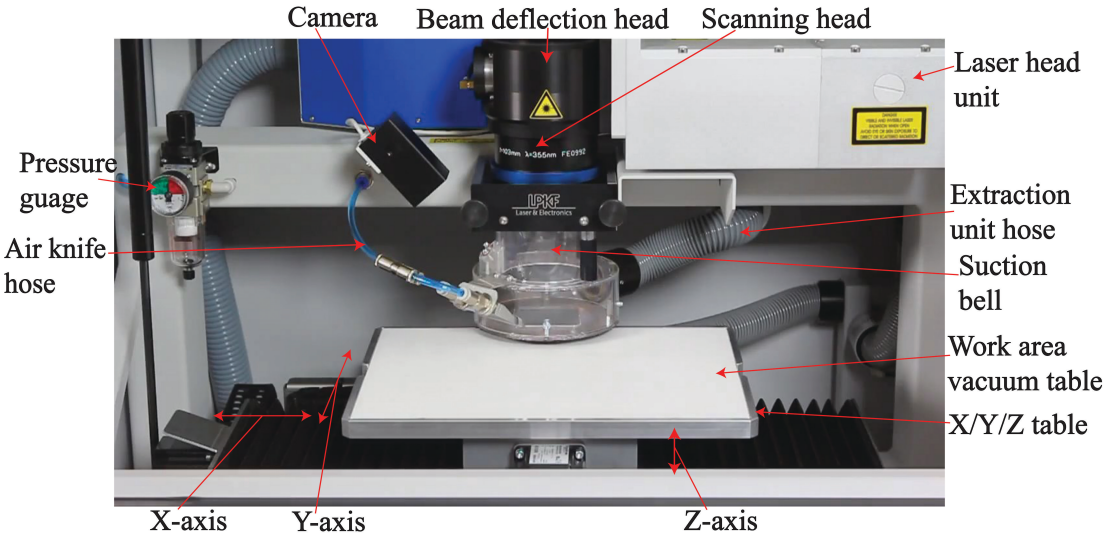


Figure 5.1 LPKF ProtoLaser U3 positioning system.

The laser source employed in the LPKF ProtoLaser U3 is an Nd: YAG diode pumped solid state laser system, which delivers 5 W of 355 nm UV radiation. This source provides sufficient power at 15 µm beam resolution to make for the structuring of PCB, LTCC, thin sheet metals, polyimides, resists and drilling cavities/ fiducials in dielectric materials [96].

The laser beam processing system consists of an expansion, deflection and focusing units comprising of two 45 ° deflecting mirrors, the X/Y galvanometer scanners in the scanning head, and a telecentric F-theta lens, which allows the beam to be deflected across the work surface. The LPKF ProtoLaser U3 beam deflection system is indicated in Fig. 5.1. This system of deflections produces an image field called the scanning field. The incident light beam travels from the source to the galvanometer scanner mirror surfaces, which

can be rotated to form cushion or barrel distorted images. These images combine to form a square image after calibration in the scanning head. A reddish pilot laser, quite apart from the UV structuring laser, allows for zeroing of this scanning field, measurement of the workpiece material size and thickness, and its alignment on the vacuum table. The positioning system consists of the X/Y/Z vacuum table, which moves the workpiece under the laser according to addressed laser fields in the LPKF CircuitMaster 1.0™ produced job file. The workpiece is positioned flat against the surface and affixed to the table with aid of a suction pressure vacuum line. The table's travel along the X/Y/Z plane is driven by a stepper motor via a gear system, which also helps to make for the optimal focus of the beam on the workpiece. Also attached to the positioning system is an extraction socket atop the suction bell which supplies the table with high-pressure air, clearing debris and cooling the workpiece, thus limiting the possibility of redeposition of chaff

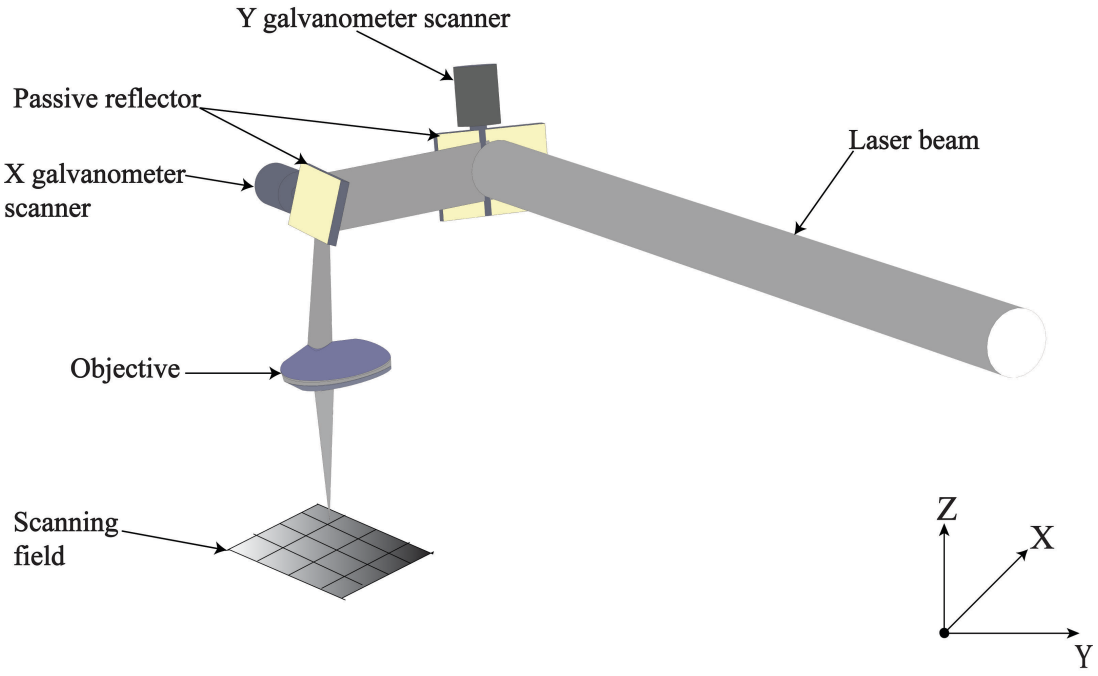


Figure 5.2 LPKF ProtoLaser U3 beam deflection system [96].

on the target material surface. A camera is positioned on the on the ring socket light fixture, to capture live and still images of progress on the work, and for remote monitoring of the job. The LPKY ProtoLaser U3 unit is cooled by an internal cooling circuit, with embedded exchange water pipes circulating fluid from an in the situ intake supply system, with the expulsion of the spent water facilitated via a discharge outlet. The LPKF ProtoLaser U3 parameters specification is as indicated in Table 5.1.

Table 5.1 LPKF ProtoLaser U3 technical parameters specification [96].

Parameter	Value
Maximum layout area (X/Y/Z)	229 x 305 x 10 mm
Laser beam source	Nd:YAG diode
Laser wavelength	355 nm
Laser power	5 W
Beam focus diameter	15 µm
Laser pulse frequency	25 -200 kHz
Mark speed	1 mm/s to 2000 mm/s.
Laser jump delay	1 µs to 1×10^6 µs
Laser jump speed	1 mm/s to 6000 mm/s
Minimum pitch on planar surfaces	75 µm (trace width of 50 µm and a clearance of 25 µm)
Resolution inside the scan field	2 µm
Repeatability	± 2 µm
Laser pulse frequency	25 – 200 kHz continuous wave (CW)
Air supply	8 bar
Cooling	Water cooled (internal cooling circuit)

Parameters used during the structuring of a workpiece fall under scanner parameter group, and includes mark delay (µs), mark speed (µs), jump delay (µs), jump speed (µs), repetition, z-offset (µm). These parameters are mutually dependent, and conduce to create structured patterns on the workpiece for the laser beam excursion during the work sequence (production phase) and require optimization for job phase in view. During structuring, the laser beam scans in two distinct patterns, contour and hatching patterns, on the scanning field. The contour pattern is used for creating the borders of the LPKF CircuitPro PL 2.0™ generated geometric structure, by joining a number of linear segments, whereas hatching and other variations of the laser heat job phases are used to obtain a rubout of the designated region between the insulated CAM generated layer vector segments. Improvements of the edges of the structure can be made with an extra contour line separating the rubout regions from the structured geometry. This, however, is not without a loss in the workpiece material at the structured vector edges. Additional scan field patterns include the precut, short heat, text, heat, short heat and dot patterns. These patterns are components of the CAM generated hatch grid patterns, employed in treating the HAZ with preprogrammed amounts of heat, and limited simultaneous ablation and contouring to make for a thin vector inscription in the case of text pattern for an output similar to that obtained in silkscreen engraving, or the ablation or rubout of materials. A description of

each of these laser parameters makes for an understanding of the operation of the machine and the derivation of an optimized routine proceeds as follows.

The laser pulse frequency indicates the open/close sequence of the light source and can be varied from 25 -200 kHz. As a rule, the lower this amount, the higher the laser power within a pulse. The laser power parameter specifies the instantaneous laser power consumption.

The laser mark speed dictates the speed of the laser beam while processing the structure vectors, during the movement of the mirrors with the shutters open. This value alongside the frequency is markedly important as it is decisive for material removal. A lower value results in more energy supplied to the target material per unit area, as the overlap is single pulses is significantly higher. Mark speed values can be set for the intended job, and range from 1 mm/s to 2000 mm/s.

The laser jump delay parameter describes the waiting period required before the jump between two vector scan fields, to give the mirrors a calming period before scanning the next field. This parameter can be varied from 1 µs to $1 \text{ x } 10^6$ µs, and must be optimally set to prevent too long a processing time at the extremes or too short that results in oscillations in the beam's excursion on the next vector field or structure.

The laser jump speed dictates the speed of the mirrors when jumping between vectors when the laser shutter is closed. Values can be between 1 mm/s and 6000 mm/s.

The tool repetition rate describes the number of excursions for one job routine, while the z-offset parameter adjusts the laser focus deeper into the material during the machining process.

Additional scanning head parameters include laser off/on delay and the mark delay time sequence. These parameters were tuned and provisioned after installation, and it is recommended that they remain unchanged as they impact on laser mirror shutter opening and close times. These parameters when improperly adjusted can result in omissions in vector structuring, long processing periods and misalignment of the beam travel path for general work [96].

The laser off delay which indicates how long the waiting period would be at the end of a vector or a sequence of vectors before the shutter is closed for the next vector jump. It is recommended that this remains at 100 µs. A long delay results in burrowing at vector endpoints, while an insufficient delay period results in uncompleted portions of a vector.

The laser on delay parameter represents the waiting period at the end of a vector or a sequence of vectors before the laser shutter is closed for the next set of vectors, and is set at installation to be 50 µs. Too long a setting, results in missing portions of the vector at its start, whereas too short a setting results in additional ablation or burrowing at vector trace start points.

The mark delay, set at 600 µs, represents the waiting period at the end of the sequence of a vector and is required to compensate for tracking errors. Too short a setting results in a drag and excisions at the tail end of the structure, with observable looped trails, representative of the laser beam travel handoff path en route the adjoining vector. Too long a setting translates to longer than normal processing times, and attendant cost in yield and machine productivity.

5.1.1.1.1 Optimization of laser parameters

The LPKF Protolaser U3 was used to fabricated the copper cladded FR4 CPW transmission lines, Aluminium foil MEMS upper membrane members, and microlithography masks. As indicated, in the preceding section, the aforementioned parameters require optimization for each production phase as they relate to different work materials, pitch, tool path assignments, and libraries. Thus with these requirements, it is meet to set guidelines for each job phase for a set of optimal parameters. These goals were defined in line with the thrust of this work, and include:

1) The degree of accuracy of the structured geometric features relative to design, without marked degradation of the fabricated device response.
2) Repeatability of the fabrication routine with each job phase.
3) Reasonable turnaround times and yields for each job routine.

For each MEMS device structure member, test patterns were used to evaluate and optimize these parameters for the laser hatch and contour job phase definition modes with the use of computer-aided manufacturing (CAM) suites, LPKF CircuitPro PL 2.0™ and LPKF CircuitMaster™ toolkit libraries, via each software's graphical user interface (GUI). Each workpiece material was held in place on the work table by appropriate suction pressures. Initial processing of the geometric pattern CAD import was executed via a laser phase fields assignment CAM application called the LPKF CircuitPro PL 2.0™. This stage plays a crucial role in the microstructuring production phase sequence as this is where the laser work assignments take place, with chosen field scan values and insulation channel widths. This software takes the imported CAD data layers, and converts it into individual production process steps for the laser

excursion routine, which includes contour, hatch, text, silkscreen, heat, preheat

A structuring and rubout process consists of the assignment of a reference line segment in the CAD layout to a layer in the LPKF CircuitPro PL 2.0™, preferably the board outline layer. Then the vector or geometry to be structured is assigned to another work layer preferably the top layer. In the structuring, ablation or rubout process, a contour is generated around these two layers, and the insulation width defined, as the first sequence of steps. For this work, the width was set to 18 µm, slightly higher than the beam minimum diameter to minimize instability in the job execution phase. The next step dictates the outcome of the intended laser job, which can be rubout or just basic contour structuring. The latter is suited for very thin workpieces like the Al foil employed for the MEMS bridges, while the former is the preferred option for the copper cladded FR 4 substrates. With simple laser contour structuring, the location of the cut can be set to be inside or outside the initial contour line segment around the vector. The former implies that the laser beam heat radius is positioned close to the vector, while the latter is located away from the vector, at just after the contour segment line. Contour routing on the inside can result in excess loss of the material and is favoured if accuracy is not desired, while the outside contouring allows for minimal material loss. It is defined by a channel width which is set during the contour routing stage and it ensures that the target vector is at a bordered distance from the laser heat during the execution of the contour phase. For this work, the external contour routing for the Aluminium sheets was adopted, and the channel width was set to 30 µm, twice the minimum laser beam diameter, which resulted in two contour line fields outlining the width defined at the vectors. This value was chosen to ensure a constraint on the beam overlap during the job phase, resulting in the region being exposed to sufficient heat needed for the cut, while also minimizing excessive loss of the Al material.

In the rubout method, the entire region between the assigned top layer (geometry or vector) and in our case, the board external outline layer is removed. Here the hatching grid and length are specified in the software and they describe the density of the LPKF heat, precut, short heat, and contour phase lines to implement the ablation of this target region. In our case, the hatching grid was set to 100 µm, strip width was set to 50 µm, half the amount of the grid, and grid phase length set to 5 mm. Too small a grid width implies the heat generated would be clustered in one region which would lead to a damage of the workpiece with burrowing into the dielectric by the laser. The

length specifies the phase line length for each grid and travel of the laser. With these parameters defined, the laser phase grid is generated and is used for the ablation of the workpiece in one excursion. This rubout is repeated throughout the material as the laser travels throughout the grid. For multilayer job cycles, top and bottom laser contour routing and insulation layer scan fields can be distinguished into the separate structure and rubout phases, and the processed file output assessed for consistency, breaks, and layer misassignments before transitioning to LPKF CircuitMaster™, which interfaces the assigned laser fields to job routines and tool libraries for the laser machine. In this work, laser structuring was designed for a single layer, the top layer, and the tool library was specified for each work material and its associated rubout/structuring depth. A description of the output of the LPKF CircuitPro PL 2.0™, for the rubout of regions surrounding a rectangular vector with delineations by the LPKF laser structuring phases, is shown in Fig. 5.3

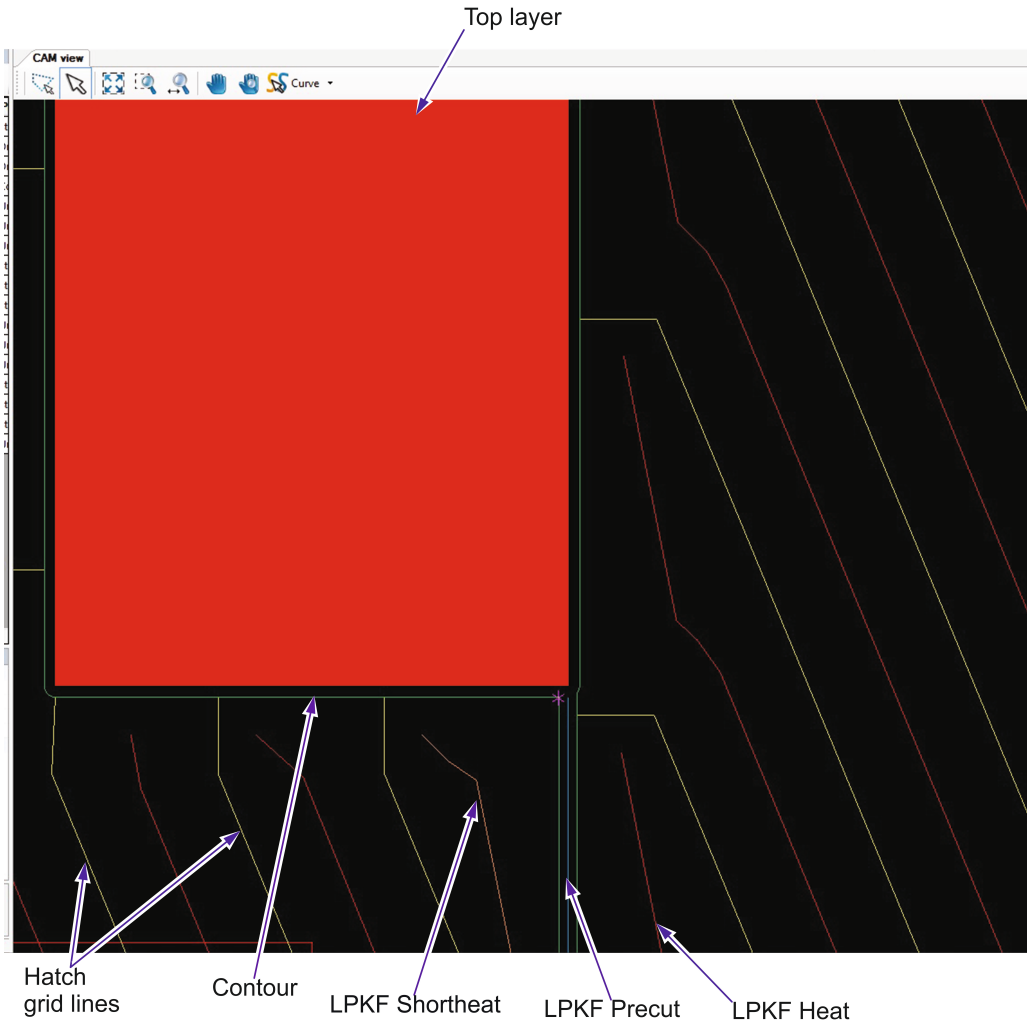


Figure 5.3 LPKF laser structuring phase lines and grid.

In the LPKF CircuitMaster™, placement of the imported project (.lmd file) to a fitting location on the laser scan field for optimal management of the work

material is executed with the use of X/Y/Z chuck table GUI controls. The pilot beam is then used to acquire the specified work area origin before the onset of the ablation process. Monitoring of the structuring process is facilitated by the camera, and at the end of each job phase, the structured material is assessed to gauge the structured output dimension relative to design.

A list of track widths and pitches were employed to optimize the laser work parameters for the 14 μm Aluminium foil, CPW transmission lines, and the 100 μm Aluminium sheet. Test workpieces shown in Fig. 4.4, with dimensions indicated in Table 5.2, were selected for each workpiece material, such that they closely mirrored designed MEMS structures. This was to allow for both performance evaluation and tooling of the LPKF ProtoLaser U3 for the job in view. To make for an accurate description of a measure of the shift in variation in the measured error between these fabricated species and their target specification, eight samples with accompanying plots were processed. Plots of measured fabricated results relative to design specifications and the standard deviation error bar obtained for both the Aluminium and Copper-based materials for each corresponding set of optimal laser parameters are also presented. A flowchart used in optimizing these set of laser work parameters for each material was developed and is presented in Fig. 5.5.

Table 5.2 Workpiece specifications for optimizing parameters for the LPKF ProtoLaser U3.

Material	**Design width value (μm)/Symbol**		**Target length value (μm)/Symbol**	
Aluminium test strip	55	S_w	980	S_l
Aluminium test switch bridge	600	w	800	l
Aluminium test suspension width	45	A_x	140	A_y
Copper test short strips	55	C_w	12.18 mm	C_l
Copper test signal line	430	S	22.42 mm	L
Copper clad FR4 space	70	G	22.42 mm	L

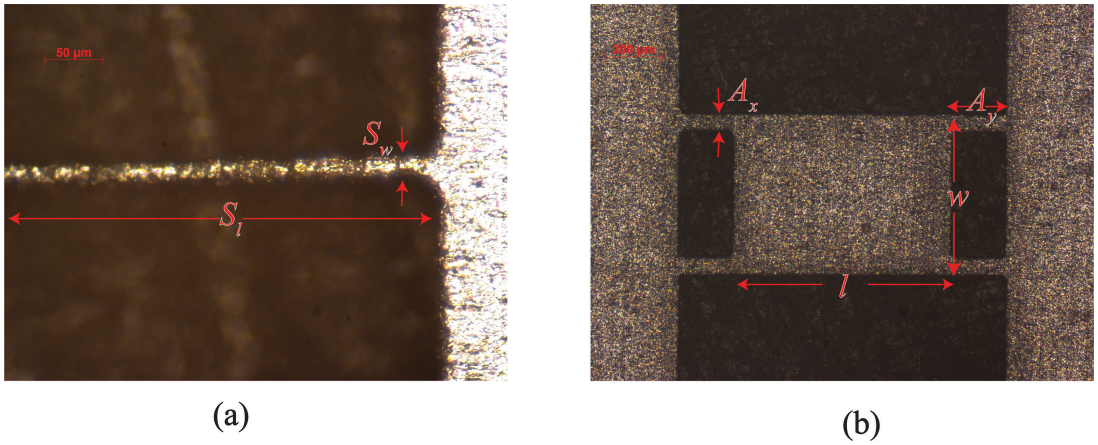


Figure 5.4 (a) Aluminium strip and (b) bridge used to optimize laser parameters.

By employing the laser job optimization flow chart in Fig. 5.5, an optimal set of parameters for the Aluminium based structures were derived and are indicated as 2.5 W laser power, pulse frequency 50 kHz, jump delay of 1000 µs, jump speed of 1000 mm/s, mark delay of 600 µs/s, mark speed of 350 mm/s. These parameters were used to fabricate the test Aluminium workpieces, and measurements of these fabricated workpieces satisfied the aforementioned goals. The measured fabricated geometry list for the test workpieces is reproduced in Appendix A.

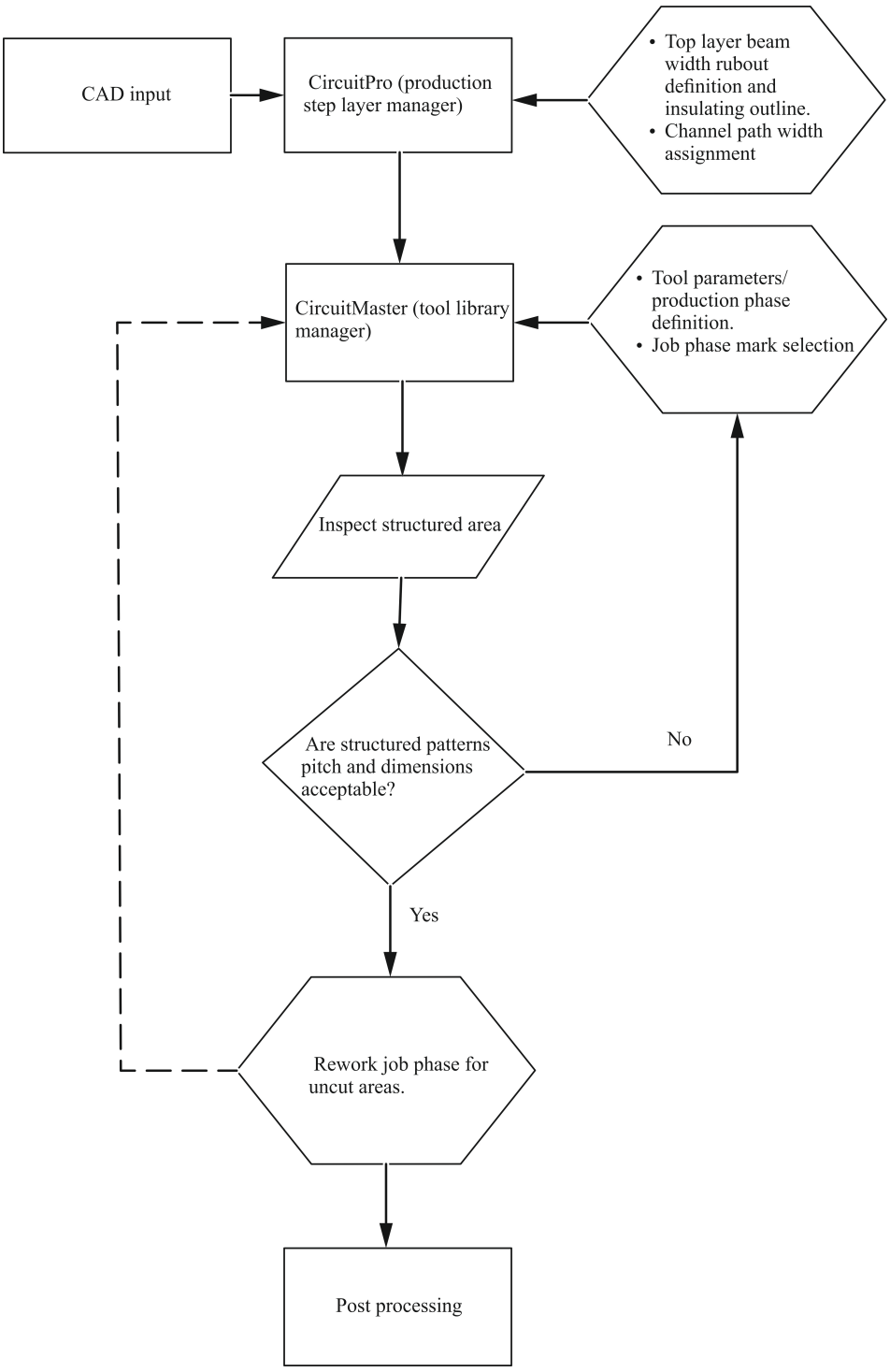


Figure 5.5 Flow chart for optimizing laser job tool parameters.

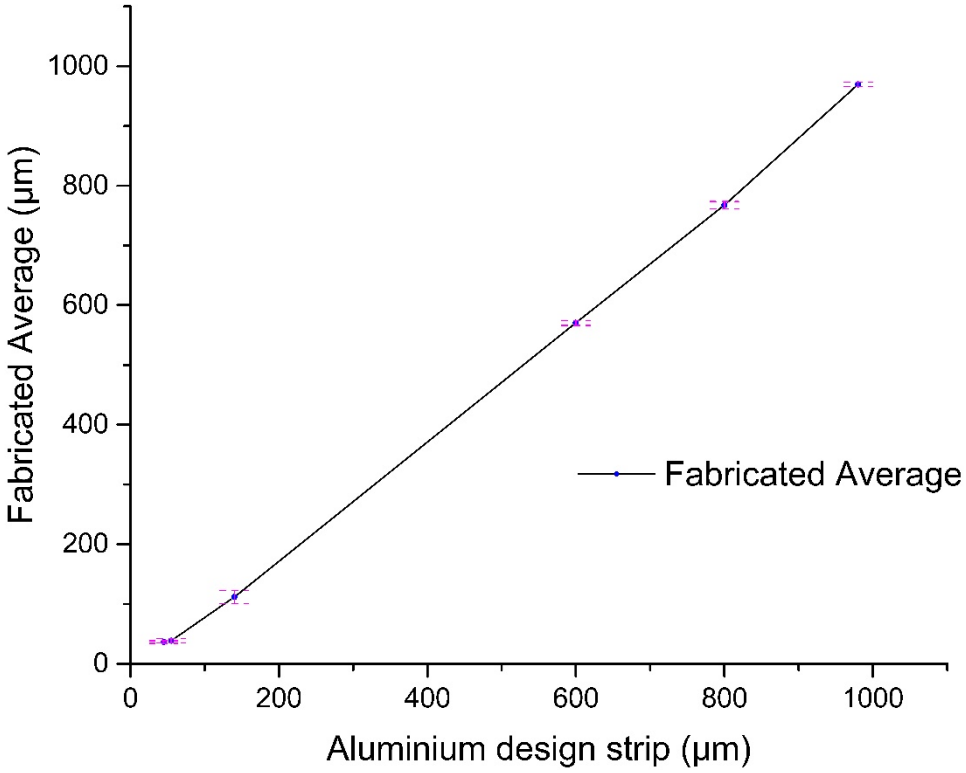


Figure 5.6 Plot of fabricated and error bars vs design specification for Aluminium strip workpieces under the condition of power/mark/pulse: 2.5W/350 mm^{-1} /50 kHz.

The corresponding plot in Fig. 5.6 shows the relationship between fabricated measurement results and error bars vs. design dimensions for sets of Aluminium strip workpieces shown in Table 5.2. From the plot, we can deduce, a linear congruence in the relationship between design and fabricated dimensions. Deviations are indicated in by error bars with an average of 3.44 % across test dimensions with the laser parameters, lending credence to the aptness of the parameters devised. Equally relevant to these set of parameters is the indicated repetition rates, N, adopted as separate metrics for the 14 µm foil, and the 100 µm Al sheets used for the microlithography masks. For the former, this value was pegged at 1, while for the latter the cycle of repetitions was set to 10.

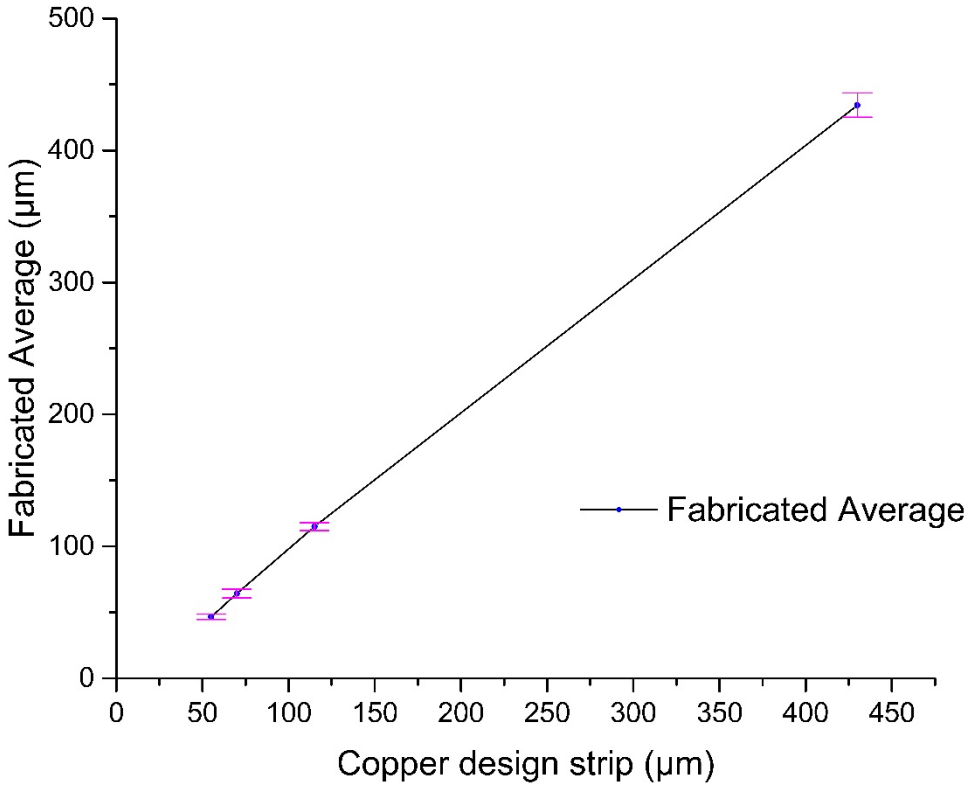


Figure 5.7 Plot of fabricated and error bars vs design specification for Copper strip test workpieces under the condition of power/mark/pulse: 5.2 W/400 mm^{-1} /60 kHz.

By the same token, an optimal routine for Copper strip workpieces were devised and laser job parameters are were obtained as 5.2 W laser power, jump delay of 1000 µs, jump speed of 1000 mm/s, mark delay of 600 µs/s, mark speed of 400 mm/s, and with number of repetitions set to 3. The plot showing the trend between measured fabricated CPW geometries and standard deviation error bars vs. design plot dimensions is indicated in Fig. 5.7. Deviations are indicated in by error bars with an average of 3.33 % across test dimensions with the laser parameters.

5.1.2 Spin Coater and UV curer

The underlying principle governing lithography and the requirements of both deposition and curing of the photosensitive polymer (photoresist) has been discussed in chapter two. In this work, the deposition of the epoxy novolac (SU-8) photoresist was facilitated by a relatively inexpensive solution with the Chemat KW-4A-CE™ spin coater, and curing of both photoacids activated, epoxy polymer ADEX™ thin sheet films and the SU-8 photoresists achieved with the Chemat KW-4AC UV™ curer. Both types of equipment are presented in this section, alongside methods used to derive optimal process routines.

5.1.2.1 Chemat KW-4A-CE™ spin coater characterization

The Chemat KW-4A-CE™ is equipped with a two-stage spin process allowing for dispensing the polymer onto the substrate in the first slower stage revolutions, followed by homogenization of the polymer coat on the second stage at higher speeds. Control and monitoring of these two-stage speeds are facilitated by separate timers defined for present cycle times and LED speed indicators. The first stage speed can be set to run from 500 rpm to 2500 rpm, and the timer a period between 2 s and 18 s. The second stage speed can also be defined from 1000 rpm to 8000 rpm, with a timer that can be set to run between 3 s and 60 s. Suction pressure is provided by a standalone 4 kW motor, through flexible tubes attached to the coater. The wafer or substrate is secured on a 4-inch diameter cross patterned grooved type Aluminium vacuum chuck. The substrate-vacuum chuck-rotor shaft assembly is housed in a Teflon®-coated stainless steel bowl, offering protection from displaced fluids and runaway substrates on the fly.

The resist is manually applied at the centre of the substrate with the aid of a syringe, and optimal spin speeds recipes for both stages developed from the Microchem speed vs. film thickness curve and process guideline template for the SU-8 2002 [97]. Speed adjustments were made after measurements of the deposited SU-8 coat thickness was obtained with the stylus-based step profiler, the KLA-Tencor Alpha-Step IQ™ Surface Profilometer. The first stage provides for even spread of the resist, and the thickness of the coat determined by the second stage spin speed. To obtain a 1 μm thick SU-8 2002 coat layer, the application recipe consists of 2 mils in the centre of a 2-inch wafer, followed by initial spin speeds of 500 rpm for 10 s, and final ramping to 4000 rpm for 30 s. The optimized routine is aided with substrate preparation and dispensing techniques that ensure:

1) A minimization of pinholes and comet surfaces through prior cleaning with acetone to remove organic impurities, followed by rinsing in isopropyl for the contaminated acetone, and storage in deionized water.
2) A promotion of the SU-8 resist's adhesion to the substrate via initial baking at 100 ℃ for 3 mins.
3) An elimination of chuck marks though equalization of temperatures between the resist, substrate and chuck surface.
4) The elimination of uncoated areas with the centralized placement of the resist.

5.1.2.2 Chemat KW-4AC UV™ curer characterization

The Chemat KW-4AC UV curer is a relatively inexpensive solution for facilitating the curing of photoresists. It is equipped with four 6 W low-pressure mercury UV (365 nm) lamps, and a 4-inch chuck rotating at 6 rpm to make for uniform curing. The resist coated substrate is placed on the chuck, and the interlock door works with the UV switching system to prevent accidental exposure during operation.

Theoretical UV exposure times were obtained after calculations of the intensity (I) with the OAI handheld 308 UV™ Light Meter, and adjustments with dosage (D) recommendations provided in [94] for indicated resist thickness and substrate types exposure energies. The relationship between the exposure energy and intensity is given by D= It, and for copper clad based substrates, the minimum dose is expected to be twice the recommended Si substrate specified amounts. These values are indicated for 0.5 to 2 microns and 6 to 15 microns resist thickness to be $80\ {}^{mJ}/_{cm^2}$ and $140\ {}^{mJ}/_{cm^2}$ respectively. The UV intensity of the Chemat KW-4AC UV curer were derived from the mean of five measurements shown in Table 5.3.

Table 5.3 Chemat KW-4AC UV curer intensity measurements.

UV intensity	Measurements (mW/cm^2)					Analysis	
	1	2	3	4	5	Average	STD
	0.39	0.32	0.28	0.27	0.35	0.322	0.04977

Thus the recommended exposure time for the 1 μm and the 6 μm final multilayer photoresist deposits are, $(160 / 0.322) \cong 9\ \text{mins}$, and $(280 / 0.322) \cong 15\ \text{mins}$ respectively.

This theoretically determined recommended value required validation and adjustment in concert with other lithography process factors. Designs of experiments are the preferred route to optimizing process variables, with one factor a time (OFAT) and statistically driven experiment environments most commonly employed [98]. Work reported in [99] adopted the OFAT optimization route with stepped exposure regulation and UV diffraction minimization techniques at the coat to mask interface for strict control of dosage times. In [100], the optimum exposure period for high resolution and low aspect ratio patterns was established to be dependent on an interplay of other lithography process parameters. A derivative of the statistically driven experiment based on Fisher factorial run, the Taguchi statistical methodology, was used to obtain an optimum range of the process parameters. The Analysis of variance (ANOVA) of the process parameters was used to

interpret the experimental results, and requiring decisions as to what parameter factor needs promoting or demoting [98, 101]. A matrix of significant factors and their respective levels were identified and set to optimum levels, followed by a confidence interval calculation, and finally, Taguchi method confirmation tests are to verify the results obtained. This work employed the ANOVA statistical method in identifying percentage contributions of key parameters, prebake, expose, postbake, develop, for observable resist pattern characteristics in the lithography process, and recalculations based on the outcome of the Taguchi array response SNR ratio. A breakdown of the Taguchi optimization procedure is discussed in section 5.2.2.1.

5.2 Fabrication process

The MEMS fabrication techniques employed is based on rapid prototyping and layered manufacturing processes. The capacitive shunt switch and varactor designs have been discussed in chapter three, alongside characterization, tooling, and optimization of the process equipment to be used. The fabrication process is primarily developed and optimized for MEMS devices on PCB, with the prospect of extension into Monolithic Microwave Integrated Circuits (MMIC). Both MEMS devices are fabricated from high purity 14 µm thick Aluminium foils, mounted above laser etched CPW transmission lines on FR4 substrates. The build cycle consists of three key stages: MEMS top members and substrate structuring, MEMS lithography and dry film emboss process layer and the integration process. The fabrication process employed readily available materials in all three stages and includes Aluminium foils, sheets, copper clad FR4 substrates; antimony-free photoacid ADEX dry film sheets, Glycidyl-ether-bisphenol-A novolac (SU-8); organic solvents, Propylene Glycol Methyl Ether Acetate (PGMEA) and Cyclohexanone.

5.2.1 Laser structuring fabrication process

In line with the thrust of this work, we adopted laser ablation technique to realize, micro-structuring of 14 µm thick Aluminium foils for the MEMS device membranes, the 100 µm thick Aluminium sheets employed as lithography masks, and CPW transmission lines on copper cladded FR4 substrates. This method was adopted due to its relatively low cost, reasonably high yields, and a short turn around period.

The operation defining the laser structuring routine consists of a sequence of steps indicated as follows. The first step in the fabrication sequence is to

prepare the workpiece for laser etching and structuring. Dry air was employed as cleaning agents to remove dirt and surface impurities on all materials, thereafter the board start point and material thickness was scanned by a pilot diode beam. This was followed by a scan of the job phase start point, alongside alignment of the board along the x, y, and z-axis, via positioning and travel by the pilot beam, first at the origin of chuck and at target workpiece. Manual adjustments in the alignment of the workpiece, relative to the laser focus beam, are controlled via the LPKF CircuitMaster 1.0™ project move

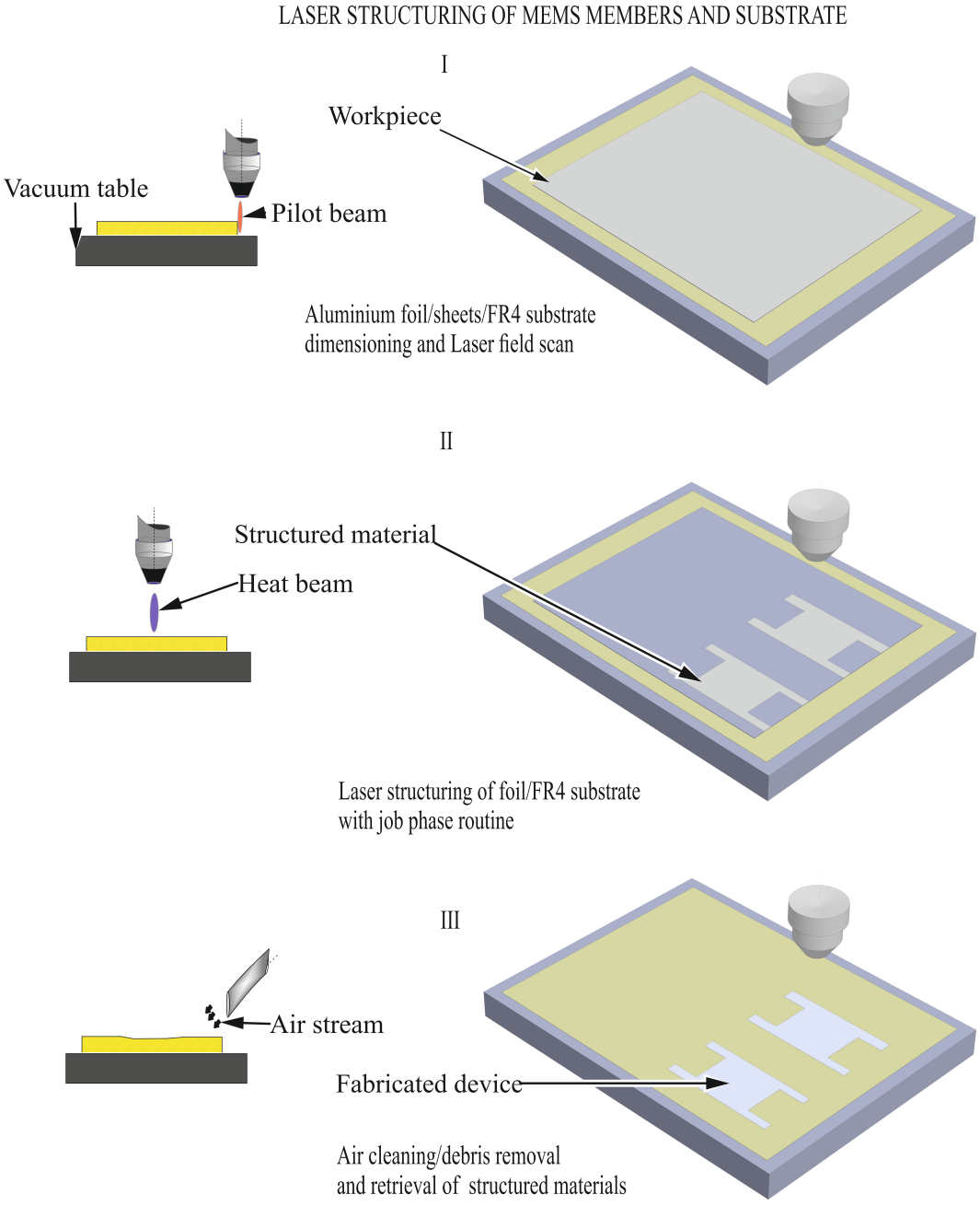
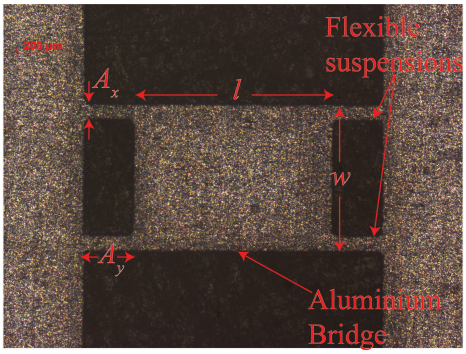


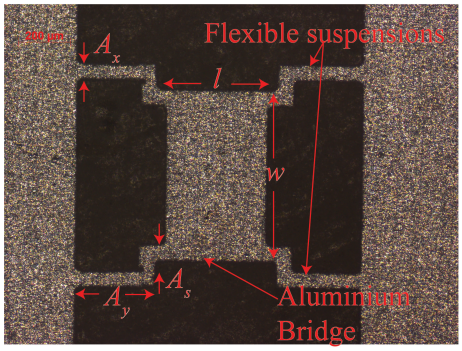
Figure 5.8 Laser structuring process for MEMS members/lithography masks and FR4 substrates.

GUI key and facilitated by the servomotor powered gear system for the X/Y/Z travel. During this travel, the workpiece was held in place with vacuum suction pressure applied to the chuck.

The MEMS members and substrate structuring process is indicated is illustrated in Fig. 5.8. For each material workpiece, the optimum job laser production parameters derived in section 5.1.1 describing the laser and machine work excursion schedule were employed. The production sequence was obtained from the processed CAD in the LPKF CircuitPro PL 2.0™, which contained laser work field allocations, prior to their assignments as job and project toolkit routines in the LPKF CircuitMaster 1.0™. The fields included pre-heating and cutting of the target scan field in the precut phase and an excision border work between the rubout and insulated regions for the contour field function. This was complemented by the material heating and ablation of the scanned target area with the heat fields in generated hatch grid. During the laser ablation process, a stream of high-pressure air cleared the debris and minimized the possibility of contamination from ablated material re-solidification, and redeposition. The next step consists of the workpiece extraction phase, where a final flush of high-pressure air was fed on to the



(a)



(b)

Figure 5.9 Fabricated MEMS bridges for shunt a) switch and b) varactor, with laser parameter conditions: power/mark/pulse/air pressure/repetitions (N): 2.5W/350 mm^{-1} /50 kHz/1 bar/1.

work and vacuum table and the suction pressure disengaged, to make for pick-up of the end target MEMS device/mask/CPW transmission line.

A summary of the work parameters employed for each workpiece and snapshot of the fabricated member is indicated in Fig. 5.9 a) Aluminium switch bridge and b) Aluminium varactor bridge. Fig. 5.10 a) and b) also show the fabricated lithography masks and CPW transmission lines respectively. A comparison of measured and fabricated design dimensions are presented in tables 5.4 and 5.5. These measured fabricated dimensions for the Aluminium switch and varactor bridges, lithography masks, and CPW transmission lines are averages from five separate runs with standard deviations consistent with values reported in the optimization cycle for each material employed as indicated in section 5.1.1.

Table 5.4 Comparison of dimensions of design and fabricated Aluminium switch and varactor bridges.

Symbol	MEMS device geometry	Switch		Varactor	
		Design (μm)	Fabricated (μm)	Design (μm)	Fabricated (μm)
l	Bridge length	800	772	450	414
w	Bridge width	600	567	700	685
A_x	Suspension width	50	46	50	45
A_y	Suspension length	140	127	140	129
A_S	Thigh length	N/A	N/A	50	44

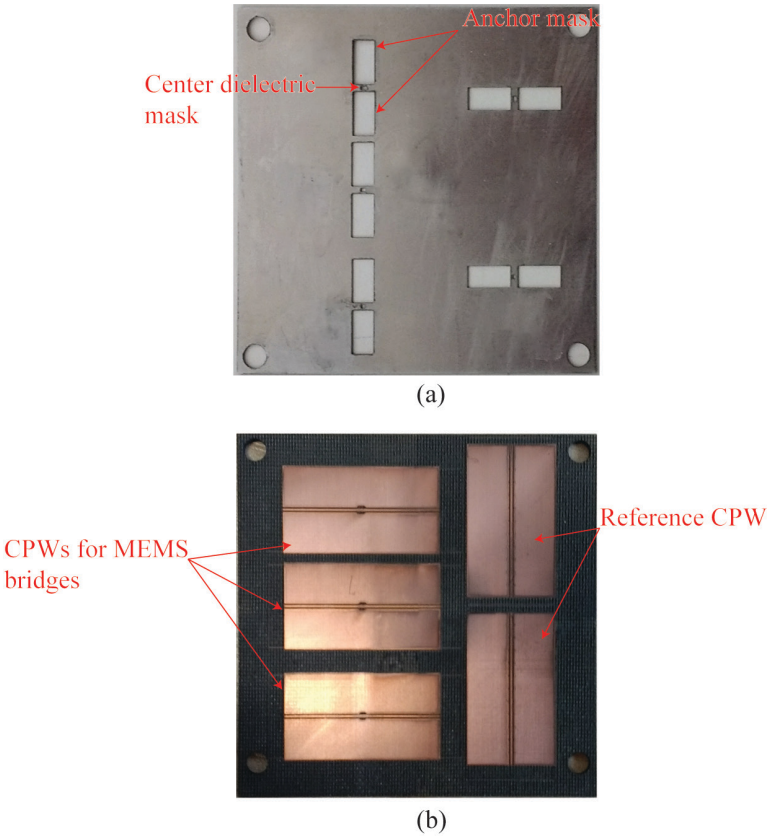


Figure 5.10 Fabricated lithography a) mask and b) CPW transmission line with laser parameter conditions: a) power/mark/pulse/air pressure/repetitions (N): 2.5W/350 mm^{-1} /50 kHz/6 bar/10; b) 5.2 W/400 mm^{-1} /60 kHz/3.

Table 5.5 Comparison of dimensions of design and fabricated MEMS switch and varactor lithography and CPW parts.

Geometry	MEMS switch lithography and CPW parts		MEMS varactor lithography and CPW parts	
	Design	Fabricated	Design	Fabricated
Anchor mask length	600 μm	581 μm	700 μm	689 μm
Anchor mask width	250 μm	241 μm	250 μm	238 μm
Center dielectric mask length	600 μm	583 μm	700 μm	686 μm
Center dielectric mask width	460 μm	445 μm	460 μm	448 μm
CPW signal width	460 μm	449 μm	460 μm	451 μm
CPW gap	65 μm	61 μm	65 μm	62 μm
CPW signal line length	22.42 mm	22.414 mm	22.42 mm	22.416 mm

5.2.2 Lithography and the ADEX film fabrication process

The lithography and the dry film lamination fabrication process made for SU-8 patterned centre dielectric layers and embossed ADEX™ thin film polymers patterns for the bridge anchor support. The reported process consists of an adaptation of wet bench fabrication processes with dry film embossing techniques, to implement multilayer microstructures with high adhesion properties with faster implementation cycles when compared to standard cleanroom processes.

SU-8 originally developed, and patented by IBM-Watson Research Centre (Yorktown Height-USA, US Patent No.4882245 (1989) and others), is composed primarily of polyfunctional epoxy novolac resin EPON Resin SU-8, sold by Shell Chemical, dissolved in an organic solvent, gamma-butyrolactone (GBL), and triarylium-sulfonium salts (CYRACURE® UVI from Union Carbide), which acts as photoinitiator. These salts are approximately 10 wt % of EPON SU-8 [102, 103]. Alongside GBL, cyclopentanone is also used as a solvent for the SU-8 2000 series, and in both, the quantity of the solvent determines the resin viscosity, which ultimately determines final thickness of the spin-coated film. SU-8 resist is currently commercialized by the company MCC (Microlithography Chemical Corp.) under the name NANOTM XP SU-8. The SU-8 2002 resist is reported as possessing a viscosity of 45 centistokes (cSt) [104, 105].

SU-8 epoxy resins are catatonically polymerized by the photoinitiator which generates a strong acid upon exposure to ultraviolet light (365 to 436 nm), with the acid facilitating polymeric cross-linking reactions during heat treatment referred to as the post-exposure bake (PEB). Thus the exposed resist contains the acid catalyst, while the unexposed resist is devoid of this catalyst. This heat treatment is necessary as the kinetic reaction of the cross-linking mechanism is slow at room temperature, which is lower than the resin's glass transition temperature T_g=55 °C. The transition temperature is the temperature at which the transition between solid glass and viscous fluid occurs. Cross-linking, however, does not occur in the absence of this photoacid, at the temperature of the PEB. The cross-linking reaction catalysed by the photoacid results in the epoxy groups reacting with similar or dissimilar molecular other epoxy groups and takes place in a "zipping up" fashion. Extensive cross-linking promoted by the catalyst, PEB, and subsequent bakes results in a dense network and a solid film that is insoluble in a developer, which presents a near optically transparent layer with good mechanical and

chemical resistive properties, for various SU-8 product types delineated by the resultant coat thickness [102, 104].

ADEX thin film sheets were developed by DJ DevCorp, and are chemically amplified, i-line sensitive negative dry film epoxy catatonically cured photoresist, which is placed between two protective polyethene terephthalate (PET) film sheets, with thicknesses ranging from 5 μm to 75 μm. It is a modification of the dry thick film sheet series, SUEX [106, 107], with the epoxy layer embossed on to the target material via heat treatment typically in a laminator. The use of ADEX dry film presents lower capital investment and operating costs when compared to a spin coat process.

In this work, a combination of photolithography and hot embossing techniques is used to pattern these polymers, with both cured coatings presenting excellent adhesion to the metallic surfaces, Aluminium, and copper. The process also made for excellent adhesion at the polymer-metallic interface, with strong mechanical properties to boot. Work reported in [107, 108] and [109], provide insight into multilayer applications of ADEX film sheets and in [99, 104] for investigations involving multilayer SU-8 structures. These investigations report on their individual robust mechanical and bonding properties. The combined application of both SU-8 photoresist and ADEX dry film sheets maximizes the benefits from both, with stable adhesion to the MEMS membrane and copper clad transmission lines, and for an inexpensive fabrication process relative to complex deposition methods discussed in chapter two. We propose this combined wet bench lithography and thin film emboss process described in Fig. 5.11, as the fabrication method for realizing patterned SU-8 dielectric and ADEX polymer anchor support layers on the CPW, lined FR4 substrate for the MEMS switch, and in Fig. 5.16, multilayer SU-8 pattern posts for both dielectric and anchors in the MEMS varactor.

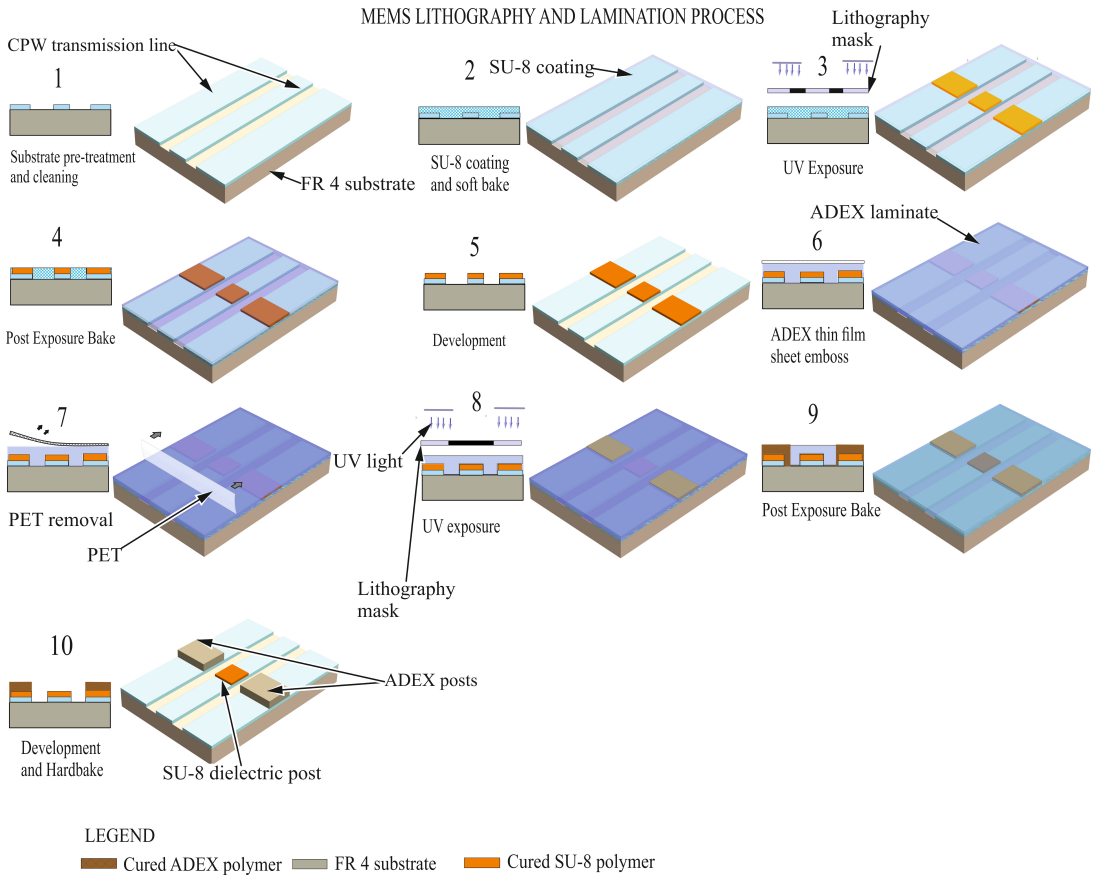


Figure 5.11 Process flow for photolithography and ADEX film emboss pattern fabrication technique for the MEMS switch.

5.2.2.1 Lithography process optimization by Taguchi design methodology

The main challenge with SU-8 processing is its sensitivity to variations in processing variables [101]. It is thus pertinent to optimise the process and derive process parameter values which would make for increased fabrication quality and where possible minimize the costs. With the lithography process characterized by a small number of processing steps and a large range of possible values for each step, the number of experiments runs needed to account for a full factorial of possibilities is prohibitively large. In our case, for four parameters (factors) at four levels initially derived from pilot experiments, a full Fisher factorial would have required a total of 256 experiments (4^4), to fully describe possible conditions.

The Taguchi methodology allows for the optimization of control variables which make considerable contributions towards solving the problem, with the use of orthogonal arrays, desired response defined by the signal-to-noise ratio, and analysis of variance (ANOVA) to determine the contribution of the factors to the indicated response. This technique thus considerably reduces the number of tests needed, with significantly decreased fabrication cost and

time loss for measured response characteristics. The Taguchi method uses a loss function to calculate the deviation between the experimental values and the desired values. This loss function is further converted into a signal to noise (SNR) ratio which minimizes the effects of factors that cannot be controlled. It is the measure of the response of the design experiment when noise factors are present. This ratio consolidates repetitions and the effect of noise levels into one data point, with a subsequent reduction in variation from the identification of significant factors which ascribe required qualities in the desired SNR ratio. In quality engineering and with the Taguchi design of experiments method it is referred to as the Taguchi SNR [98].

There are three kinds of quality characteristics in the analysis of the SNR ratio, namely the smaller is better, the higher is better, and the nominal the best. For each process parameter level response, y, the SNR ratio is calculated based on the SNR analysis as indicated in equation 5.1 to 5.3 [98],

SNR for higher is better,

$$-10\log\left(\frac{1}{n}\sum_{i=1}^{n}\frac{1}{{y_i}^2}\right) \tag{5.1}$$

SNR for smaller is better,

$$-10\log\left(\frac{1}{n}\sum_{i=1}^{n}{y_i}^2\right) \tag{5.2}$$

SNR for nominal is better,

$$-10\log\left(\frac{\bar{y}^2}{s^2}\right) \tag{5.3}$$

where, n is the number of tests in one trial, and $\bar{y}$, is the response mean, s, is the standard deviation of the response data set.

The orthogonal array (OA) is defined by special properties, allowing for conducting a minimal number of runs which provides full information on all the parameters that affect the performance response. These properties include parameter level settings that appear an equal number of times, and this is referred to as the balancing property. All level values are used for conducting the process experiment or runs. In addition, the array of each factor columns are mutually orthogonal to any other column of level values. In other words, the inner product of vectors corresponding to weights is zero for normalized levels.

In our work, the fabrication process was initially accessed to determine which variables primarily influenced the characteristics of the SU-8 film from

literature and prior experimental information. In addition, four data point levels per parameter were chosen to span the space of possible values. The Taguchi orthogonal array technique required only 16 experiments with the focus on four variables: soft-bake time, exposure time, post-exposure bake (PEB) time, develop time. The time components of these parameters were employed as they allowed for ease of statistically handling and process control, as opposed to temperature and UV dosage.

Two problems associated with the non-optimized process were observed: adhesion to the substrate, where crust appears at the film to copper cladding interface, with the SU-8 structure floating away when left long in the developer; and poor resolution between closely situated patterns with some SU-8 resist straying into the boundary spaces. Thus these measurable or observable responses were chosen as quality characteristics to be optimized: (i) film adherence to the substrate, and (ii) pattern space resolution. The goal was to maximize the adherence of the resist to the copper cladded substrate surface, and adjacent pattern space resolution due to diffraction challenges observed with the mask employed. For example, the patterns were evaluated for adhesion response on a scale of one to ten, with ten being the best. Observable comet pits, pinholes and crusts in the structure meant lower scores. With the resolution response, the measured separation distance between SU-8 patterns was employed for an assessment of the quality of a run.

The most suitable orthogonal array, L16 (4^4), was selected to determine these lithography parameters and to analyse from experimental results the sensitivity analysis of each parameter contribution to output. The lithography process parameters and their levels based on the L16 orthogonal array are indicated in Table 5.6. The L16 orthogonal array used for conducting the experiments is shown in Table 5.7.

Table 5.6 Lithography process parameters and their levels of dimensions.

Parameter	Symbol	Level 1	Level 2	Level 3	Level 4
Softbake (seconds)	A	30	45	60	90
Exposure (mins)	B	8	10	12	15
PEB (mins)	C	1	2	3	4
Development (mins)	D	1.5	2	4	5

Table 5.7 L16 (4^4)Taguchi orthogonal array level design.

A	B	C	D
1	1	1	1
1	2	2	2
1	3	3	3
1	4	4	4
2	1	2	3
2	2	1	4
2	3	4	1
2	4	3	2
3	1	3	4
3	2	4	3
3	3	1	2
3	4	2	1
4	1	4	2
4	2	3	1
4	3	2	4
4	4	1	3

5.2.2.1.1 Analysis of the Taguchi method Signal to Noise Ratio response

Data from the experiment was gathered with a focus on optimizing the signal to noise ratio (SNR) with the higher the better response, as opposed to the mean of observed responses. The SNR optimization is used for the purpose of ensuring the reproducibility and robustness of the fabrication process across many trials. Optimizing the mean only makes for improved output, without the required guarantee of robustness in the fabrication process. The optimization process consists of choosing levels which would require trade-offs in the levels indicated for the SNRs of the observed responses. Hence the result is a compromise and one that makes for the best overall quality for the two measured characteristics. In both responses, higher values are required for quality improvement of the SU-8 film in the fabrication process, and also for lowering run times and hence costs. Thus the higher the better equation was employed for the calculation of the SNR ratio. Tables 5.8 and 5.9 shows the values of the SNR ratios for observations of the adhesion response indicator and measured pattern resolution distance for three runs per experiment.

Table 5.8 Results of experiments and Taguchi SNR for adhesion quality.

Experiment	Process Factors				Adhesion 1	Adhesion 2	Adhesion 3	SNR (dB)	Mean
No.	Softbake (s)	Exposure (mins)	PEB (mins)	Development (mins)					
1	30	8	1	1.5	4	5	4	12.596	4.333
2	30	10	2	2	6	7	7	16.408	6.666
3	30	12	3	4	7	6	6	15.965	6.333
4	30	15	4	5	5	6	5	14.446	5.333
5	45	8	2	4	3	4	3	10.227	3.333
6	45	10	1	5	2	2	2	6.021	2.000
7	45	12	4	1.5	8	9	8	18.377	8.333
8	45	15	3	2	9	9	8	18.716	8.666
9	60	8	3	5	3	4	4	11.04	3.666
10	60	10	4	4	4	4	5	12.596	4.333
11	60	12	1	2	5	5	6	14.446	5.333
12	60	15	2	1.5	7	7	6	16.408	6.667
13	90	8	4	2	2	3	3	8.029	2.666
14	90	10	3	1.5	6	5	7	15.317	6.000
15	90	12	2	5	4	4	5	12.596	4.333
16	90	15	1	4	5	5	4	13.233	4.667

Table 5.9 Results of experiments and Taguchi SNR for measured pattern space distance response.

Experiment	Process Factors				Resolution space distance 1 (mm)	Resolution space distance 2 (mm)	Resolution space distance 3 (mm)	SNR (dB)	Mean
No.	Softbake (s)	Exposure (mins)	PEB (mins)	Development (mins)					
1	30	8	1	1.5	0.055	0.041	0.061	-25.999	0.052
2	30	10	2	2	0.064	0.055	0.045	-25.517	0.055
3	30	12	3	4	0.075	0.065	0.055	-23.951	0.065
4	30	15	4	5	0.080	0.072	0.061	-23.138	0.071
5	45	8	2	4	0.090	0.110	0.095	-20.238	0.098
6	45	10	1	5	0.061	0.058	0.073	-24.001	0.064
7	45	12	4	1.5	0.050	0.031	0.025	-30.058	0.035
8	45	15	3	2	0.033	0.021	0.015	-34.054	0.023
9	60	8	3	5	0.110	0.120	0.115	-18.803	0.115
10	60	10	4	4	0.098	0.093	0.085	-20.769	0.092
11	60	12	1	2	0.073	0.059	0.067	-23.665	0.066
12	60	15	2	1.5	0.031	0.023	0.018	-33.023	0.024
13	90	8	4	2	0.099	0.084	0.091	-20.846	0.091
14	90	10	3	1.5	0.065	0.060	0.061	-24.168	0.062
15	90	12	2	5	0.055	0.071	0.064	-24.111	0.063
16	90	15	1	4	0.068	0.062	0.076	-23.355	0.068

Three runs per experiment were executed to minimize the influence of measurement errors and to factor in as much process response variations and characteristics as possible. The average adhesion indicator and resolution distance were calculated to be 5.17 and 0.065 mm respectively. Similarly, the average values of the Taguchi SNR for the adhesion response and resolution distance were calculated and shown to be 13.53 dB and -27.73 dB respectively. Initial analysis of the effect of the process parameters: softbake,

exposure, PEB, and developments were performed with the SNR response table. The SNR response tables for the adhesion quality indicator and resolution space distance is shown in Table 5.10 and 5.12 respectively. The associated mean is also tabulated and presented in Tables 5.11 and 5.13. Both the values are derived from the average of the indicated factor response for the levels described in the orthogonal array, shown in Table 5.7. For example, the effect of Factor A (Softbake), m_{A1}, and factor B, m_{B1}, (Exposure) at level 1 for computed SNR and measured response quality are given respectively as [98],

$$m_{A1} = {(\Pi_1 + \Pi_2 + \Pi_3 + \Pi_4)}/{4} \tag{5.4}$$

$$m_{B1} = {(\Pi_1 + \Pi_5 + \Pi_9 + \Pi_{13})}/{4} \tag{5.5}$$

where Π_i, is the SNR or measured response quality at the ith row specified for the appropriate level in Tables 5.7, employed for corresponding array outcomes in Tables 5.8 and 5.9. The statistical computation software Minitab[5] made possible these SNR experimental data response computations.

Table 5.10 relates the Taguchi SNR ratios with respective factor effects for the adhesion quality response, while Table 5.11 conveys the raw response mean with the indicated SNR value for these lithography parameters. Thus if we were to concern ourselves with just adhesion quality, then the highlighted levels (A1, B4, C3, D1) combination corresponding to 30 s of softbake, 15 minutes of exposure, 4 minutes of PEB, and 1.5 minutes of development would ensure optimal adhesion. Thus choosing all the points with the highest SNR values in Fig. 5.12, would give us the best adhesion quality.

By the same token, if we were concerned with solely addressing the resolution, then the highest SNR combination shown in Table 5.12, (A4, B1, C4, D3) corresponding to 1.5 minutes of softbake, 8 minutes of exposure, 4 minutes of PEB, and 4 minutes of development would make for best discrimination distance between the resist patterns. Hence choosing all the points with the highest SNR values in Fig. 5.14 would give the best discrimination between resist patterns.

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[5]Minitab, Ver. 18, 2014, Minitab, Inc., PA., 2014.

Table 5.10 Response Table for Taguchi Signal to Noise Ratios for adhesion quality (Larger is better).

Level	Softbake	Exposure	PEB	Development
1	**14.85**	10.47	11.57	**15.67**
2	13.34	12.59	13.91	14.40
3	13.62	15.35	**15.26**	13.01
4	12.29	**15.70**	13.36	11.03
Delta	2.56	5.23	3.69	4.65

Table 5.11 Response Table for Taguchi level means for adhesion quality response.

Level	Softbake	Exposure	PEB	Development
1	**5.667**	3.500	4.083	**6.333**
2	5.583	4.750	5.250	5.833
3	5.000	6.083	**6.167**	4.667
4	4.417	**6.333**	5.167	3.833
Delta	1.250	2.833	2.083	2.50

Table 5.12 Response Table for Taguchi Signal to Noise Ratios for resolution discrimination quality (Larger is better).

Level	Softbake	Exposure	PEB	Development
1	-24.65	**-21.47**	-24.26	-28.31
2	-27.09	-23.61	-25.72	26.02
3	-24.07	-25.45	-25.24	**-22.08**
4	**-23.12**	-28.39	**-23.70**	-22.51
Delta	3.90	6.92	2.02	6.23

Table 5.13 Response Table for Taguchi level means for measured resolution distance response.

Level	Softbake	Exposure	PEB	Development
1	0.06075	**0.08925**	0.06283	0.04342
2	0.05517	0.06817	0.06008	0.05883
3	0.07433	0.05750	0.06625	**0.08100**
4	**0.07133**	0.04667	**0.07242**	0.07833
Delta	0.01917	0.04258	0.01233	0.03758

The lithography parameters and levels with matching SNR ratios are also shown in graph forms for both quality response data sets. The SNR response

for the adhesion quality indicator and resolution space distance is shown in Fig. 5.12 and 5.14 respectively. The associated means for the adhesion and resolution space distance are also presented in Fig. 5.13 and 5.15 respectively.

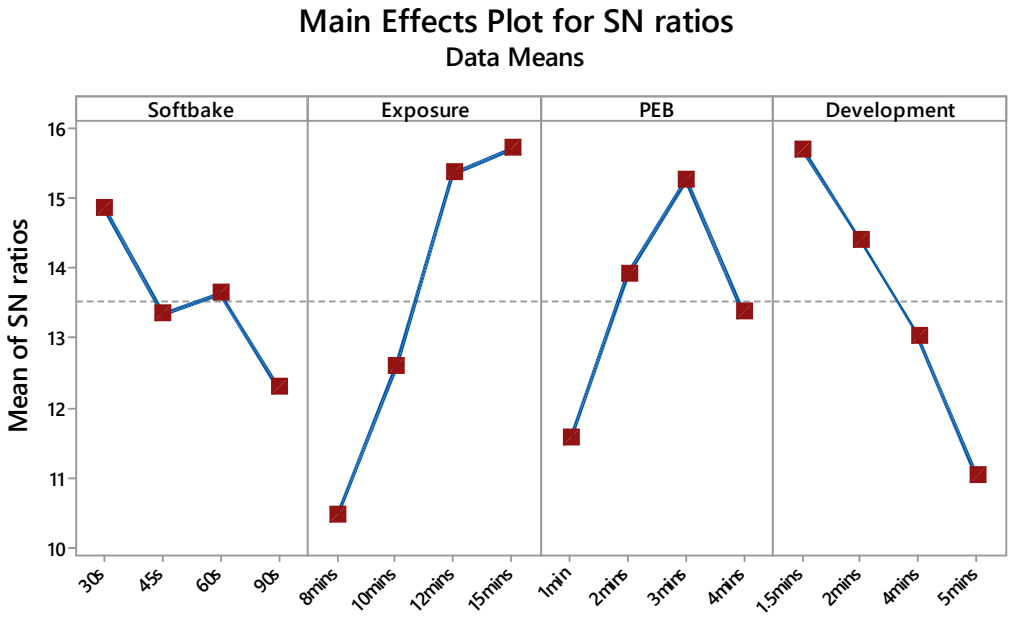

Figure 5.12 Effect of lithography process parameters on average S/N ratio for adhesion quality factor.

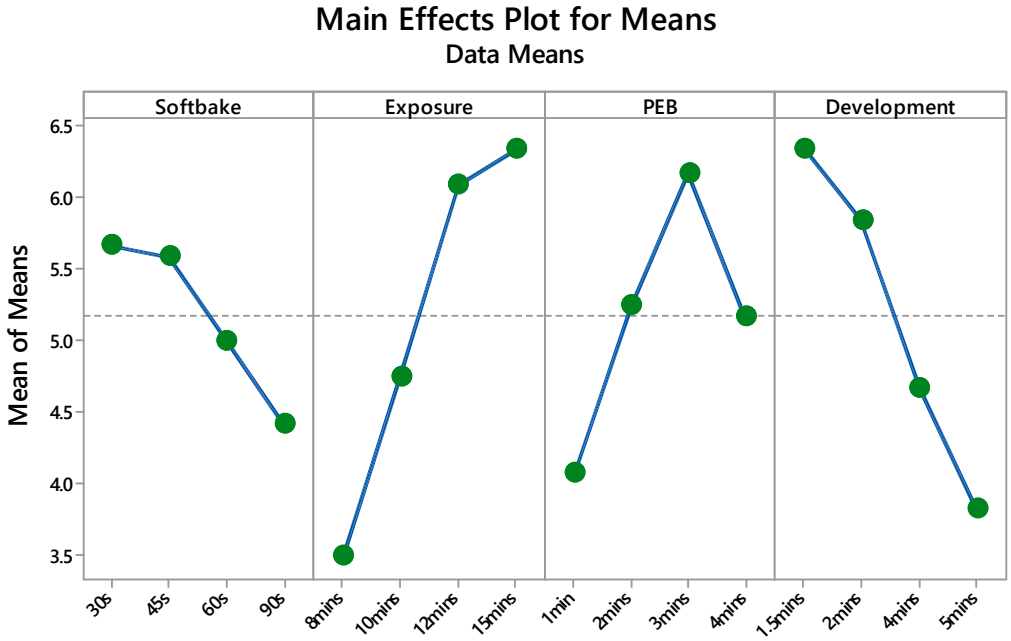

Figure 5.13 Effect of lithography process parameters on average adhesion quality factor.

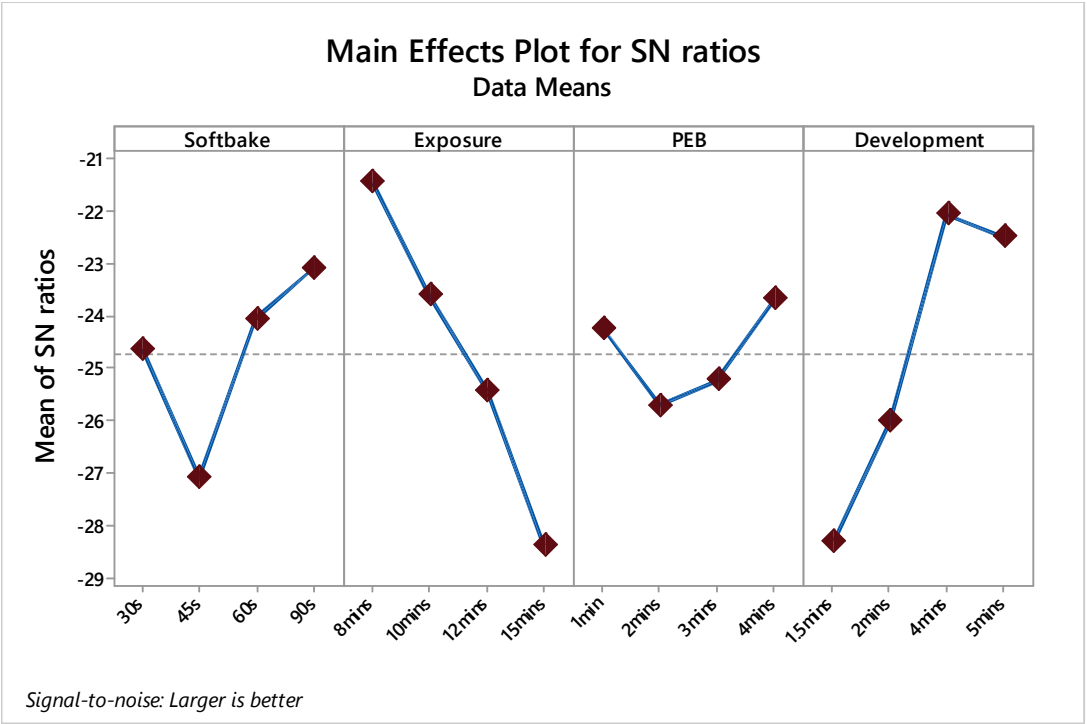

Figure 5.14 Effect of lithography process parameters on average S/N ratio for resolution distance quality factor.

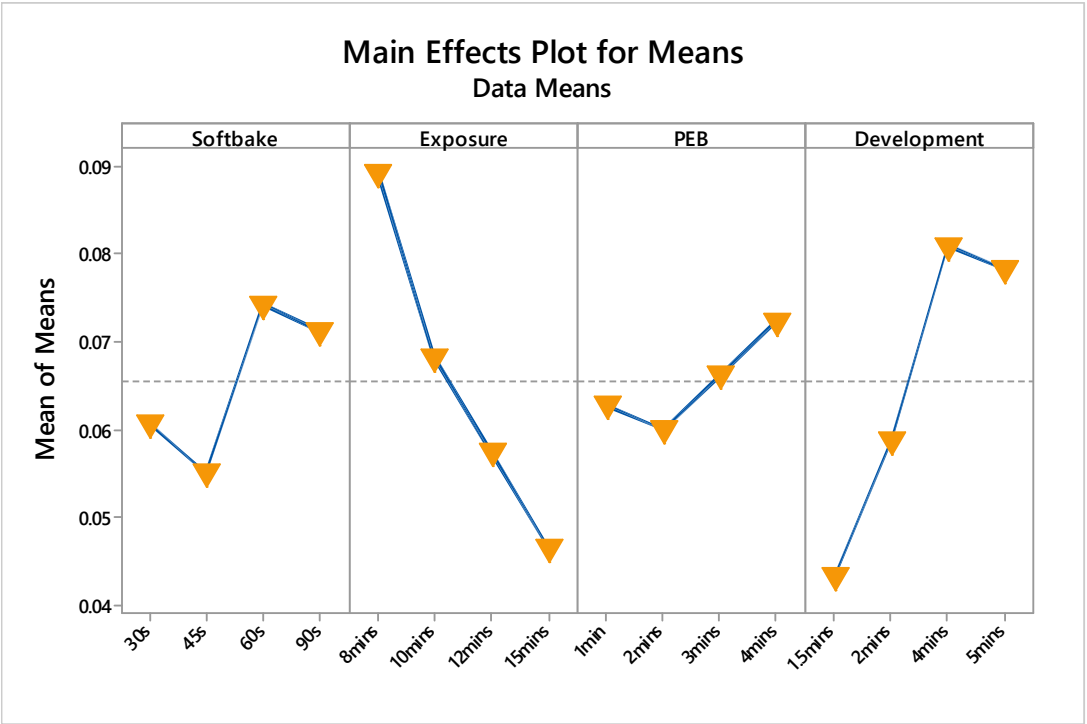

Figure 5.15 Effect of lithography process parameters on measured average resolution distance quality factor.

In addition, the ANOVA statistical analysis method was also employed to determine the individual interactions of all of the control factors, in the

experimental process design. It was used to analyse the effect of the lithography parameters, softbake, exposure, PEB, and development on the adhesion quality and pattern resolution discrimination. The ANOVA results are shown in Tables 5.14 and 5.15 for adhesion quality and resolution respectively. This analysis was carried out at 95 % confidence level and 5 % significance level. The significance of the factors in ANOVA is determined by comparing the F values of each control factor. The last column indicates the parameter contribution in percentage values, which shows their relative influence on the process performance. The ANOVA computation of experimental outcomes was also by the statistical computing software, Minitab.

Table 5.14 Results of ANOVA for adhesion response quality.

Source of variance	**Degree of Freedom (DoF)**	**Sum of Squares (SS)**	**Mean Square (MS)**	***F* ratio**	**Contribution (%)**
Adhesion quality response					
Softbake	3	4.056	1.352	0.92	7.64
Exposure	**3**	**20.611**	**6.870**	**4.70**	**38.81**
PEB	3	8.722	2.907	1.99	16.42
Development	3	15.333	5.111	3.49	28.87
Error	3	4.389	1.463	-	8.26
Total	15	53.11	-	-	100

Table 5.15 Results of ANOVA for resolution response quality.

Source of variance	**Degree of Freedom (DoF)**	**Sum of Squares (SS)**	**Mean Square (MS)**	***F* ratio**	**Contribution (%)**
Resolution distance response					
Softbake	3	0.000965	0.000322	1.43	9.97
Exposure	**3**	**0.003959**	**0.001320**	**5.86**	**40.87**
PEB	3	0.000339	0.000113	0.50	3.50
Development	3	0.003748	0.001249	5.55	38.69
Error	3	0.000675	0.000225	-	6.97
Total	15	0.009687	-	-	100

From Table 5.14, the percentage contributions of softbake, exposure, PEB and development factors on the adhesion response were found to be 7.64 %, 38.81 %, 16.42 %, and 28.87 %. The percentage error contribution was determined to be 8.26 %, from factors not accounted for which can be attributed to the environmental conditions e.g. humidity, and cladding surface conditions. The two most significant factors affecting adhesion were exposure and development. By the same token, the percentage contribution of the process parameters on the resist pattern resolution distance was found to be

softbake (9.97 %), exposure (40.87 %), PEB (3.50 %), and development (38.69 %). Error contributions were computed to be at 6.97 %. These results are conveyed in Table 5.15.

With each theoretical optimal process parameter and response values determined, the optimization process consists of selecting points which results in the best overall quality for both output responses. Hence trade-offs are required with the better value process situated between the test parameter levels. This was also followed by a run to see if satisfactory results are obtained. Modifications were required with reduced test space windows, as opposed to our initial set of parameter levels. The optimization and trade-offs for both responses are better evaluated with the graph form data sets presentation.

Fig. 5.12 shows the adhesion response to the four process parameters and for the indicated levels. We can deduce that softbake (factor A) has levels situated close to the mean, while exposure (factor B) and PEB (factor C), development (factor D) have large variations for all levels, with further swings in excursions exhibited by exposure and development contributions. This implies that exposure and development are especially critical for this response, with PEB coming just after. We can also infer from the plot that levels 2 and 3 satisfy opposite responses when transiting from left to right for exposure and development. We also note that in Fig. 5.14, for the resolution response that exposure, development are also critical for the resolution response output, but in this case levels, 2 and 3 satisfy opposite responses. Thus we can conclude that there is an exposure and a development time level that lies midway, which would satisfy both desired responses and still work for all outputs. So in the validation phase, we employed 11 minutes for exposure and 3 minutes for development to make for the proposed levels values of the process variables shown in Table 5.16. We also note that at these interpolated levels, the process output is not severely impacted, as they are close to the mean.

Table 5.16 Results for optimized lithography parameter levels.

Parameter	Optimum level
Softbake	60 s
Exposure	11 minutes
PEB	3.5 minutes
Development	3 minutes

5.2.2.1 Patterning of MEMS dielectric and support layers on the CPW transmission line

The MEMS switch and varactor bridges obtained in section 4.2.1, are to be integrated to the CPW lined substrate. They required multilayer polymer deposits to make for the desired air gap, and a dielectric layer on the centre conductor to mitigate against stiction. This multilayer requirement for the elevated MEMS membrane exploits a sacrificial layer, with the dominant trend being the use of polyimide materials. Extant cleanroom processes for fabricating sacrificial layers, with adhesion their to the substrate and membrane materials as governing concerns have been discussed in chapter two. Cleanroom deposition methods such as electroplating, chemical and vapour deposition, are employed for metallic sacrificial materials like Cu, Al, Cr, and Ti. While for non-metallic sacrificial materials like polyimides, polymers, polysilicon, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), deposition can be by LPCVD, PECVD, ICPCVD, ALD, spin-dip-spray coating, alongside complementary etching techniques, such as ion coupled plasma (ICP) etching and reactive ion etching (RIE), and selective area masking in lithography. As previously discussed with lithography, multilayer SU-8 resist deposition requires a repeat of the coating process on the substrate alongside curing by UV exposure, such that the number of runs mirrors the number of intended layers. Investigations into alternative sacrificial fabrication methods have been discussed in [110], where selective layer ion treatment of traditional water-soluble polymers, poly(acrylic acid) (PAA) and dextran, impedes their solubility, and hence the ability to remove deselected regions. These polymers were treated with salt solutions (NaOH or NaCl).

5.2.2.1.1 Lithography and ADEX emboss process for the switch

The process employed in this work to realize the dielectric and MEMS support layers for the switch is chosen to be a blend of photolithography and a hot emboss of ADEX thin film epoxy sheets for the switch. Whereas for the

varactor a multilayer SU-8 lithographic process was employed. This process aptly described as the wet bench-dry film press, consists of a transition between polymer depositions via spin coating, to dry film polymer embossing on the substrate. A description of this process would follow for each device. The lithography process to be employed on both copper cladded FR4 substrate and the interfacing MEMS switch membrane has been optimized using Taguchi optimization technique.

The process begins with the treatment of the FR4 substrate and CPW transmission lines, through cleaning by Isopropanol (IPA), and pre-heating to allow for dehydration, and adhesion improvement. Thereafter, the SU-8 2002 resist is applied via a syringe on the substrate centre, and ramped to 4000 rpm, from 500 rpm with the Chemat KW-4A-CE spin coater. This was followed by a trimming of excess beads. The copper clad surface of the FR4 substrate now coated with 1 μm layer of SU-8 2002, is soft baked (prebaked) at 95 ℃ on a hotplate, from a ramped up temperature of 65 ℃. After the softbake procedure, the temperature was ramped down, first to 60 ℃, and then ambient temperature, to minimize stress build up in the polymer molecules as they re-crystallised. Curing was made possible by a flood of 365 nm wavelength UV light provided by the Chemat KW-4AC, with the chuck rotating at 6 rpm to make for uniform exposure, with the resultant cross-linking of the SU-8 polymer molecule. The exposed SU-8 coat was then baked first at 65 ℃, and stepped up to 95 ℃, in the process called post-exposure bake (PEB), which resulted in discernible patterns on the substrate. Development of this coated, exposed and post-exposure baked SU-8 resist layer was done in PGMEA. After which the substrate and coat were rinsed in propanol. The CPW was now patterned with the 1 μm centre dielectric layer and foundation posts for the ADEX support layer. Additional baking of the substrate was conducted at 65℃ and then 95 ℃ to allow for complete curing of this initial posts and patterned centre line dielectric SU-8 polymer layer. Patterning of the MEMS anchor post proceeded with a sacrificial coat of SU-8 2002 resist, which was spun on the wafer, thereafter the ADEX sheet was embossed on to the substrate by feeding both film and substrate into the SKY 335R6 laminator at 0.3 m/min, with the rolls heated to 65 ℃. A thin uniform layer of the ADEX polymer was consequently stamped onto the copper cladded substrate, with this process. Curing of this embossed polymer was also provided by the Chemat KW-4AC UV curer. The wafer was later baked on the hot plate at 85 ℃ from a stepped-up temperature of 65 ℃. This allowed for the polymerization of the anchor post patterns, which would be now visible. The ensuing ADEX polymer patterned substrate was developed by soaking and agitation in

Cyclohexanone. The alignment accuracy achieved between the two SU-8 and ADEX layers was found to be, on average, 69 µm. The complete routine with process times, temperature and a description of how the alignment accuracy was determined are provided in Appendix B.

5.2.2.1.2 Lithography process for the varactor

The approach presented here follows the routine employed in the lithography fabrication process for the switch. The modification adopted for this multilayer SU-8 post section derives from the polymer's intrinsic ability to allow for the deposition of N number of layers, with adjustments in process conditions to achieve the intended microchannel. The process flow adopted is as indicated in Fig. 5.16. A summary of this process follows, with the complete routine with a description of times and temperature employed provided in Appendix B.

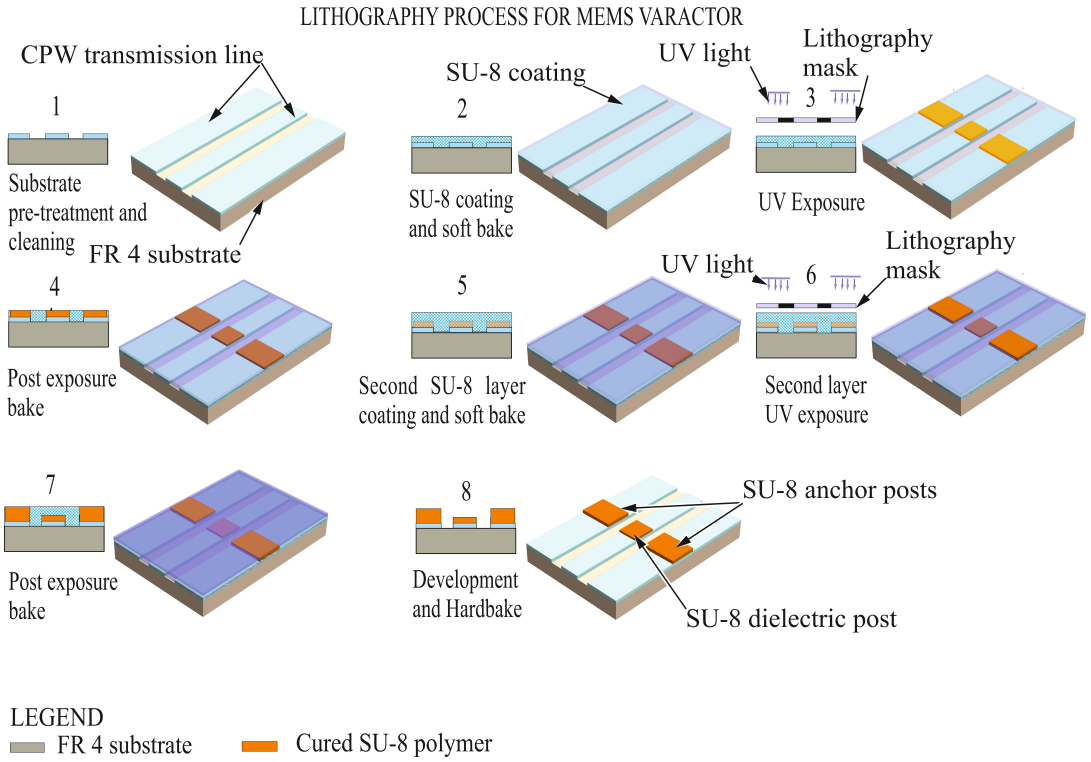

Figure 5.16 Lithography flow for the MEMS varactor multi-layer SU8 posts.

Two millilitres of the SU-8 2002 resist was applied on the FR4 substrate positioned on the Chemat KW-4A-CE spin coater, via a syringe. This was done to make for the centralized spread of the resist, during the spin process. The substrate and resist were spun at 4000 rpm from an initial ramp speed of 500 rpm. Thereafter the substrate was soft-baked on a hotplate at 95 ℃, ramped up from 65 ℃, to reduce the viscosity thus allowing for an increase in the mobility of the polymer molecules to make for increased polymerization. The prebaked SU-8 coated substrate was cured in the Chemat KW-4AC curer, with the flood of 365 nm UV light, and then baked for 105 s, i.e. half the

duration of the single layer deposit PEB time. This reduced duration was to accommodate a furthering of this layer's polymerization with additional PEBs after the deposition of the next layer, while also limiting the diffusion of the solvent of a newly coated layer onto the cured layer. At this point, the centre dielectric post, and anchor initial layer posts were now patterned. An additional layer of SU-8 2002 was applied in the same manner with the first resist deposit with the syringe, and the spin speed set to 4800 rpm, 1.2x twice the speed for the single layer as required for SU-8 surfaces. The substrate was baked at 95 ℃ from ambient temperature, with ramped increases of 30 ℃ for 60 s. This was employed due to the low thermal conductivity of SU-8, and to also allow for the continued polymerization of the lower layer. Thereafter the coated layer was exposed for 15 minutes. The 1 μm extra patterned anchor posts now visible, were baked for 3.5 minutes at 95 ℃ from ambient temperature. The baked substrate was allowed to gradually cool back to ambient temperature. Development of all layers proceeded with agitation of the substrate in PGMEA.

5.2.3 MEMS members integration process

With the MEMS members, bridge, SU-8 resist layers and ADEX support posts CPW transmission lines, now fabricated, integration into a composite MEMS device can proceed for the shunt switch and varactor respectively. The process consists of an alignment of the bridges with the patterned CPW transmission lines. To make for an accurate positioning of the substrate with the MEMS membranes, and furthering the bond into a single assembly, the circular fiducial markers on the components of the device were matched. The integration process that made for the bonding of the MEMS membrane with the board and patterned polymers is as depicted in Fig. 5.17.

A computer numerical controlled (CNC) machined Aluminium block functioned as the holding fixture. Design and modelling were in executed in Solidworks[6], prior to milling with the lathe machine. It was equipped with complimentary circular fiducial markers to provide accurate alignment for the MEMS members. Alignment accuracy between the Aluminium membrane members and the dielectric posts, using this method, was found to be, on average, 49.5 μm. An illustration of how this was determined by the layer to layer registration is presented in Appendix B.

[6]Solidworks, Ver. 2015, Dassault Systèmes, Villacoublay, France, 2015.

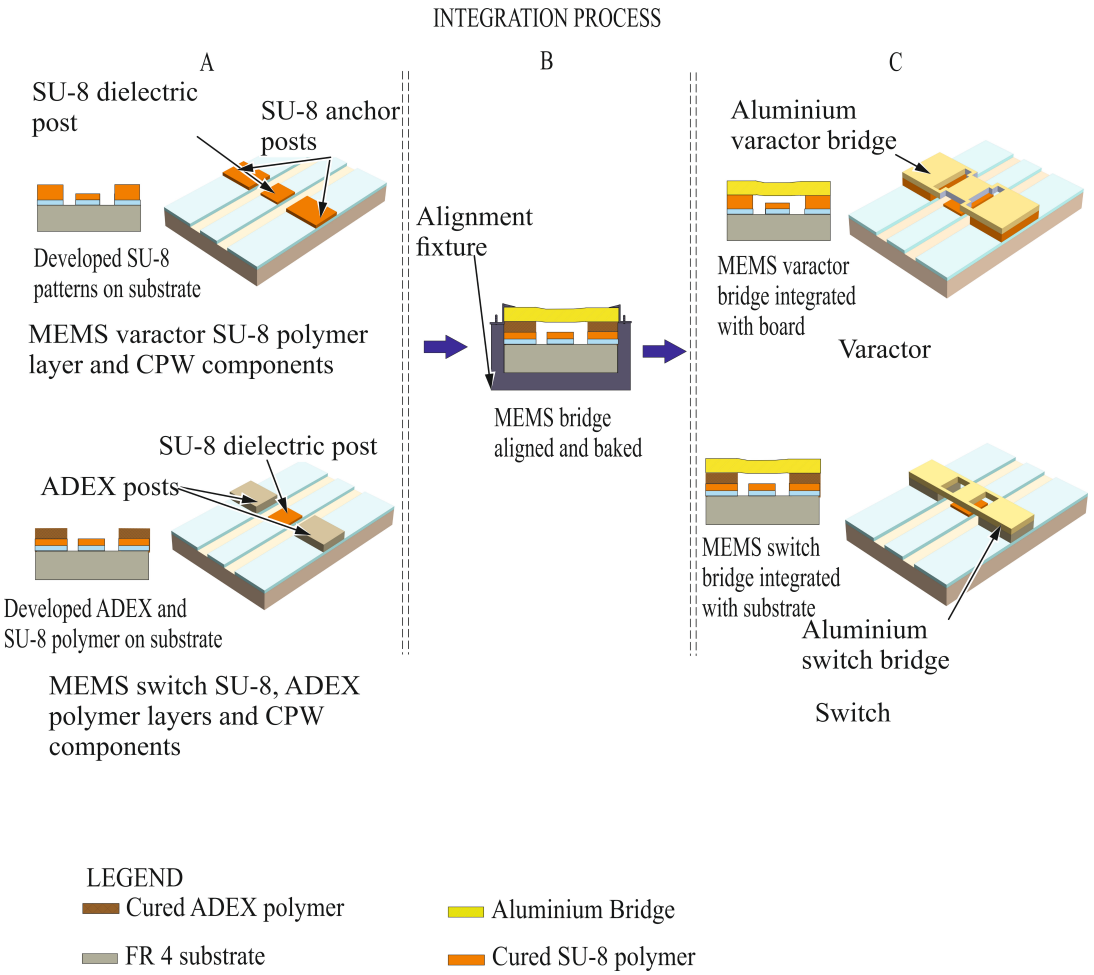

Figure 5.17 Integration process for fabricated MEMS devices.

This aligner fixture is as shown in Fig. 5.18, consists of a recess to make for the accommodation of MEMS device assembly, and fiducial embossed fixture cover with matching holes for the steel screw pins.

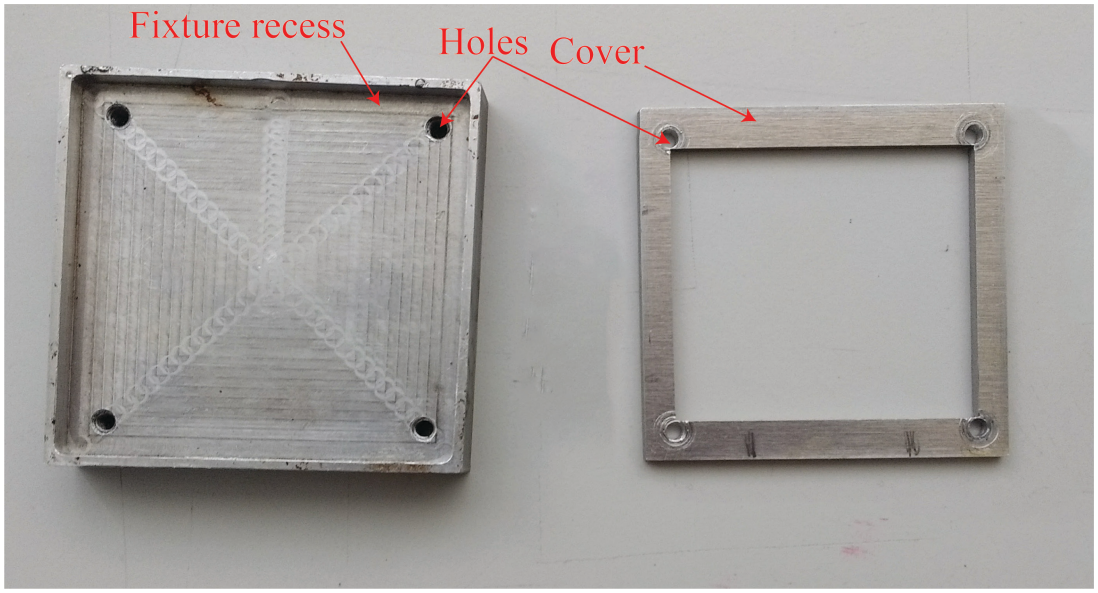

Figure 5.18 Alignment fixture for fabricated MEMS devices.

Each member is lowered into the alignment fixture, first the patterned substrate, then the Aluminium membrane, in calibrated steps with a calliper under careful observation through a microscope. Isopropanol (IPA) is used to rinse the wafer, and the sacrificial layers, to make for the air gap between the bridges and the transmission line. To further both ADEX polymer and SU-8 molecular polymerization and bonding to the aluminium membrane at the posts, thus making for a composite assembly, the substrate, MEMS bridge, and the alignment fixture posts were then hard baked at 150 ℃, ramped from 130 ℃ for two hours. This resulted in fully set composite structures. Finally, the now composite assembly was allowed to cool in graduated intervals 10 ℃ for every 5 minutes, and air dried to forestall the possibility of the MEMS bridges being pulled down by the surface tension of any leftover fluids or moisture.

MEMS shunt switch and varactor devices fabricated using the sum of these techniques: laser structuring, lithography/ADEX film emboss and device integration are shown suspended over the CPW transmission line depicted in the microphotograph Fig. 5.19 a) and a). Measured dimensions of fabricated structures are shown in Table 5.17.

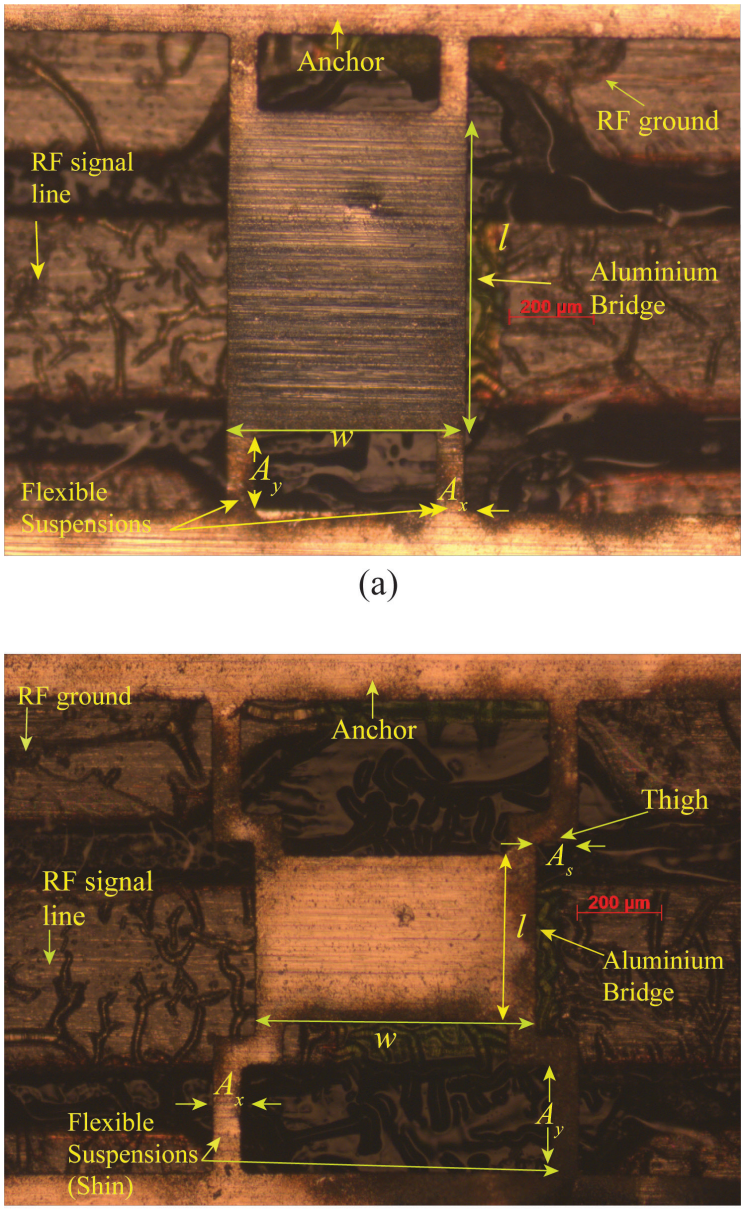

Figure 5.19 Microphotograph of the MEMS Aluminium switch and varactor.

Table 5.17 Measured dimensions for fabricated RF MEMS shunt switch and varactor.

Symbol	MEMS device geometry	Switch		Varactor	
		Design (µm)	Fabricated (µm)	Design (µm)	Fabricated (µm)
B_l	Bridge length	800	772	450	414
B_w	Bridge width	600	567	700	685
$w\ (A_x)$	Suspension width	50	46	50	45
$L\ (A_y)$	Suspension length	140	127	140	129
A_S	Thigh length	N/A	N/A	45	37
h_a	Bridge height	6	6.2	2	2.3
t_d	Dielectric height	1	1.1	1	1.2

5.3 Conclusion

In this chapter, the novel technique developed for the microfabrication of the MEMS switch and varactor has been discussed. The fabrication process entails only laser micro-structuring technique, non-cleanroom micro-lithography, standard wet-bench and hot-film emboss of dry film polymers to make for a low-cost micro-fabrication technique for manufacturing RF MEMS switches and varactors.

Characterisation of equipment employed and optimisation of the developed technique, at each cycle of the fabrication process was undertaken to make for a robust and cost-effective routine. Microstructuring of the MEMS upper membrane members, microlithography masks, and CPW transmission lines was facilitated by the LPKF Protolaser U3 laser machine. Optimization of line parameters was set to meet unique goals in each material, Aluminum foil, sheet and copper clad FR4 substrate. These goals have been discussed and chief among them was the accuracy of structured geometric features relative to design and repeatability. A flow chat functioned as routine to realise the optimise parameters in each instance and the efficacy is verifiable in the linear congruence between structured vectors with respect to design specifications and the highest deviation of 3.5 % for a structured vector. The wet bench lithography process was executed with relatively inexpensive solutions. Chemat KW-4A-CE spin coater and Chemat KW-4AC curer. Hot film emboss of the ADEX™ polymer was with the SKY 335R6 laminator. Optimisation of process factors was by the Taguchi design methodology which reduces the number of experiment test designs through the use of orthogonal arrays. It was employed with the wet bench and hot film emboss process, to make for optimized hybrid rapid prototyping manufacturing process with a reduction in build cycles while ensuring good yields.

In the switch, spin coated 1 µm SU-8 2002 deposits was used as centre dielectric layer, while the hot embossed 5 µm ADEX™ thin film polymers functioned as the bridge anchor support in the MEMS switch. The use of ADEX™ dry film presents lower capital investment and operating costs when compared to a spin coat process. Whereas in the varactor, the SU-8 deposit functioned as both centre 1 µm dielectric and 2 µm bridge support layers. The accuracy of these layers was within ± 0.2 µm. The lithography process included curing, development and post-processing, for example, MEMS members' integration and alignment. The latter was with a machined Aluminium block fixture. The alignment accuracy achieved between the two dielectric layers, i.e. the SU-8 and ADEX layers, was found to be, on average,

69 μm, while the alignment accuracy between the Aluminum sheet layer and the dielectric posts, using this method, was found to be, on average, 49.5 μm.

Following the development of the novel microfabrication method, and fabrication of the MEMS devices, measurement of the RF response of these devices to measure the degree of agreement with the design is described in chapter six.

Chapter 6
Fabricated MEMS shunt switch and varactor performance results and discussion

This chapter presents the measured RF and actuation response of the fabricated MEMS shunt switch and a varactor. A measure of the yield of this fabrication process, at each critical point of the build cycle, is also presented for evaluation of the efficacy of the proposed fabrication technique. We proceed with both measured RF and the actuation response, and a comparison of this response relative to simulation is also discussed to assess the degree of agreement with design objectives. All simulation results were obtained from the commercial 3D EM software package Ansys HFSS.

6.1 RF and actuation response

The RF response of both MEMS switch and varactor was measured from 0.25 GHz to 3 GHz by an E8316A PNA Network Analyzer, connected via SMA cables to 500 μm pitch coplanar probes Cascade Microtech microprobes, ACP-GSG-500, mounted on a Cascade Microtech 9600 Thermal probe station. This setup is as indicated in Fig. 5.1. The measurement was monitored by a combination of the still and video capture of an AmScope 5MP USB Microscope Digital camera connected to the C-mount of a stereo-zoom Olympus SZ-CTV 60 microscope. The DUT was held in place on the chuck by vacuum suction pressure provided by Charles Austen Dymax 30 vacuum pump. The effects of the right-angled SMA connectors and the 500 μm pitch, Microtech RF probes and the 3.5 mm VNA cables connected to the PNA were de-embedded by on wafer standard wideband SOLT calibration methods. Actuation of the device was provided by a series termination connection comprising an Agilent 6811B power supply, a 1 MΩ resistor, and a bias-tee separating connected SMA cables from feeding direct DC power to the PNA while allowing for RF measurements.

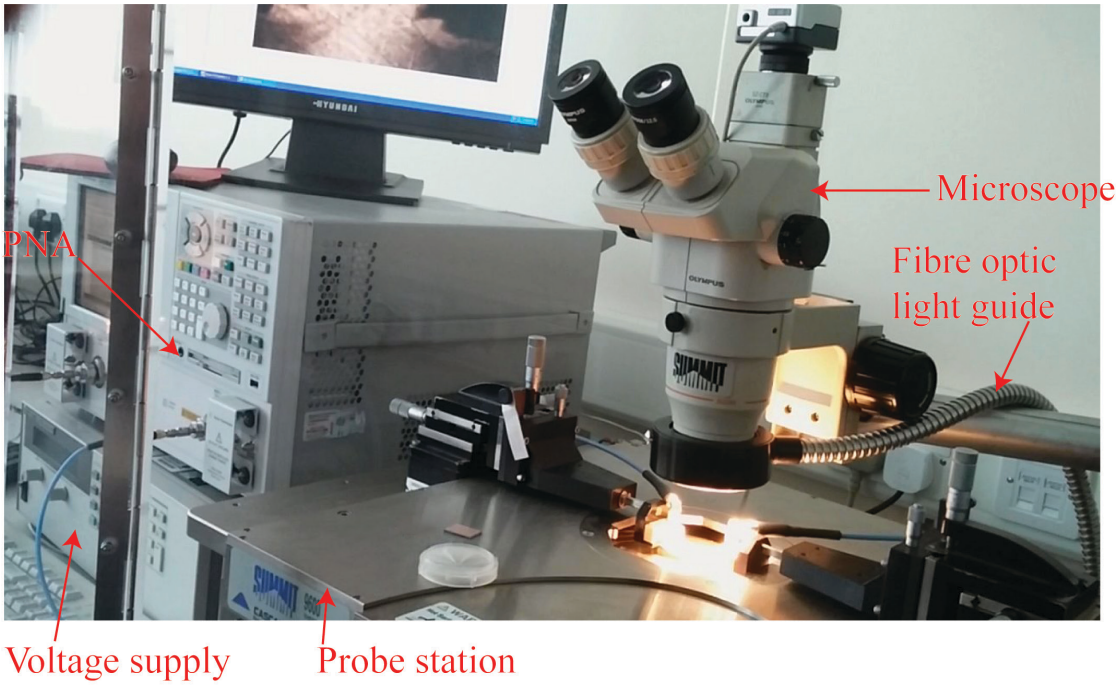

Figure 6.1 Measurement setup for MEMS switch and varactor.

6.1.1 MEMS shunt switch

A comparison between the response of simulated and measured reflection coefficient S_{11} and transmission coefficient S_{21} of the RF MEMS switch fabricated using the process is shown in Fig. 6.2 and Fig. 6.3, for the UP and DOWN states, respectively. The simulation response is indicated for

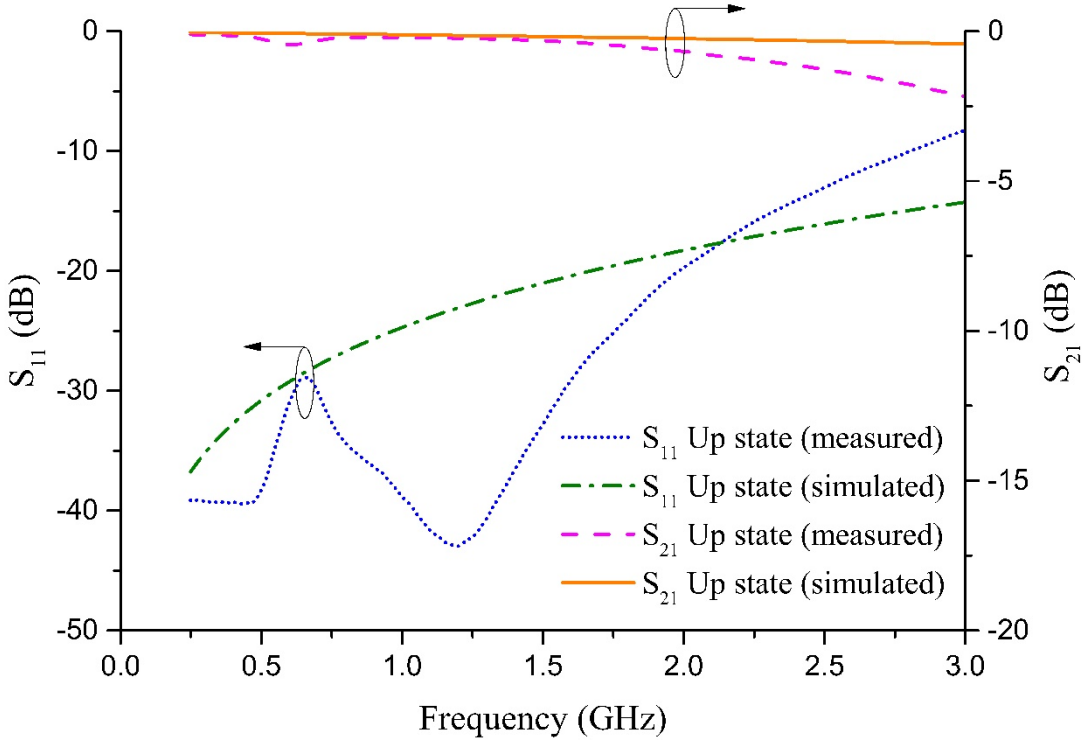

Figure 6.2 UP state transmission and return loss response of the MEMS Aluminium shunt switch.

fabricated geometry shown in Table 5.4. As shown in Fig. 6.2, the return loss of the MEMS shunt switch following the shunt loading of the CPW transmission line is measured at 2 GHz to be −19.6 dB, compared to a simulated value of −18.25 dB, for the UP state position. The transmission loss of this switch in the UP state from measurements at 2 GHz is found to be −0.63 dB, compared to −0.25 dB from simulations.

In the ON state or DOWN state, and for an actuation voltage of 140 V, the return loss of the switch from measurements at 2 GHz as indicated in Fig. 6.3, is −4.8 dB compared to −1.2 dB from simulations. The isolation of the switch at 2 GHz from measurements is also shown here to be −7.3 dB, and −7.6 dB from the simulations.

Deviations between measured and simulated responses are attributable to the inability to characterize actual dielectric constant and loss tangent of ADEX layer at the design frequency, the surface roughness of the FR4 substrates and the acknowledged misalignment of the ADEX anchor support layers relative to the SU-8 layer.

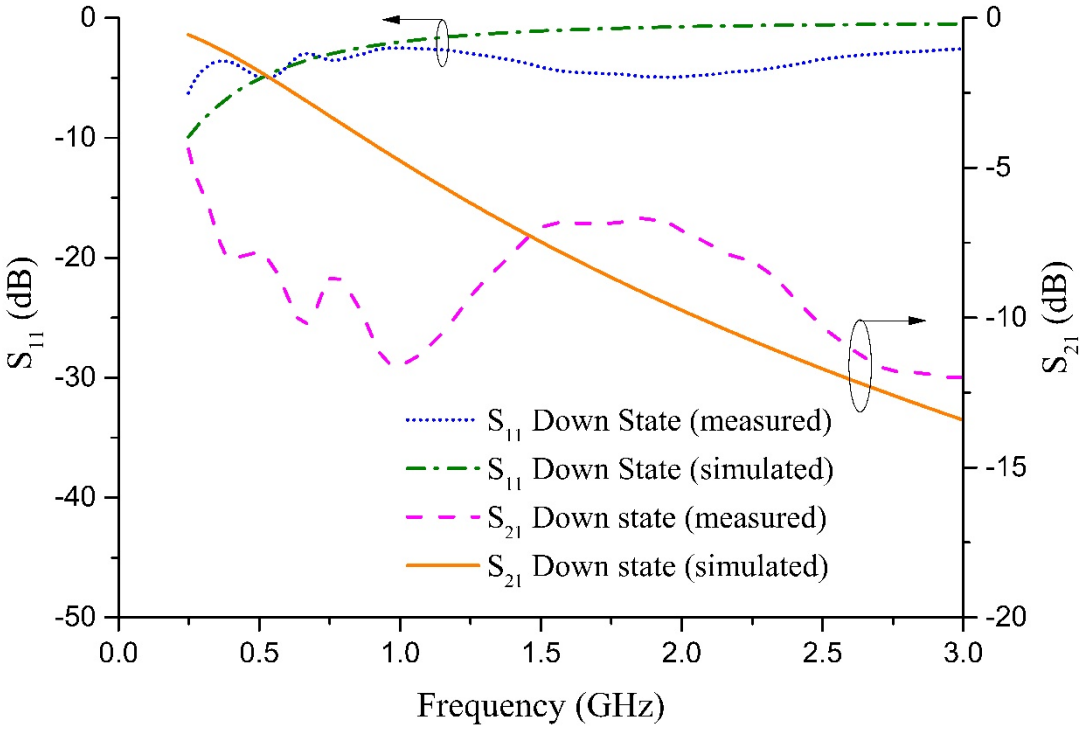

Figure 6.3 DOWN state transmission and return loss response of the MEMS Aluminium shunt switch.

6.1.2 MEMS varactor

The RF response of the fabricate varactor in the ON and OFF states were also measured, and are shown in Fig. 6.4 and Fig. 6.5 respectively. The return loss response for the varactor in the OFF (UP) state from measurements is shown

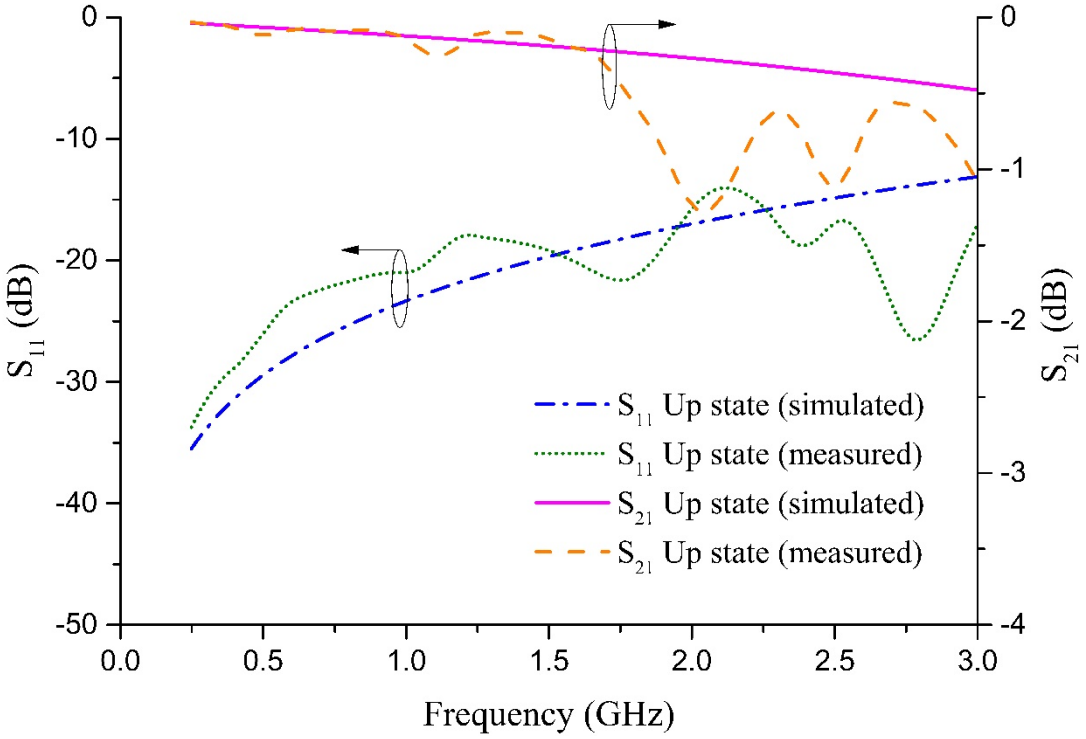

Figure 6.4 UP state transmission and return loss response of the MEMS Aluminium varactor.

to be −16.96 dB at 2.5 GHz, and −15.1 dB from the simulated response. A transmission loss response of −0.91 dB and −0.38 dB were also obtained from measurements and simulations respectively.

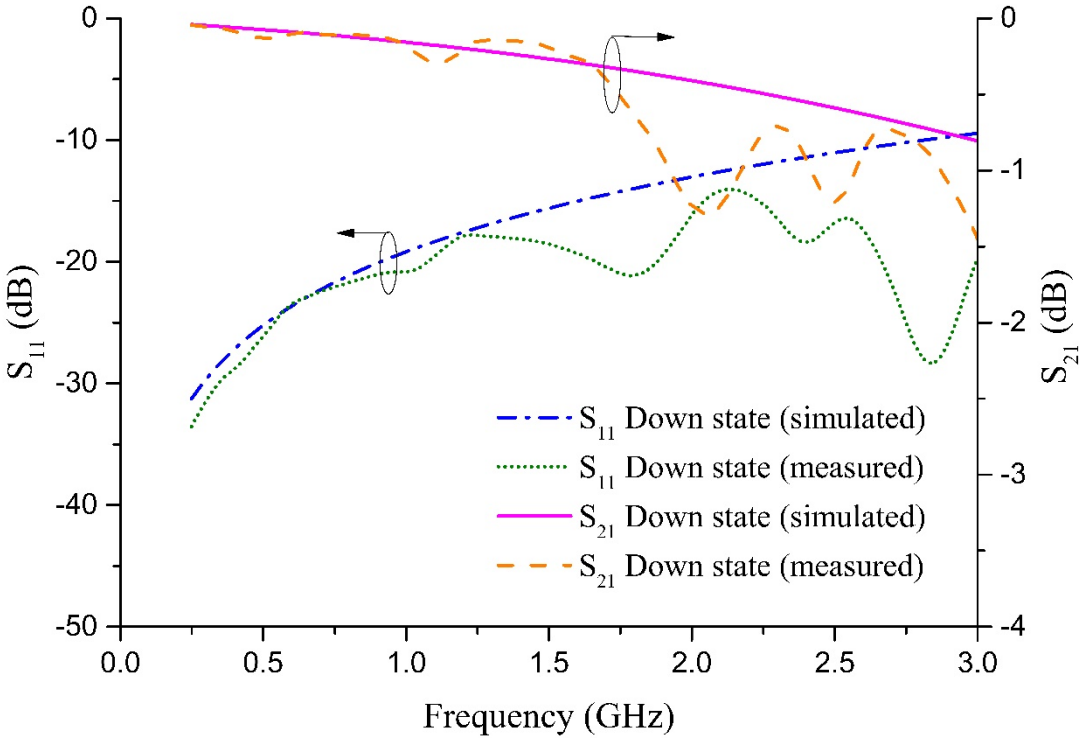

Figure 6.5 DOWN state transmission and return loss response of the MEMS Aluminium varactor.

In the ON or DOWN state, the measured return loss of the varactor is −16.35 dB at 2.5 GHz, compared to −11.3 dB obtained from simulations. The insertion loss is similarly measured to be −1.21 dB compared to a simulated −0.61 dB at 2.5 GHz. Deviations between measured and simulated responses are attributable to the surface roughness of the FR4 substrates and reported misalignment of the superseding SU-8 anchor support layers relative to the base post that was unaccounted in the simulation model.

The response of the varactor, when depicted on the Smith chart, makes for an assessment of the capacitance ratio over the frequency of interest and is indicated in Fig. 6.6.

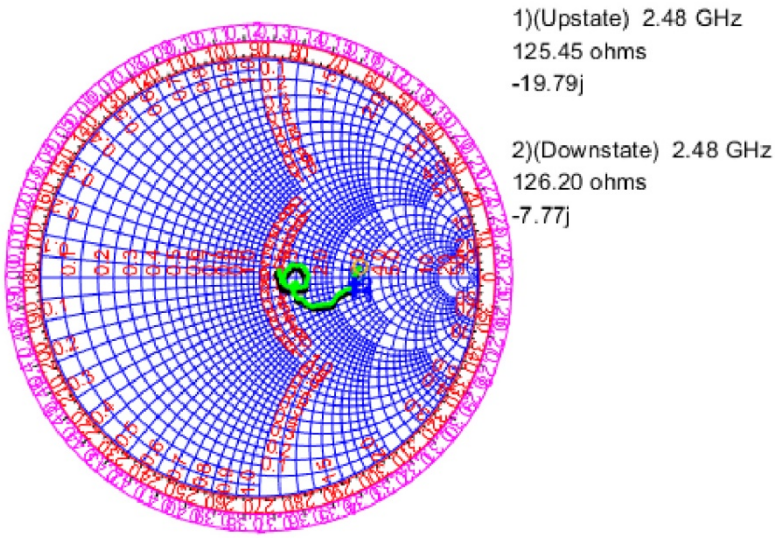

Figure 6.6 Smith chart response of the MEMS Aluminium varactor.

From (4.11), the capacitance ratio, C_r, is given as the ratio of the downstate capacitance C_d to the upstate capacitance C_u. The downstate and upstate capacitance at 2.48 GHz is derived from capacitive reactance, $X_{c_d} = 7.77\ \Omega$ and $X_{c_u} = 19.79\ \Omega$ are derived as,

$$C_d = {}^{1}\!\Big/\!_{\left(2\pi * 7.77 * (2.48 \times 10^9)\right)} = 8.26\ \text{pF} \tag{6.1}$$

$$C_u = \left({}^{1}\!\Big/\!_{2\pi * 19.79 * (2.48 \times 10^9)}\right) = 3.24\ \text{pF} \tag{6.2}$$

Thus C_r is obtained as,

$${}^{8.26\ \text{pF}}\!\Big/\!_{3.24\ \text{pF}} = 2.6 \tag{6.3}$$

This value closely follows the design C_r value of 4, and divergence are on account of the bridge and mechanical travel distance fabrication deviations relative to designed values.

A comparison of the performance of the MEMS devices with reviewed work is shown in Table 6.1.

Table 6.1 Comparison of key factors of reviewed fabricated RF MEMS devices.

Key factor	[111]	[112]	Our work
MEMs device type	Switch	Switch	Switch/Varactor
Membrane material	Gold/Chromium	Chromium/Gold	Aluminium
Operating Frequency	5 GHz	6 GHz	2/2.5 GHz
Insertion loss OFF (dB)	-36.6	-0.4	-0.63/-0.91
Isolation ON (dB)	-39.2	-16	-7.3/-1.21
Return loss OFF (dB)	N/A	-18	-19.6/-16.96
Return loss ON (dB)	N/A	-0.8	-4.8/-16.35
Actuation voltage (V)	93	37	121/19
Substrate type	Silicon/RO4003	TMM4	FR4
Fabrication techniques	Clean room (Evaporation/Lithography/ Sputtering)	Clean room (HDICP/Wet etching/ Electroplating)	Wet bench/ Hot film emboss/ Laser structuring
Fabrication complexity	Complicated	Fairly complicated	Simple
Overall costs (including materials)	Fairy high	Fairly high	Low

From this table, we observe that in [111], work aimed at reducing clean room based fabrication costs, explored a springless switch design fabricated with a three wafer assembly, consisting of a glass slide, a Rogers RO4003 board, and a silicon wafer. Feature patterning was achieved in the reviewed work using mask based resins for the Ta_2O_5 dielectric and the switch membrane derived from the thermal deposition of an Au/Cr layer. In [112], a four-mask process was employed to realize RF MEMS switch on a TMM4 PCB substrate. The Ti/Cu CPW transmission lines were formed by sputtering and patterning with FeCl. Si_3N_4, was employed as the dielectric layer, and deposition was by High-Density Inductively Coupled Plasma Chemical Vapour Deposition

(HDICP CVD) methods. The Cr/Au membranes were grown by electroplating the initial seed layer of Au film, which also served as the bridge anchor posts. Both reviewed work placed emphasis on employing cheaper substrates while still employing complex clean room techniques discussed in chapter two. With our work for the indicated response and given the challenges encountered, it is fair to conclude that our proposed method achieved the goals without complex cleanroom procedures and accompanying cost.

6.2 Yield of the fabrication technique

To optimize materials, labour costs, and increase the turnaround, it was decided that a modular design architecture is employed for each CPW based MEMS structure. Five separate MEMS devices were designed in the 50 mm x 50 mm substrate layout cluster, with 6 mm spacing between the devices to minimize the probability of critical failures for the two separate production cycles undertaken. The production cycles include the laser structuring and wet bench dry film lithography fabrication build cycles. The CPW transmission line estates on each workpiece were designed with excision marks to act as a guide for the laser during the removal of the MEMS placeholders MEMS after the assembly and as a way to identify impaired devices. This allowed for computation of the fabrication yield indicating the number of modular sections completing the process at each stage, relative to the number of starts.

The total yield is defined as Y_{total},

$$= Y_{laser} \times Y_{lithograpy} \tag{6.4}$$

The yield for the laser structuring stage is obtained using the Poisson yield model, which describes defects as spatially uncorrelated, uniformly distributed and one which conduces to a fault in the device. Thus for the extreme case, where there were M =2, numbers of possible defect types with M1= incomplete contour structuring, M2 =laser precut and heat phase fields overlap leading to deep incisions in the contour line bordering the vector, as shown in Fig. 6.7. Thus for C =5, number of devices per 50 mm x 50 mm workpiece, there are, $C^M = 5^2$ possible ways these two defects can be distributed. The probability that each work piece will contain zero defects of any type is given as given,

$$\left(1 - \frac{1}{C}\right)^M = 0.64 \tag{6.5}$$

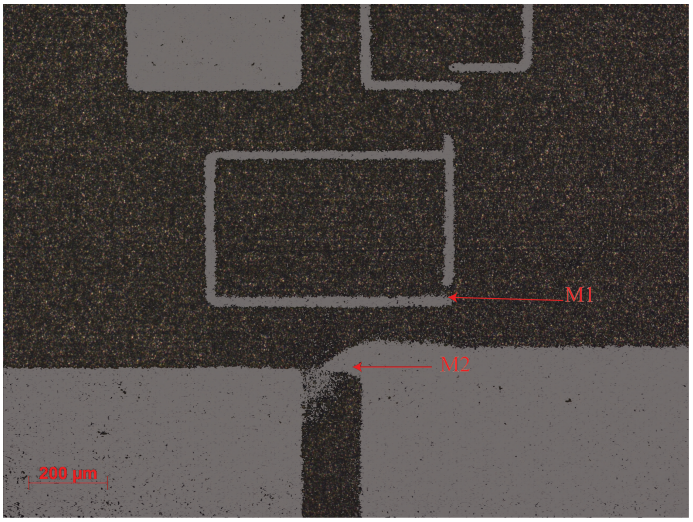

Figure 6.7 Aluminium sheet laser structuring defect types.

Thus substituting, $M = CA_cD_0$, the yield given as the number of work pieces with zero defect, results in the Poisson yield model limit expression expressed as,

$$Y_{laser} = \lim_{C\to\infty}\left(1-\frac{1}{C}\right)^{CA_cD_0} = e^{(A_cD_0)} = e^{(-0.4)} = 0.67 \quad (6.6)$$

where, $A_cD_0 = {}^{M}/_{C}$, and A_c is the critical area, D_0 is the defect density.

In a similar manner, the optimized lithographic process yield is defined by the absence of defects. This is indicated by the measured infinite electrical resistance between centre dielectric (A) lithographic patterns and the bridge anchors' support layers (B) on a test workpiece, as illustrated in Fig. 6.8. In addition, the degree of agreement of the pattern dimensions relative to the impressed design mask also served as a complimentary yardstick for the yield of the lithography process. With ten samples and two registered defects as described above, the lithographic yield is given by,

$$Y_{lithography} = \lim_{C\to\infty}\left(1-\frac{1}{C}\right)^{CA_cD_0} = e^{(A_cD_0)} = e^{(-0.2)} = 0.82 \quad (6.7)$$

The overall yield for the fabrication process, Y_{total}, from (6.1), (6.2) and (6.4) is given as,

$$Y_{total} = 0.82 * 0.67 = 0.56 \quad (6.8)$$

This computed yield closely follows the nominal ratio of functional fabricated devices (six) to the device cluster population size (ten) on each workpiece.

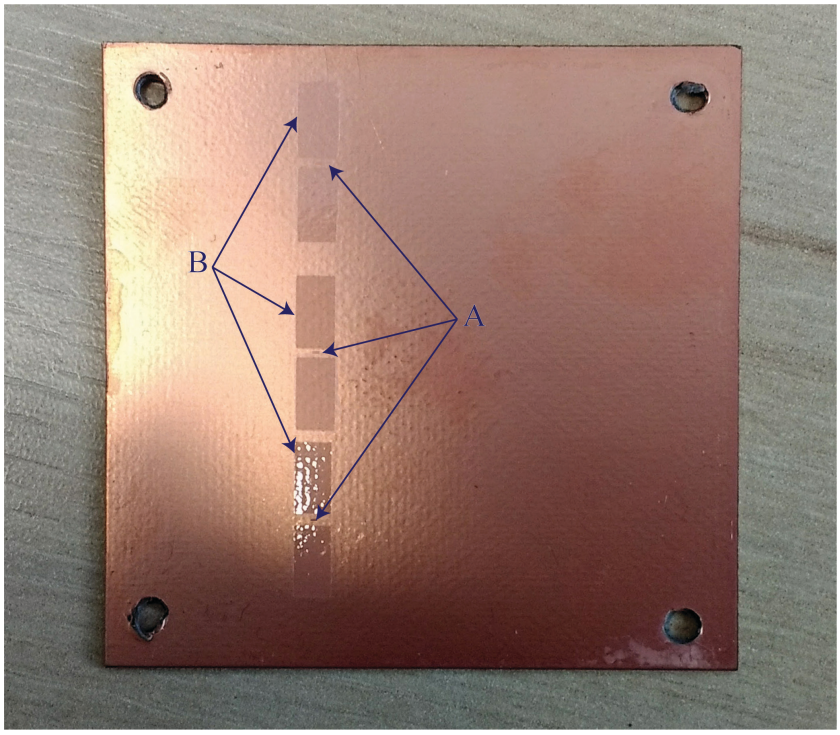

Figure 6.8 Lithography patterns isolation and defect categorization on a sample workpiece.

The cost of ownership (CoO) wasn't computed due to factors that were beyond our control. Some of which included access to machine downtime logs, repair and maintenance costs, and billing accounts for an aggregation of the hourly labour charge and rework rates. These data were inaccessible and are vital for making an accurate assessment of the laser machine's productivity per-fabricated device and an estimate of its lifetime. However, given the reported yields (67 %), short run time per lot for contour/rubout structuring (3/20 mins), CAM development time (10 mins) and warmup time (8 mins), the LPKF ProtoLaser U3™, employed as this project's main structuring tool, can be described as very good machine for achieving cost-effective rapid prototyping of MEMS, with a higher than average return on investment.

6.3 Conclusion

In this chapter, the RF response of both MEMS devices and the yield of the developed microfabrication technique were evaluated.

The computed yield was developed using the Poisson yield model and closely follows the ratio six functional fabricated devices relative to total cluster population size (ten) in each workpiece. This yield computed as ≈ 60%

describes the efficiency of the developed method as good, and admissible for further development and improvement.

A comparison between the simulated and measured reflection coefficient S_{11} and transmission coefficient S_{21} of both RF MEMS switch and varactor fabricated using the process presented in this chapter. The region of operation of these devices is up to 3 GHz, and measurement was with the E8316A PNA Network Analyzer. The states of these devices are electronically controlled by a bias voltage, 121 V for the switch, and 19 V for the varactor. A degree of agreement was observed between the measured and simulated response of both switch and varactor, with an isolation of -7.3 dB at 2GHz in the former and -1.21 dB at 2.5 GHz in the latter when actuated. The measured response show that the RF MEMS devices fabricated by using the novel micro-fabrication process present reasonable good figure-of-merits, achievable at much lower overall fabrication costs, as compared to the devices fabricated by conventional cleanroom process. Thus enabling the developed technique as a very good micro-fabrication process for cost-effective rapid prototyping of MEMS.

With the objectives met, a summary of the research embarked on and a discussion of recommended prospects involving developed technique follows and is presented in chapter seven.

Chapter 7
Conclusion and suggestion for future work

7.1 Conclusion

RF MEMS switches and varactors are fabricated on planar substrates, using conventional clean room fabrication methods as established in MEMS background theory. Cleanroom fabrication techniques consist of complex development cycles, which includes metal and dielectric film depositions, material patterning via etching and chemical processes. The associated investment and operational costs, for cleanroom equipment and maintenance, ensures relatively steep budgets are required to manufacture RF MEMS structures. Some research works aimed at lower costs have employed more complex processes and are still clean room based, and unsuited for rapid prototyping imperatives. In this research, a cost-effective micro-fabrication technique for manufacturing RF MEMS switches and varactors have been proposed. The techniques employed include laser micro-structuring, non-clean room micro-lithography, standard wet-bench and hot film emboss of SU-8 and ADEX polymers. The process results in similar design features with those obtained from conventional clean room based fabrication processes. The fabrication process is segmented to make for reusable work routines, and yield optimization, thus reducing the probability of critical failures in the whole assembly. The materials employed are readily available and conform with those that are employed in clean room processes, and the devices fabricated can compete with conventional complex processes. Cycle time for the lot which includes machine warm-up time, process queuing period and preparation with the optimized routines at each process stage averaged at three hours. An estimate of the cost of ownership which includes laser etching facility and tooling cost, lithography equipment installation cost, consumables, and yield conduces to a relatively inexpensive investment cost.

The design of the MEMS devices and the decision informing topology, layout, and materials choice were also examined. A description of the proposed fabrication techniques was expounded on, and an optimization routine for each build cycle presented. The MEMS movable structures were fabricated out of 14-μm-thick high purity Aluminium foils suspended above coplanar-waveguide transmission lines, implemented on top of FR4 substrates, via 5 μm thick ADEX polymer dielectric anchors for the shunt switches, and 2 μm SU-8 supports for the varactors. The 1 μm SU-8 dielectric layer atop the signal line make for increased capacitive coupling in addition to mitigating stiction.

Both MEMS structures and FR4 substrate were integrated using micro-patterned polymers, developed by using dry-film ADEX and SU-8 polymers, for a composite assembly. These structures were packaged on 51 mm x 51 mm substrates, as five 17 mm x 13 mm sub-component CPW circuit sections to maximize material usage and to provide statistical significance for optimization and yield measurements. This made for an improvement in the efficiency of the fabrication method. A comparison of the performance of fabricated MEMS devices relative to reviewed work was also presented.

The LPKF ProtoLaser U3™ served as the microstructuring workhorse in the fabrication of the MEMS membrane, lithography masks, and CPW transmission lines. Photoresist patterning through lithography techniques facilitated by the Chemat KW-4A-CE™ spin coater and Chemat KW-4AC™ curer, with alignment and integration by fiducial markers engraved on an in-house fabricated Aluminium block. These equipment were characterized to make for optimization of each build cycle stage as discussed in Chapter 4. The fabrication facility consisting of these machines a fume cupboard with a guard screen, blue light filters to minimize unwanted photoresist exposure. was found to be sufficient for the developed process. The techniques can be tailored to other materials with minor adjustments in the equipment operational parameters.

The potential of the developed fabrication method has been demonstrated in the efficiency and yield, from the fabricated planar devices. RF MEMS switches have been developed with comparable isolation for application in RF circuits. In addition, fabricated varactors have been shown to present the limited tuning expected for the designed frequency range. These devices have been shown to present minimal loss in their OFF state, thus lending credence to the efficacy of the design and fabrication methods developed. The simulated and measured response of both devices were found to be in good agreement over the 2 GHz to 3 GHz frequency range.

7.2 Suggestions for future work

We’ve demonstrated the efficacy of low-cost fabrication technique developed for the passive RF MEMS components packaged on planar PCB substrates. The work presented in this technique is open to improvements especially with improvements in the alignment stage, through the use of additional alignment pins, complementary cross reference interfaces such as crosshair reticles,

progressively smaller diameters, and a vertical translational mechanism for steady placement of structured layouts. This might come at increased costs, but are invaluable to realizing ≤ 50 µm cross-sectional structures where alignment is critical to them functioning as designed. The current level of accuracy is acceptable for this frequency range, especially given how cost-efficient the process is, and can be extended to higher frequencies with increased alignment accuracies, and to traditional clean room based substrates, including Low-Temperature Co-fired Ceramics (LTCC).

Additional research work involving cost-effective fabrication methods for further consideration is discussed in the next sections.

7.2.1 RF MEMS for reconfigurable switching matrices

MEMS switches present research opportunities for convenient replacement of PIN diodes (used in base stations) and coaxial based switches (used in satellite systems), as the demand for miniature switch-matrices systems for switching and rerouting of RF signals in terrestrial and satellite telecommunication platforms [113, 114]. With minimal estate requirements, it is possible to increase the complexity of the switching unit, via an increase in the number of channels, while still meeting isolation requirements without unwieldy increases in size, weight, and implementation costs. In addition, with the replacement of existing coaxial switching system in satellites by RF MEMS switching circuits, it is possible to envision the development of whole front end system integration on a chip (SoC).

The basic component for more complex switching and commutation schemes can be considered to be the single pole, double throw (SPDT) switch, which is a T-like path, where the input RF signal can be diverted to one of the two

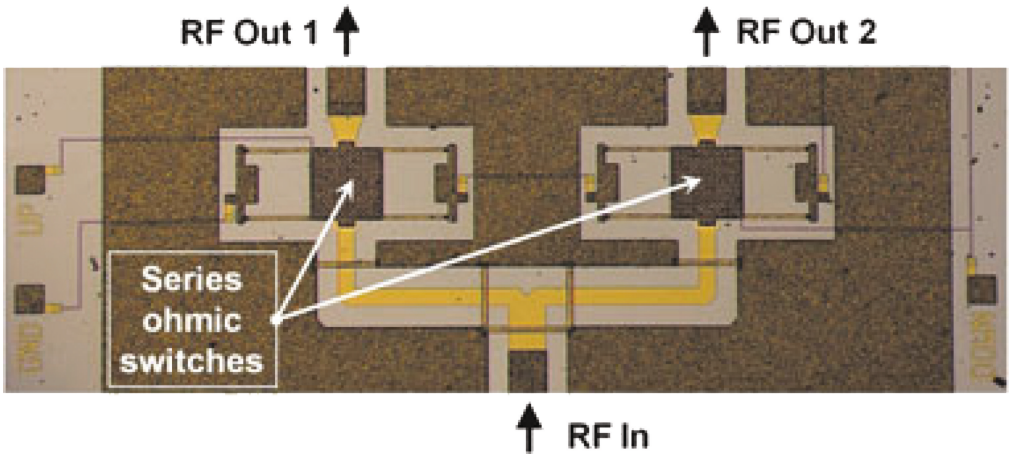

Figure 7.1 Microphotograph of an RF-MEMS based single pole, double throw switch realized in the micromachining process [113].

output branches, to both of them, or to neither of them [113]. A micrograph of this an RF MEMS equivalent is indicated in Fig. 6.1. They are based on established designs and developed with conventional clean room based processes, marked by their associated implantation costs and complexity for a staircase layout as reported in [114].

A method for rapid prototyping of this reconfigurable switching system, while fulfilling RF response requirements would be welcomed as a cost-effective approach, attractive for teaching, commercial and defence end use. Extant laser structuring equipment like the LPKF ProtoLaser U3™ or newer models, LPKF ProtoLaser U4™, with reportedly higher precision, stability, and ablation abilities would make convenient workhorses for this envisioned project, alongside switch post-patterning as examined in this work.

7.2.2 PCB based microfluidics systems

In contrast to silicon-based technologies, PCB based fluidic systems allow for low-cost integration of sensor electronics alongside enclosed fluidic channels. In addition, with classical PCB technology, integration of fluidic components on the same board, and definition of fluidic interfaces for other components readily available [115]. Examples of fluidic microsystems in PCB technology are sensors for temperature, flow rate, colour, pH-value, pressure; and micropumps active and passive The PCB embedded cavities are bordered by copper lines on both sides and a top cover made of glass, ceramic or plastic cover to make for an encased assembly. A PCB based microfluidic system is shown with the top cover lifted in Fig. 7.2

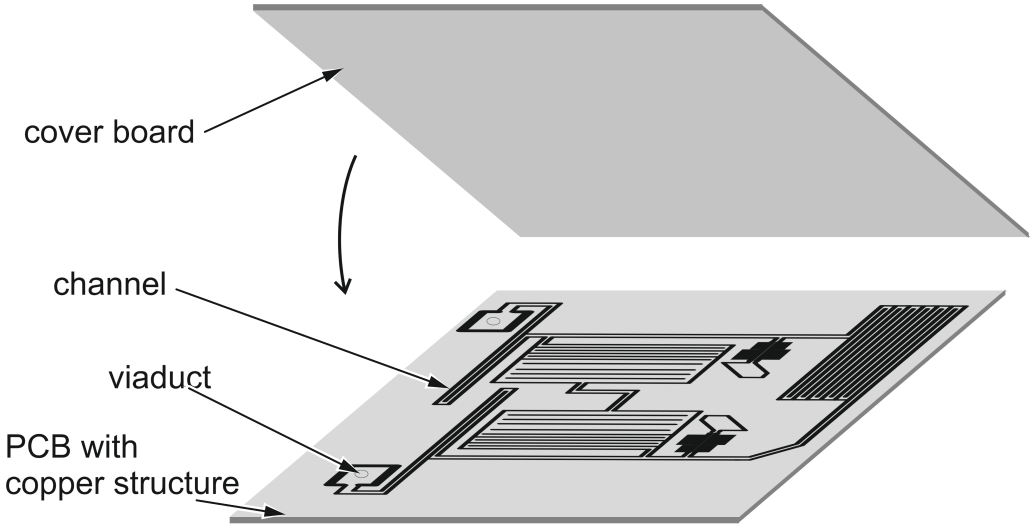

Figure 7.2 PCB based fluidic system of different elements in PCB technology (the cover board is shown lifted up) [115].

The cross-section of the cavity is defined by the thickness of copper on the PCB and by the distance between the bordering copper lines. The copper bordering the microfluidic channel can be protected with resins films, beneficial for protection of the hygroscopic PCB board materials against the effects of fluids, e.g. swelling, and in reducing the influences of toxic copper on the fluids. This property was exploited in [116], with FR4 board laminates used to house fluidic based environmental sensing systems.

It is fitting to propose the inexpensive fabrication process employed here, and in the co-authored work [117] as the template for exploring this opportunity based on the success recorded. The cavity structuring can be realized with the laser process, and the ADEX epoxy polymer to act as resin, given its bonding properties to host of material after heat treatment. An annealing system can also proceed with the application of the resin in the microchannel. The potential for this cost-effective method for fabricating this microfluidic system makes it an allure for consideration in future works.

7.3 Publication

The paper presented here originated during the course of this work and a copy has been deposited in the University repository.

I. E. Obuh, V. Doychinov, D. P. Steenson, P. Akkaraekthalin, I. D. Robertson, and N. Somjit, "Low-Cost Micro-Fabrication for MEMS Switches and Varactors," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* doi:10.1109/TCPMT.2018.2834865 (received 8th December 2017; final revision, 30th March 2018; accepted, 7th May 2018)

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Appendix A
Measured fabrication and design results for test pieces used to optimize laser parameters.

This appendix presents a tabular list of measured and design dimensions for geometries used to optimize the laser parameters. The parameters are described separately for Aluminium based materials and Copper-based materials respectively. Development of the parameters followed the flow chart specified in Fig. 4.4, from an understanding of the role the parameters play in the ablation and structuring process.

Table A.1 Measured and design geometries for Aluminium based workpieces used to optimize the laser parameter.

Material (Aluminium)	Measured fabrication instances								Average	STDEV
	1	2	3	4	5	6	7	8		
Suspension width 45 µm	36	38	34	40	38	35	35	35	36.375	2.066
Strip width 55 µm	44	40	39	36	32	39	38	41	38.625	3.543
Suspension width 140 µm	114	108	104	133	123	103	105	104	111.75	10.951
Switch bridge width 600 µm	570	567	572	574	571	562	575	573	570.5	4.243
Switch bridge width 800 µm	758	769	763	767	768	779	770	766	767.5	6.024
Strip length 980 µm	968	971	969	969	971	963	969	976	969.5	3.625

Table A.2 Measured and design geometries for Copper based workpieces used to optimize the laser parameter.

Material (Copper)	Measured fabrication instances								Average	STDEV
	1	2	3	4	5	6	7	8		
Strips 45 µm	49	47	45	48	49	45	44	45	46.50	2.000
Copper gap 70 µm	61	65	64	63	64	62	63	72	64.25	3.370
Bridge post length 115 µm	112	116	113	114	115	117	121	112	115.00	3.024
Signal line 430 µm	433	415	441	433	434	447	436	435	434.25	9.146
Strip length 12180 µm	12195	12166	12112	12158	12198	12198	12198	12166	12173.90	30.230

Appendix B
Lithography and integration process for fabricated MEMS switches and varactor.

This appendix presents detailed fabrication processes for the shunt MEMS switch and varactor presented in this thesis. The processing was executed on FR4 substrates in a wet bench fabrication facility equipped with a fume cupboard and a guard screen found to be sufficient for the developed process. Additionally, blue light filters were installed on the lights inside the lab to minimize unwanted photoresist exposure. The routine developed for both devices proceeds as follows.

B.1 MEMS switch lithography and integration fabrication process

A breakdown of specific processes employed in the fabrication of the MEM switch in this thesis is listed below.

B.1.1 SU-8 pattern and ADEX film processing

The substrate is a 50 mm x 50 mm, 1.524 mm thick FR4 substrate, with 0.5 oz. double sided copper cladding. All processing is single sided, and on the laser structured CPW transmission line.

1. Substrate pretreatment
   (a) Clean the substrate by agitating in acetone for 3 minutes.
   (b) Soak in Isopropyl alcohol(IPA) for 6 minutes.
   (c) Rinse off IPA by immersing the substrate in deionized water and agitating for 5 minutes
   (d) Air dry the substrate for 5 minutes
   (e) Dehydrate the substrate at 95 ℃, ramped up from ambient temperature for 3 minutes.
2. Spin coat
   (a) Secure the substrate on the Chemat KW-4A-CE spin coater, with vacuum pump switch, turned on.
   (b) Set first stage spin speeds at 500 rpm for a duration of 12 s, and second stage spin speed fat 4000 rpm for a duration of 40 s.
   (c) Apply 2 ml of SU-8 2002 to the centre of the substrate with a pipette.
   (d) Turn the spin coater speed switch on to uniformly spread out the SU-8 2002.
   (e) Beads formed at the substrate edge can be trimmed with a slicer following pickup of the substrate.

(f) Turn the vacuum switch off and power switch off, and clean with a clean acetone damped cloth.

3. Softbake
   (a) Prebake the substrate at 65 ℃, on the hotplate for 10 s.
   (b) Ramp to 95 ℃ and bake for 60 s.
   (c) Cool the hot plate first back to 65℃, and the ambient temperature in graduated steps of 15 ℃, for every 2 minutes.
4. Exposure
   (a) Secure the substrate in the aligner and check for matching fiducial.
   (b) Place lithography mask atop the substrate in the aligner, and secure with cover and screws.
   (c) Place the assembly in the Chemat KW-4AC curer, and set the timer for 11 minutes.
   (d) Turn on the curer for UV exposure.
5. Post Exposure Bake (PEB)
   (a) Retrieve substrate from the aligner, and bake on the hotplate at 65 ℃ for 30 s.
   (b) Ramp to 95 ℃ for 180 s, in intervals of 15 ℃ for 45 s from 65 ℃.
   (c) Cool back first to 65 ℃ on the hotplate and then slowly back to room temperature spread over 15 minutes.
6. Development
   (a) Pour 50 ml Propylene Glycol Methyl Ether Acetate (PGMEA) developer into the 250 ml beaker.
   (b) Place the substrate in the developer and gently agitate for 180 s.
   (c) Extract the substrate, and rinse in IPA by agitating for 10 s and then deionized water for 30 s.
   (d) Allow to air dry for 10 minutes.
7. Lamination of ADEX thin film sheet
   (a) Remove ADEX sheet PP cover in ambient temperature.
   (b) Turn SKY 335R6 laminator on, and allow to heat to set temperature of 65℃, alongside rollers speed on defined at 0.3 m/min. Check temperature and speed are at defined settings by pressing the hot button.
   (c) Place steel support sheet on the flat platform in front of the laminator, at 2.5 cm from the rollers.
   (d) Place a protective transparent laminator sheet atop the same size as the steel support sheet.

(e) Press the RUN button to start the rollers, and run until the upper protective laminator sheet is just under the rollers, then stop the rollers with the STOP button.
(f) Place the ADEX laminate sheet atop the substrate with the film pressed against the side to be laminated, and both placed 2 cm from the leading edge of the steel sheet.
(g) Press the RUN button, to start the rollers and insert the support sheet into the laminator, with the support sheet folded over the roller assembly. The entire assembly now feeds into the roller and would exit at the roller end guard.
(h) Allow for 60 s to cool, and then gently remove the protective laminator cover, and then slowly peel the ADEX carrier PET sheet at room temperature.
(i) Clean both steel and laminator protective sheet with acetone and allow to dry, and feed into laminator to clear out any creases for reuse purposes.

8. ADEX pattern exposure
   (a) Place substrate in the aligner and ensure fiducial.
   (b) Secure the lithography mask atop the substrate with the aligner jig cover and screws.
   (c) Place the substrate in the Chemat KW-4AC curer and expose the assembly for 15 minutes.
9. ADEX pattern post exposure bake (PEB)
   (a) Extract the substrate from the aligner fixture, and bake at 95 ℃ for 9 minutes.
   (b) Cool back to room temperature on the hotplate in graduated amounts of 15 ℃ for every 3 minutes.
10. ADEX pattern development
   (a) Soak the substrate in the Cyclohexanone developer, ensuring it is well immersed.
   (b) Agitate the developer and the substrate for 6 minutes.
   (c) Remove the substrate from the developer and rinse in IPA while agitating for 30 s, and in deionized water for 30 s.
   (d) Allow to air dry for 5 minutes.

B.1.2 MEMS switch integration

With the patterned ADEX anchor posts and SU-8 dielectric layer now processed, the procedure to obtain a composite assembly with the bonding of the Aluminium bridge on the substrate follows.

1. Alignment and hardbake

(a) Retrieve the air-dried substrate from the fume cupboard and situate in the aligner.

(b) Position substrate and alignment fixture fiducial holes such that they are matching.

(c) Place the MEM Aluminium membrane alongside the attached placeholders on the substrate and alignment fixture, and check for matching fiducial.

(d) Secure the recess cover with screws and place the assembly on the hotplate.

(e) Bake the assembly with the fixture at 150 ℃, ramped from 130 ℃ for two hours, to ensure all structures are set.

(f) Allow assembly to cool back to room temperature.

(g) Extract the recess cover, and excise device placeholders with structuring over predefined excursions.

(h) Clean the MEMS device with IPA, and allow to dry in air.

B.2 MEMS varactor lithography and integration fabrication process

The fabrication routine used to realize the MEMS varactor follows the set of processes employed in the fabrication of the MEM switch with modifications in the SU-8 patterning, to account for the multilayer construct of the device.

B.2.1 SU-8 pattern and device integration

The initial centre dielectric fabrication process follows steps 1-5 indicated in Appendix B.1.1 and is referred to in step 1. The fabrication process is described as follows.

1. Follow steps 1-5, in appendix B.1.1
2. An additional coat of SU-8.
   (a) Place the substrate with the initial baked layer on the Chemat KW-4A-CE spin coater, and turn the vacuum pump switch on.
   (b) Set spin first stage speeds at 500 rpm for a duration of 15 s, and second stage spin speed at 4800 rpm for a duration of 45 s.
   (c) Apply 2 ml of SU-8 2002 on to the centre of the substrate with a pipette, and proceed with spreading the coat over the substrate by switching the coater on.
   (d) Eliminate beads formed at the edge by trimming with the slicer in the pickup of the substrate

3. Softbake of the coated layers.
   (a) Prebake at 95 ℃ for 60 s, with ramped increases of 30 ℃ from room temperature.
   (b) Cool the hot plate back to room temperature following and allow to cool for 2 minutes.
4. Exposure of the additional layer
   (a) Place the substrate in the aligner's recess and position the fiducials so they match.
   (b) Secure the lithography mask atop the substrate in the aligner with the cover and screws.
   (c) Place the assembly in the Chemat KW-4AC curer, and set the timer for 15 minutes.
   (d) Proceed with curing by turning the Chemat KW-4AC power on.
5. Post-exposure bake of the coated layers.
   (a) Extract the substrate from the aligner, and detach the masks.
   (b) Bake the substrate on the hotplate at 65 ℃ for 30 s, and ramp to 95 ℃ for 3.5 minutes.
   (c) Cool back to ambient temperature on the hotplate.
6. Device alignment.
   (a) Place substrate in the alignment fixture such that fiducial holes match.
   (b) Gently place the MEMS Aluminium membrane on the substrate and check for matching fiducial.
   (c) Secure the recess cover and the assembly with screws and bake at 95 ℃ for a further 60 s.
7. Development
   (a) Retrieve substrate and bonded membrane from the aligner
   (b) Submerge in PGMEA, and slowly agitate for 180 s.
   (c) Extract the substrate and rinse in IPA by agitating for 10 s.
   (d) Dry in air for 10 minutes.
8. Hardbake
   (a) Place the substrate on the hotplate and bake at 150 ℃ for 30 minutes, ramping from room temperature.
   (b) Ramp back down to 95 ℃, for 5 minutes and to room temperature.
   (c) Cool for 15 minutes in the fume cupboard.

B.3 Alignment accuracy

The alignment accuracy is defined as the measure of the layer to layer registration as designed, relative to that obtained from the lithographic process. It is indicated for the SU-8 and ADEX, layers in both x and y planar directions. In addition, the integration and alignment of the Al bridge relative to the ADEX layer are also characterized by the measured skewness in both x and y directions for the fabricated devices. To illustrate this, please refer to Fig. B.1 below:

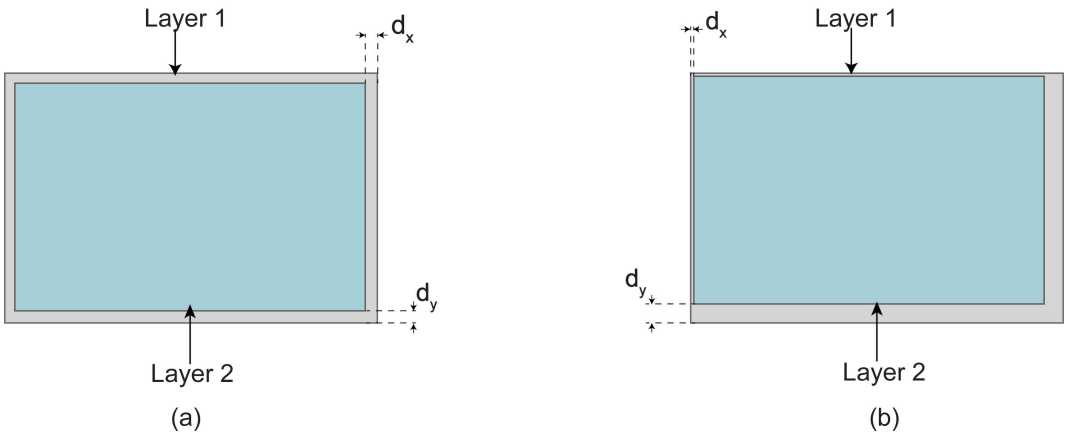

Figure B.1 a): Alignment between layers, as designed and simulated in Ansys HFSS. **Figure B.1 b):** Alignment as observed following fabrication and integration.

The design in Fig 1 a) was set for dx=dy=0 in both x and y directions. Misalignments in these directions were measured and averaged for the six working devices that were fabricated. The average alignment accuracy between the initial SU-8 layer and the overlying ADEX layer across both x and y planar directions was measured to be 69 μm. Similarly, the alignment accuracy of the Al bridge to the ADEX layer was found to be 49.5 μm.